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10-GHz band 2 × 2 phased-array radio frequency receiver with 8-bit linear phase control and 15-dB gain control range using 65-nm complementary metal–oxide–semiconductor technology

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Abstract

We propose a 10-GHz 2 × 2 phased-array radio frequency (RF) receiver with an 8-bit linear phase and 15-dB gain control range using 65-nm complementary metal–oxide–semiconductor technology. An 8 × 8 phased-array receiver module is implemented using 16 2 × 2 RF phased-array integrated circuits. The receiver chip has four single-to-differential low-noise amplifier and gain-controlled phase-shifter (GCPS) channels, four channel combiners, and a 50-Ω driver. Using a novel complementary bias technique in a phase-shifting core circuit and an equivalent resistance-controlled resistor–inductor–capacitor load, the GCPS based on vector–sum structure increases the phase resolution with weighting-factor controllability, enabling the vector–sum phase-shifting circuit to require a low current and small area due to its small 1.2-V supply. The 2 × 2 phased-array RF receiver chip has a power gain of 21 dB per channel and a 5.7-dB maximum single-channel noise-figure gain. The chip shows 8-bit phase states with a 2.39° root mean-square (RMS) phase error and a 0.4-dB RMS gain error with a 15-dB gain control range for a 2.5° RMS phase error over the 10 to10.5-GHz band.

KEYWORDS
frequency modulated continuous wave, phased-array, phase-shifter, radar, receiver

1 | INTRODUCTION

Phased-array antenna configurations generate a high gain and flexible beam steering, enabling long-range, wide-angle coverage in radar applications. In this type of architecture, radio frequency (RF) phase shifting is predominantly used due to its advantages of high pattern beam directivity and simple design, which are less costly than local oscillator and intermediate-frequency phase-shifting designs [1, 2].

In the RF domain, phase shifting with a large array size typically involves using a 2 × 2 RF integrated circuit (RFIC) and an H-tree interconnection, owing to its symmetric structure [3–5]. However, print mismatches can

degrade phased-array performance, even with an H-tree. Therefore, the 2 × 2 RFIC has a high phase resolution, enabling it to be calibrated to compensate for the variances among channels. This is also necessary for amplitude-comparison monopulse radar applications because they require finer beam steering in their subarrays [6].

The 2 × 2 RFIC's weighting factors must also be controllable to reduce its side-lobe beams. This is achieved by controlling the gain of each phased-array element to minimize gain-control phase variations. Attenuators with switched resistors have been widely utilized in conventional designs for this purpose, but they require careful engineering and consume large chip areas owing to the many switches and complicated compensation circuits needed [7–9].

Recently, several studies have been published on phase shifters with high phase resolutions [10–14]. However, the circuit structures needed to obtain high phase resolutions and high gain controllability are unusual. To address this problem, a vector-sum chip structure was proposed in Park and others [14]. However, it requires large current consumption due to its dual-vector structure and gain-control bias current. Additionally, the conventional Gilbert cell-type vector adder with a three-stack of negative metal–oxide semiconductor transistors reduces the output headroom (the dynamic range of the receiver) and increases power consumption owing to the high supply voltage [1, 11, 14].

Our proposed 2 × 2 phased-array RF receiver offers increased phase resolution and weighting-factor controllability with low current consumption and a small area owing to its simple design and low 1.2-V supply voltage. It is intended for use in unmanned aerial vehicle detection radars in an 8 × 8 array and has a range resolution of 1 m at a bandwidth of 150 MHz [15–18]. Owing to the large array size required for such applications, the costs of high phase resolution, weighting factor controllability, low power consumption, and small die size are greatly lowered.

2 | BUILDING BLOCK DESIGNS

Figure 1 illustrates a block diagram of the proposed 2 × 2 phased-array RF receiver, which has four single-to-differential low-noise amplifier (LNA) and gain-controlled phase-shifter (GCPS) channels, a four-channel combiner, and a 50-Ω driver. The four channels are combined using a current-summing method with a transconductor (g_m). The LNA provides three-step gain controllability (21/13/6 dB) to increase its input dynamic range and includes a serial-to-parallel interface that

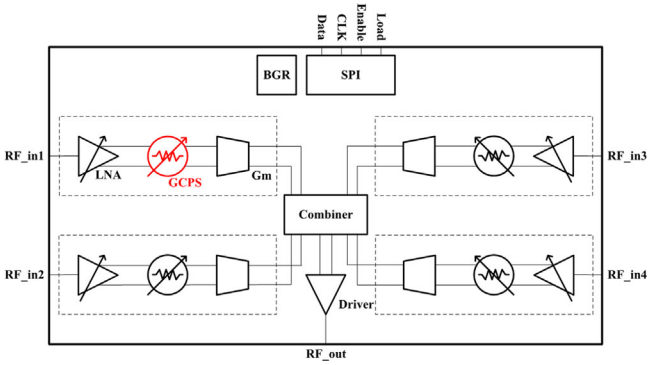

FIGURE 1 Integrated 2 × 2 phased-array radio frequency (RF) receiver block diagram.

controls its internal blocks and integrated bandgap reference circuit. All input–output pads (precisely RF, digital, and power-supply types) are protected using standard electrostatic discharge cells.

The proposed integrated low-voltage vector-sum phase-shifter circuit for high phase resolution and gain controllability is shown in Figure 2. The phase shifter comprises a quadrature generator, vector adder, 6-bit digital-to-analog converters (DACs), and a current mirror.

The quadrature generator is designed with a two-stage resistance–capacitance poly-phase filter (PPF) for small area consumption, wide bandwidth, tolerable signal loss, and precise quadrature phase [19, 20]. To compensate for signal loss in the two-stage PPF, an amplifier is added to the front of a Type-I PPF [12], and two pole frequencies are split to decrease the in-phase/quadrature (IQ) amplitude difference for wide bandwidth. The IQ phase difference of a Type-I PPF is inherently 90° over the bandwidth.

A vector adder is constructed using two cascode variable gain amplifiers (VGAs) connected by quadrant selection switches and controlled with 2-bit digital input. The cascode VGAs with two-stack transistors increase the output headroom over that of the conventional three-stack Gilbert-cell type VGA. However, owing to the phase-control code sweep, the output phases are nonlinear when lacking CBCs because the VGA bias conditions differ in terms of the reference DAC and current-mirror bias conditions. Therefore, CBCs are added to the transistor drains of the cascode input stages for output phase linearization according to the phase-control code sweep.

Two binary-weighted 6-bit current-mode DACs control the bias ratio, I_Q/I_I, for output phase generation, and the control inputs of the DACs are set such that $I_Q + I_I$ is constant for all phases of the constant amplitude response at the output of the vector adder. In the DAC, a unit cell circuit is used to turn the current on and off. Without this complementary metal–oxide semiconductor

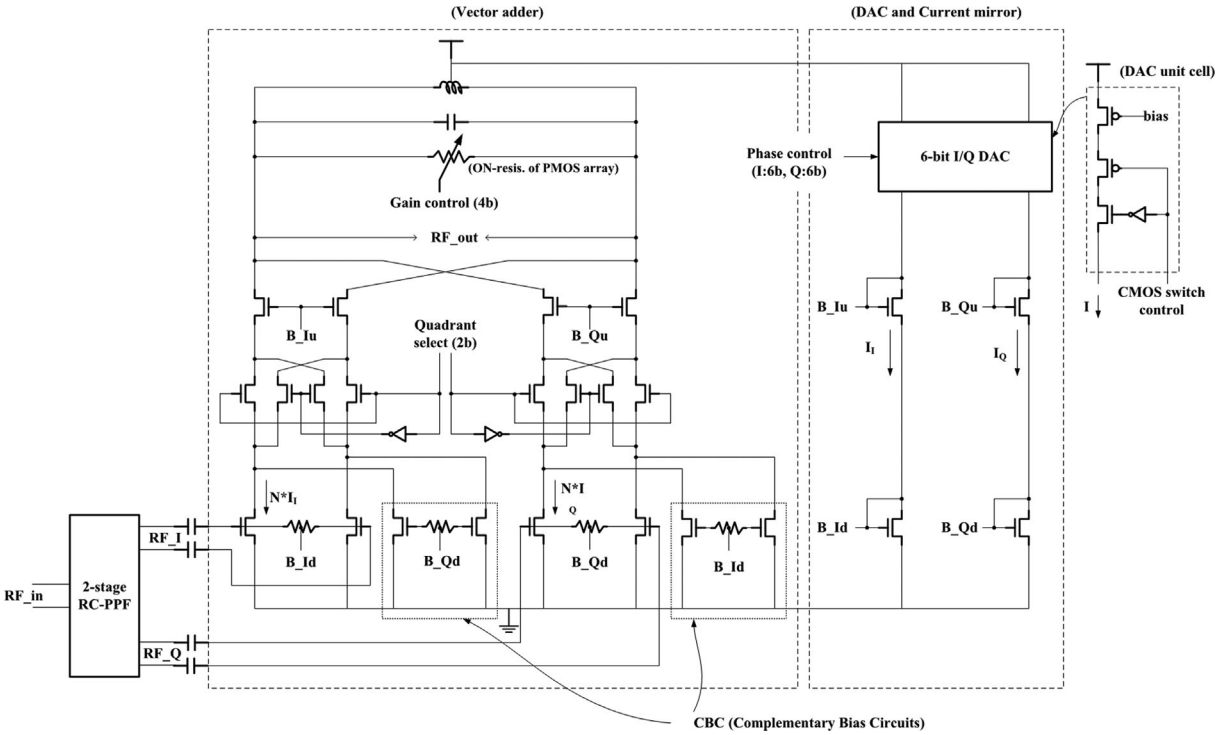

FIGURE 2 Proposed gain-controlled vector-sum phase shifter (GCPS) with complementary bias circuit (CBC) and equivalent R control.

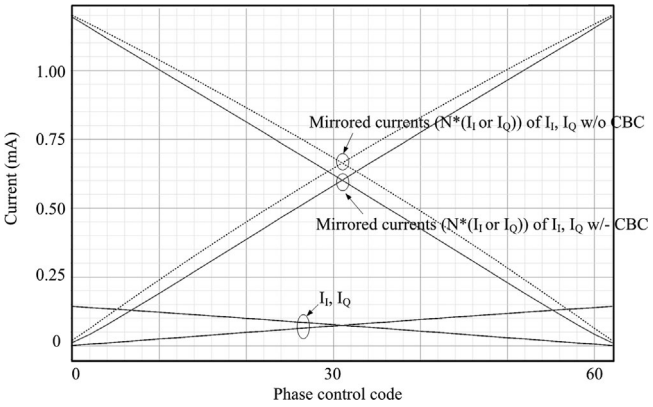

FIGURE 3 Simulation results of in-phase/quadrature (IQ) direct currents versus phase-control code of phase shifter with/without complementary bias circuit (CBC).

(CMOS)-type switch, the phase change of the vector adder will not remain linear and will exhibit an abrupt phase change at the quadrant change point throughout the quadrant selection control.

Figure 3 illustrates the simulated mirrored currents, N^*I_I, and N^*I_Q, of the vector adder and the reference I/Q currents, I_I, and I_Q, respectively, controlled by the IQ DACs. From the simulation results, the mirrored currents with CBC are highly linear, compared with the mirrored currents without CBC.

The gain control for the weighting factor of the phased array is realized using the equivalent resistance control of the resistance–inductance–capacitance (RLC) load of the proposed vector adder, as shown in Figure 2. The equivalent resistance control is performed by digitally switching the parallel p-channel metal–oxide semiconductor (PMOS) chips carrying the load using a 4-bit digital input. The total PMOS ON resistance changes the output gain, and around the resonance frequency of the load, the phase variation based on the gain control is minimized because only the real impedance value remains at the resonance frequency. Because a bandwidth with a RMS phase error over the gain control range may be increased by reducing the maximum equivalent resistance, we can optimize the maximum equivalent resistance.

Our combiner is realized using cascode amplifiers for wideband signal combinations, as shown in Figure 4. The input signal is converted to a current by the differential input pair in each channel and transferred to the cascode transistors of the 2×2 combiner. A short layout line from the transconductance (g_m) stage to the cascode transistors of the 2×2 combiner is applied for suitable current-mode operation, and the LC tank load provides the final four-channel combination.

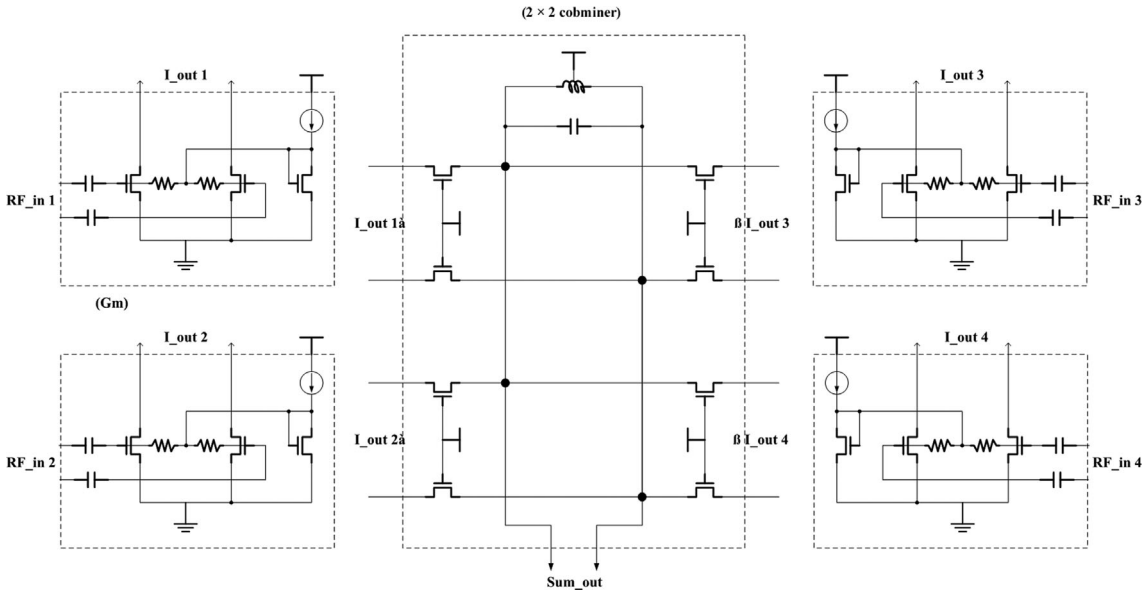

FIGURE 4 Current mode channel combiner of 2 × 2 phased-array radio frequency (RF) receiver.

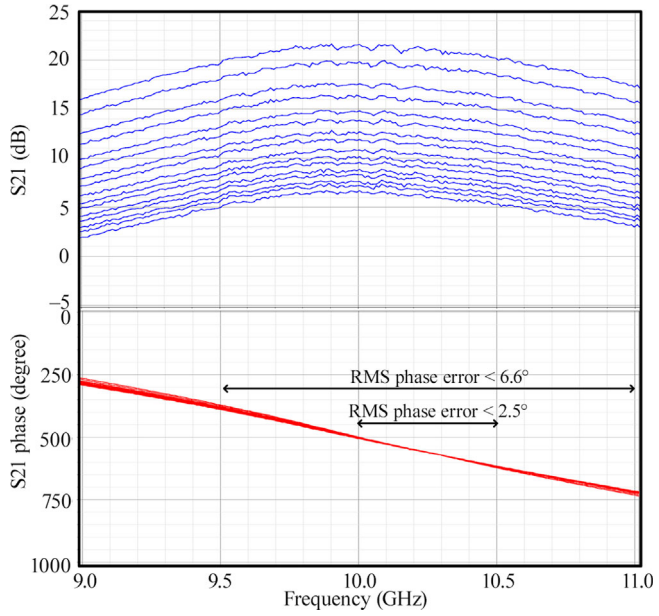

FIGURE 5 Measured gain-controlled S21 performances.

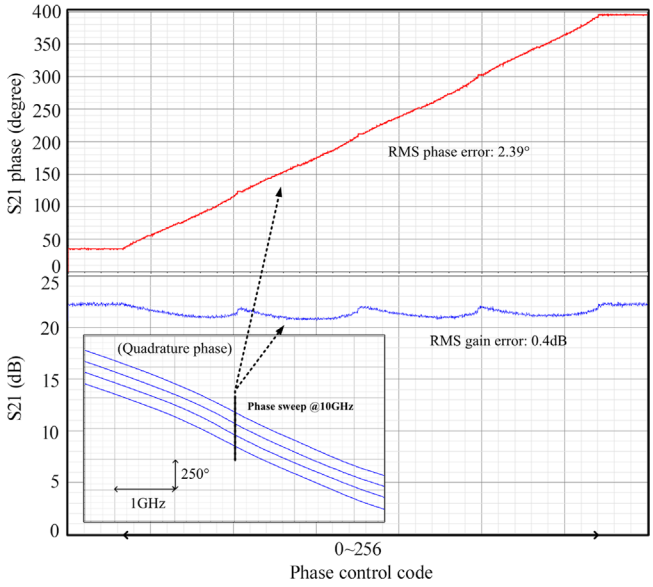

FIGURE 6 Measured S21 performances of 8-bit phase-sweep control.

3 | MEASUREMENT RESULTS

Figure 5 shows the gain-controlled S21 receiver measurement results for the phased-array weighting factor. The gain-control range was 15 dB (21 dB–6 dB), and the RMS phase error was <2.5 in the 0.5-GHz bandwidth and <6.6 in the 1.5-GHz bandwidth over the gain-control range. For kilometer-range radar applications, the bandwidth needed for a range resolution of a few meters is less than a few hundred megahertz. Therefore, our measured bandwidth is sufficient for such practical applications. Using the MATLAB simulator, the ideal maximum side-lobe level of the 8 × 8 phased array with element weighting factors of the Taylor window was found to be approximately −29.4 dB, and its required gain range was ∼25 dB (0 to −25 dB). With the measured 15-dB gain range of our chip, the side-lobe level was increased to approximately −24 dB in the MATLAB simulation.

Figure 6 shows the measured S21 performance according to the 8-bit phase-sweep control. The measured phase data were acquired by sweeping the phase control codes from 0° to 360°. The RMS phase and gain errors over the 360° phase sweep (total control code step = 256) at 10 GHz was about 2.39° and 0.4 dB, respectively. The RMS phase error can be reduced with 7- or 6-bit controls selectively extracted from the full eight bits.

Figure 7 shows our 8 × 8 phased-array receiver module and its measured beam patterns (three-dimensional boresight, azimuth, and two-dimensional elevation). The 8 × 8 vertically polarized patch antenna elements, consisting of 16 2 × 2 phased-array RF receivers (RX_2 × 2), and one 4-channel (4ch) RF receiver (RX_4ch), were used for the radar module. An 8 × 8 patch antenna was placed on the front side of the PCB module, and the 16 RX_2 × 2 chips, Wilkinson power combiners, and RX_4ch chip were placed on the rear side of the PCB module. The 4ch RF receiver, which has four RF channels on its front-end baseband analog blocks, is used for monopulse radar applications. For the 8 × 8 beam-pattern measurement, the 4ch RF receiver outputs are summed using an addition board, and the resulting signal is up-converted to an RF frequency. The beam pattern was measured with uniform gain in all the 8 × 8 array elements because it was difficult to perform measurements in the Taylor window gain setting owing to the exceedingly low gain of the antenna. The measured side-lobe levels were under −15 dB at all steering angles, and the steering accuracy was under 1°.

Table 1 summarizes the measured results and compares them with those of previously reported studies. The chip was integrated using 65-nm CMOS technology and packaged in a 36-pin quad-flat no-lead (QFN) assembly at low cost, and the total current consumption of the 2 × 2 phased-array RF receiver is approximately 140 mA at a 1.2-V supply voltage.

Figure 8 displays a microphotograph of the 2.43 × 1.78-mm^2 QFN-bonded die. To increase the isolation among channel inputs, the bonding wires of the RF signal input (RFin1–RFin4) were placed far away from the main assembly, perpendicular to one another, and ground wires are inserted among them.

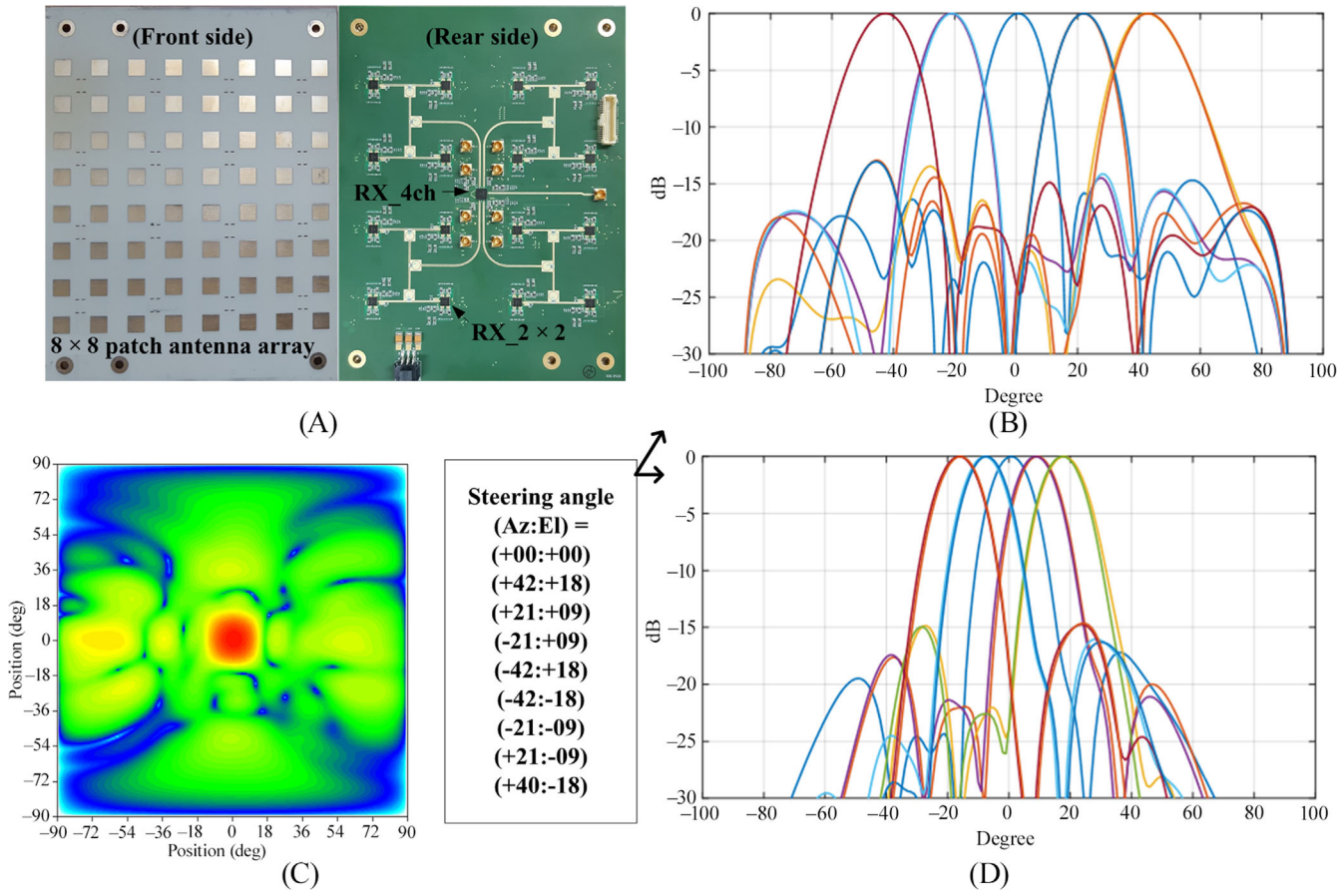

FIGURE 7 8 × 8 phased-array receiver module and measured beam patterns. (A) 8 × 8 receiver module, (B) boresight 3D beam pattern, (C) azimuth angle beam pattern, and (D) elevation angle beam pattern.

TABLE 1 Summary of the measured results and comparison.

	JSSC 2008 [1]	Radar Conf. 2015 [3]	RFIC 2017 [4]	ISSCC 2019 [14]	ESSCIRC 2022 [11]	This work
Technology	0.18-μm SiGe BiCMOS	13.0-nm CMOS	Jazz SBC18H3 SiGe BiCMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS
Supply voltage (V)	3.3	3.3	1.2/2.2	—	—	1.2
Frequency (GHz)	6–18	9–10	28–32	28 (3.8-GHz BW)	26.5–29.5	9.25–10.75
Number of channels	8	4	4	1	1	4
RX max. Gain (dB)	24.5	9	20	14.8	−13	21
NF (dB), single channel	4.2	—	4.6	4.58	—	5.7
Input P1dB @1-ch (dBm)	IIP3 = −33	—	−22	—	9	−27 (@HG)
Phase control bit width (bit)	4	6	6	8	4	8
Gain control range for weighting (dB)	—	31	—	16	—	15
Power cons. (mW)	561/8-ch	2000/4-ch rx	520/4-ch rx	44/1-ch rx	—	168/4-ch
Area (mm^2), (w/- PAD)	5.39	11.4	11.75	0.67/1-ch RTX core	0.1	4.33
Package	—	—	Chip-scale	—	—	QFN

Abbreviation: CMOS, complementary metal–oxide semiconductor.

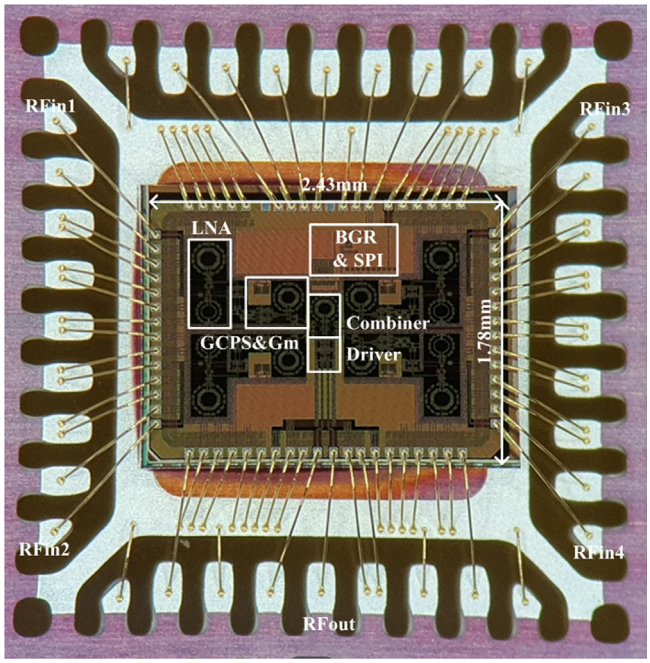

FIGURE 8 Quad-flat no-lead (QFN)-bonded die microphotograph of 2 × 2 phased-array radio frequency (RF) receiver.

4 | CONCLUSION

We proposed a 10-GHz band 2 × 2 phased-array RF receiver with an 8-bit linear phase control and a 15-dB gain control range using 65-nm CMOS technology. An 8 × 8 phased-array receiver module was successfully implemented using 16 2 × 2 phased-array RF receiver integrated circuits. Using a novel complementary bias technique in a phase-shifting core circuit and equivalent resistance control in an RLC load, our vector-sum GCPS structure increases the phase resolution and has weighting factor controllability. The 2 × 2 phased-array RF receiver chip exhibits a power gain of 21 dB per channel and a single-channel noise figure of 5.7 dB at the maximum gain. The measured results of the chip show 8-bit phase states with a 2.39° RMS phase error and 0.4-dB RMS gain error. Moreover, it has a 15-dB gain-control range with a 2.5° RMS phase error over the 10- to 10.5-GHz band. The chip consumes 140 mA, and its size is 2.43 × 1.78 mm^2, including the pad frame.

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CONFLICT OF INTEREST STATEMENT

The authors declare that there are no conflicts of interest.

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Bontae Koo received his MS degrees in electrical engineering from Korea University, Seoul, Republic of Korea, in 1991. In 1991, he was with the System Semiconductor Division, Hyundai Electronics Company, Icheon, Republic of Korea, where he was involved in the chip design of video codec and DVB modem. From 1993 to 1995, he was with HEA, San Jose, CA, USA, where he was responsible for the design of MPEG2 video codec chip. From 1996 to 1997, he was with TVCOM, San Diego, CA, USA, developing the design of DVB modem chip. In 1998, he joined the Dongbu Electronics, as a team leader with the system semiconductor Lab, and he focused on the methodology of semiconductor chip design. In 1999, he joined Application SoC team, Electronics and Telecommunications Research Institute, Daejeon, Republic of Korea, where he was a team leader, and his research activities include the chip design of MPEG4 video, T-DMB receiver, LTE femtocell modem, and DSP processor. In 2016, he joined RF research group in ETRI, where he is currently a project leader. His research activities focused on millimeter-wave AI radars.

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