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Stacking-Enabled NPN Heterostructures with GaN Collectors for Bipolar Power Devices

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Abstract

Npn heterostructures with GaN collectors were fabricated using nanomembrane (NM) stacking. N- and p-Si NMs were transfer-printed onto the n-GaN substrates, resulting in the formation of vertical n-Si/p-Si/n-GaN heterostructures. Electrical measurements of Si/Si and Si/GaN pn heterostructures exhibited rectifying properties, indicating that the formation of bipolar junctions was feasible through NM stacking. The energy band diagram of stacking-enabled npn heterostructure was analyzed to explain the rectifying behaviors of base-emitter and collector-base junctions, as well as to suggest potential applications for bipolar junction transistors with a GaN subcollector.

Key words : Heterostructures, Stacking, GaN, Si nanomembranes, Bipolar junction devices

Ⅰ. Introduction

The necessity for the development of high-speed and high-power devices has increased over the decades due to the demand for power electronics with improved operation frequency and power efficiency in electric vehicles, satellite communication, and power transmission [1]-[4]. Enhanced capabilities in breakdown field, power density, current, and unilateral gains are crucial aspects of advancements in bipolar power devices. Due to its wide bandgap, low on-resistance, high critical breakdown field, and higher carrier mobility and saturation velocity, GaN is used in power devices for high-power switching and operation frequency (Table 1) [5]. Compared to Si and SiC, GaN's electronic parameters are better suited for high-power and speed applications with low power loss. The 11.2 dBm power and 59.5 MHz speed were reported from the operation of SiC-based bipolar junction transistor (BJT) [6]. Based on the figure of merits in Table 1, the enhanced power and speed are expected from GaN-based devices.

Stacking through semiconductor nanomembrane (NM) transfer-printing onto heterogeneous materials enables the formation of heterostructures comprised of different doping types and lattice constants, leading to the construction of desired energy structures for power device applications [7]-[12]. The NM stacking technique enables lattice-mismatched semiconductors to form heterostructures with merits of both materials that can be applied for the fabrication of heterostructure devices.

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In this work, Si/GaN npn heterostructures were formed by NM junction stacking for the application of bipolar power devices. The electrical characteristics of the stacking-enabled diodes were demonstrated to show a feasible formation of bipolar structures composed of semiconductor materials with complementary merits. Improved switching speed and power density are expected from the stacking-enabled Si/GaN heterostructure devices.

Table 1. Materials parameters.

	Si	SiC	GaN
Bandgap (eV)	1.12	3.26	3.40
Breakdown field (MV/cm)	0.3	3.0	3.3
Electron mobility (cm^2/Vs)	1500	1000	2000
Saturation velocity (cm/s)	1×10^7	2×10^7	2.5×10^7
Dielectric constant	11.9	10	8.9
Johnson's figure of merit	1	400	760
Baliga's figure of merit	1	11	39

II. Results and discussion

2.1. Experimental

A Si/Si/GaN npn heterostructure was formed by NM stacking (Fig. 1) [13]. The p-Si-on-insulator (SOI) wafer (p-Si/SiO_2 = 100/1000 nm) with a boron doping concentration of 1×10^{19} cm^{-3} was patterned using photolithography and inductively-coupled plasma reactive-ion etching (ICP-RIE) to create NM formation with 5×5 μm^2 etching holes (Fig. 1i). An undercut of the p-SOI was performed in a 49% HF solution (Fig. 1ii). The undercut Si NM was picked up from the original substrate using an elastomeric polydimethylsiloxane stamp and transfer-printed onto the n-GaN wafer, followed by junction bonding (Fig. 1iii). The GaN subcollector was grown by metal-organic chemical vapor deposition with Si doping concentrations of 1×10^{18} cm^{-3} and 1×10^{19} cm^{-3} for the top and bottom layers, respectively. The as-grown GaN epi-wafer underwent RCA cleaning procedure. The 200 nm n-Si NM from the n-SOI wafer, with phosphorus doping concentrations of 1×10^{19} cm^{-3} and 1×10^{18} cm^{-3} for the top and bottom layers, was laminated onto the junction-bonded Si/GaN (Fig. 1iv), resulting in the stacked Si/Si/GaN npn heterostructures, followed by junction annealing (Fig. 1v). ICP-RIE was applied to the photoresist mask to shape the emitter and base mesas individually (Fig. 1vi). Ti/Au, Ni/Au, and Ti/Al/Ti/Au were deposited for the ohmic contacts of the emitter, base, and collector, respectively (Fig. 1vii). The functionality of the npn heterostructure device was equivalent to that of an npn BJT (Figs. 1viii and 1ix).

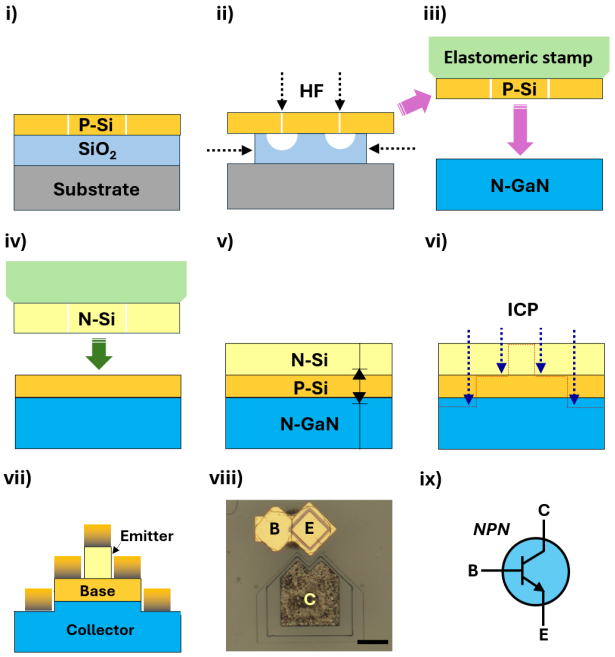

Fig. 1. Process steps for the formation of Si/Si/GaN npn heterostructures by junction stacking: i) Nanomembrane (NM) patterning on p-silicon-on-insulator (SOI) wafer, ii) undercut of SOI in HF solution, iii) transfer-printing of p-Si NM onto n-GaN collector using an elastomeric stamp, iv) transfer-printing of n-Si NM onto the Si/GaN heterostructure, v) junction-bonding of the npn heterostructure, vi) mesa formation using inductively-coupled plasma etcher, vii) formation of electrodes for the emitter (E), base (B), collector (C), separately, viii) optical image of the fabricated device, scale bar = 50 μm, and ix) symbol of NPN bipolar-junction transistor.

2.2. Electrical characteristics

The conduction properties of n-Si/p-Si and p-Si/n-GaN diodes from the stacked npn heterostructure were analyzed using a semiconductor parameter analyzer (Fig. 2). The measured I-V curves of Si/Si and Si/GaN diodes exhibited rectifying behavior, indicating that the stacked heterostructures possess bipolar polarity (Figs. 2a and 2b). The ideality factors for the Si/Si and Si/GaN diodes were 1.22 and 1.53, respectively, suggesting a low interface trap density at the stacked junction interface [14]. Since the Si/GaN diode is used for collector-base (CB) junction of npn bipolar devices, the relatively higher off current may affect the electron flow from base-emitter (BE) into CB junctions. UV/Ozone treatment can be applied to lower the reverse current by improving interface property during the junction bonding [7].

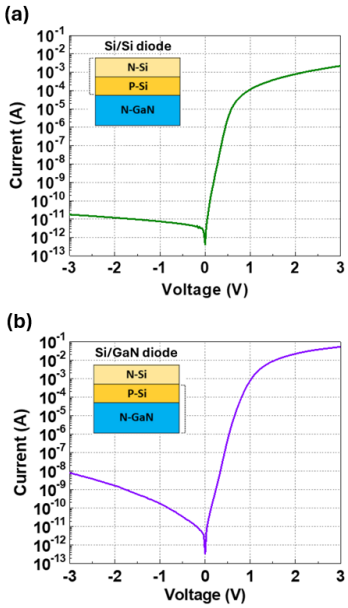

Fig. 2. Electrical characteristics of the npn heterostructures: (a) N-Si/p-Si and (b) p-Si/n-GaN heterostructures formed by junction stacking.

The energy band diagram of the Si/Si/GaN npn heterostructures was investigated to explain carrier injection for Si/Si and Si/GaN diodes (Fig. 3). Under forward bias, the energy band diagrams of both pn junctions shift to diagrams with low valence band offsets, facilitating effective electron injection (Fig. 3a). The electrical features of the stacked npn heterostructures with wide bandgap GaN subcollectors can be applied to the development of high-power npn BJTs. The switching of collector current in the npn heterostructure was analyzed based on the energy band diagram of the npn BJT in forward-active mode (Fig. 3b). Under forward BE (V_{BE}) and reverse collector-emitter (V_{CE}) biases, electrons move from the valence band of the emitter to the valence band of the collector, generating a collector current (I_C) that is amplified by the base current (I_B).

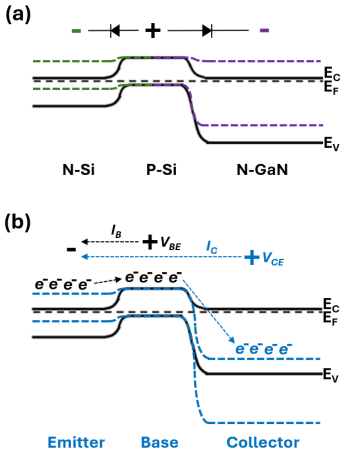

Fig. 3. Energy band alignment of the npn heterostructures: (a) Si/Si/GaN npn heterostructure under forward biases for Si/Si and Si/GaN pn diodes. Green and purple dashed lines indicate the energy band diagrams under forward biases for Si/Si and Si/GaN pn diodes, respectively. (b) Stacking-enabled Si/Si/GaN bipolar junction transistor in forward-active mode (V_{BE} 〉 0 V and V_{CE} 〉 0 V) showing electron injection from the emitter to the collector and inducing a collector current (I_C).

Ⅲ. Conclusion

In conclusion, Si/Si/GaN npn heterostructures were successfully fabricated through NM stacking. P-Si was transfer-printed onto a wide bandgap GaN subcollector to facilitate high-power and high-speed operation for device applications. N-Si was then laminated onto the Si/GaN heterostructure, resulting in an npn heterostructure suitable for manufacturing bipolar power devices. Electrical

measurements of Si/Si and Si/GaN pn diodes exhibited rectifying properties with low ideality factors, indicating the construction of bipolar structures with a low interface trap density. The energy band diagram was analyzed to understand carrier injection along the energy bands under bias conditions and support the development of bipolar power switching devices. The methodology for forming heterostructures through the NM stacking can be applied to the manufacturing of commercial electronic products by maximizing the transfer area while stabilizing the undercut procedure.

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