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Single-bit digital comparator circuit design using quantum-dot cellular automata nanotechnology

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Abstract

The large amount of secondary effects in complementary metal–oxide–semiconductor technology limits its application in the ultra-nanoscale region. Circuit designers explore a new technology for the ultra-nanoscale region, which is the quantum-dot cellular automata (QCA). Low-energy dissipation, high speed, and area efficiency are the key features of the QCA technology. This research proposes a novel, low-complexity, QCA-based one-bit digital comparator circuit for the ultra-nanoscale region. The performance of the proposed comparator circuit is presented in detail in this paper and compared with that of existing designs. The proposed QCA structure for the comparator circuit only consists of 19 QCA cells with two clock phases. QCA Designer-E and QCA Pro tools are applied to estimate the total energy dissipation. The proposed comparator saves 24.00% QCA cells, 25.00% cell area, 37.50% layout cost, and 78.11% energy dissipation compared with the best reported similar design.

KEYWORDS

comparator, energy dissipation, nanocomputation, QCA designer, QCA nanotechnology, QCA pro

1 | INTRODUCTION

Area-efficient circuit design is a fundamental objective of very-large-scale integration (VLSI) designers to develop small-size integrated circuits (ICs). Working-technology nodes are continuously being scaled down to obtain small-size electronic gadgets. Area-efficient circuit design is a challenging task in the commonly used complementary metal–oxide–semiconductor (CMOS) technology because of the limitation of materials [1]. Therefore, exploration of different technologies is needed in the VLSI domain to enhance this field, especially in the ultra-nanoscale region. Quantum-dot cellular automata (QCA) nanotechnology is an effective methodology and possibly the best replacement for CMOS technology. It offers many advantages such as area efficiency, high speed, low-power dissipation, and scalability in the ultra-nanoscale region compared with the CMOS technology [2, 3]. The operation of QCA-based circuits does not require a transistor; thus, external voltage is not required. Therefore, the QCA technology has become popular and valuable in the current systems.

The present work proposes an area-efficient digital comparator circuit. The proposed comparator uses fewer QCA cells and clock phases than the existing similar designs. The energy dissipation of the proposed design is also investigated to improve energy efficiency.

The rest of this paper is organized as follows. The fundamentals of the QCA nanotechnology, digital comparator circuit, and existing related works are presented in Section 2. The proposed QCA-based comparator circuit is detailed in Section 3. Section 4 presents the simulation analysis and comparison evaluation. The conclusion of this study is provided in Section 5.

2 | BACKGROUND

The fundamental of the QCA nanotechnology starts with the QCA cell. Four quantum dots exist in a QCA cell in which two electrons stay in the opposite corners due to a Columbic repulsion force. The positions of these two electrons in the cell affect the logic formation for digital applications. The specific location of the electron pair in the cell generates a unique polarization value. Hence, polarization values of +1 and −1 in a cell are possible, which create both true and false logic, respectively [4–6]. The Boolean logic representation of the QCA cell is shown in Figure 1.

QCA wire is an important element in QCA circuits. The QCA wire causes movement of data in the QCA circuit via cell-to-cell interactions [7,8]. Figure 2 shows a QCA wire that uses different clock phases. The data in the QCA wires move in a specific manner. The data flow from Phase 0 to Phase 1, Phase 1 to Phase 2, Phase 2 to Phase 3, Phase 3 to Phase 0, and so on by following the same path in the QCA wire.

Sometimes, crossing the QCA wires is required in complex QCA designs. Therefore, various methodologies such as planar and multilayer are adopted for the QCA designs to cross and pass the logic. The QCA cell contains two types of cells based on the quantum-dot locations. The QCA cell is further classified as regular or 90° and rotated or 45° cells. Therefore, two methods are available for the planar crossing of the wires. The first planar method is the combination of regular and rotated cells at the crossing point. The second planar method is based on the QCA-clock phases, which is also known as logical crossover. The other crossing methodology is a multilayer process in which a minimum of three layers are used for effective crossing of the wires [9–11].

Another important element in the QCA circuits is the clocking system. It is a prime component for controlling the data movement hence performs primary functions in the QCA designs. The overall operation of the QCA-based designs completely depends on the QCA clocking system. Switch, hold, release, and relax are the terminologies of the four clock phases in the clocking system [12–14]. The consecutive clock phases have 90° phase angles. Zone 0, Zone 1, Zone 2, and Zone 3 are the zones in the clocking system, as shown in Figure 3.

Any required application is first converted into the form of Boolean expressions so that it can be easily implemented using elementary logic gates. The logic gates generate the switching operations to manage the data flow. Therefore, elementary logic gates are first designed using QCA cells so that a complex circuit can be implemented using these elementary cells. The elementary logic gates are NOT, OR, and AND. The NOT, OR, and AND gates are sufficient for the required operations to develop any Boolean expression. The design of the QCA circuits is based on the specific arrangements of the QCA cells. Majority gate (MG) represents the QCA layout, which can be used for the creation of OR and AND logic gates [15–17]. The elementary logic gates in the QCA nanotechnology are shown in Figure 4.

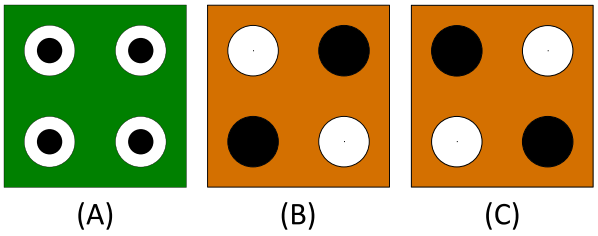

FIGURE 1 Cell illustration of (A) unpolarized and (B) polarized logic 1. (C) Polarized logic 0 [4–6]

FIGURE 2 QCA-based wire using different clock phases [7,8]

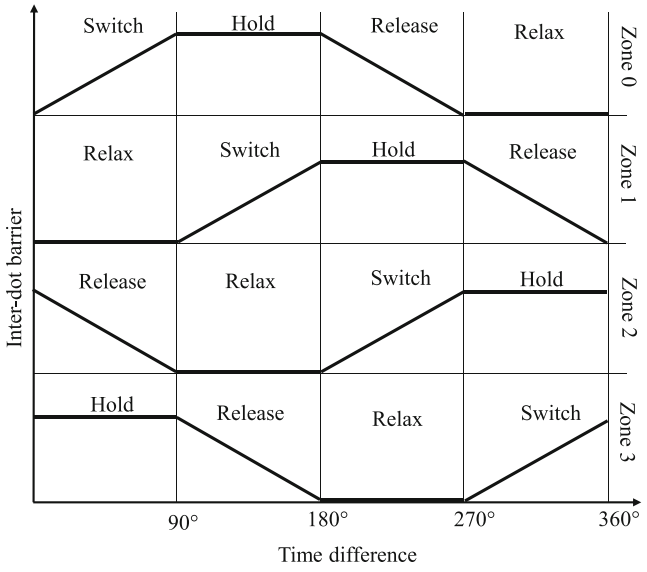

FIGURE 3 Clocking system [12–14].

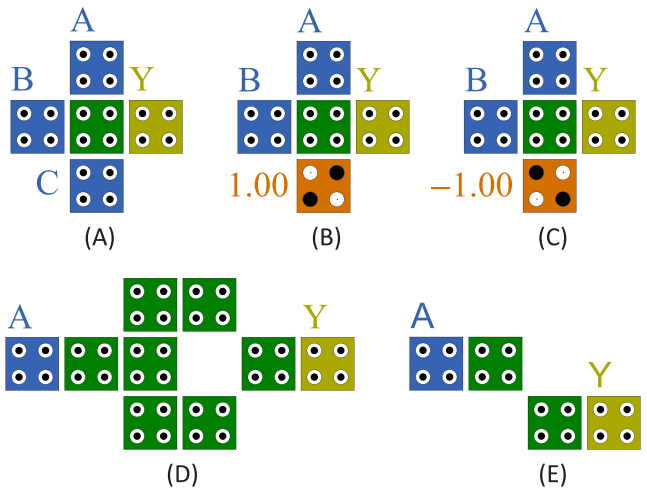

FIGURE 4 Elementary logic gates. (A) MG. (B) OR. (C) AND. (D) NOT. (E) Corner inverter [15–17]

Figure 4A shows the relationship between the inputs and output of the MG, as expressed by (1).

$$\mathrm{MG(A,\ B,\ C)} = \mathrm{Y(A,\ B,\ C)} = \mathrm{AB} + \mathrm{BC} + \mathrm{CA}. \quad (1)$$

Equation (1) shows that OR and AND logic can be created by fixing one input at Logic 1 and Logic 0, respectively.

Comparison is a key operation in many applications, including microcontrollers. Comparison is performed on two numbers. Many researchers have proposed digital comparators using the QCA nanotechnology. This section briefly presents the existing comparators. The number of used QCA cells and applied clock phases are prime factors that determine the overall performance of QCA-based circuits. Hence, previous comparator designs are presented based on these two factors.

Different nanostructures that use the QCA nanotechnology for XNOR logic have been developed [18]. The best developed XNOR logic based on the minimum number of QCA cells has been applied to develop a digital comparator. A total of 42 cells and three clock phases were utilized for the comparator layout. A novel nanostructure for the digital comparator was proposed using 31 cells and three clock phases [19]. The basis of the design depended on the inverter and MGs. A novel XOR gate that used the QCA nanotechnology was investigated in Safaiezadeh and others [20]. The investigated XOR gate was used for the design of the different digital comparator circuits. The optimized comparator circuit consisted of 25 QCA cells and three clock phases. A comparator circuit that contained a XOR gate, MG, and inverters was developed in Wang and Xie [21]. The developed comparator circuit had a single layer and used 47 QCA cells and three clock phases. Novel nanostructures for a XNOR gate were proposed as a building block for a digital comparator circuit in Majeed and others [22]. A minimum of 33 QCA cells and three clock phases were utilized to build the comparator logic.

A multilayer-based digital comparator circuit with 79 QCA cells and four clock phases was developed in Hayati and Razaei [23]. A comparator circuit that used XOR gate, MGs, and inverters was investigated in Shiri and others [24]. The investigated coplanar digital comparator circuit contained 38 QCA cells and two clock phases. Two QCA cells were translated from their original positions. Two single-layer digital comparators were proposed in Pal and others [25]. The best comparator based on the minimum number of QCA cells contained 37 cells and three clock phases. New comparator architecture with 29 QCA cells and four clock phases was presented in Mokhtarii and Rezai [26]. A single-layer digital comparator that used 44 QCA cells and four clock phases was reported in Khan and Arya [27]. A multilayer digital comparator circuit was investigated using the developed 2:1 multiplexer circuit [28]. The comparator circuit consisted of three different layers and was designed using 111 QCA cells and seven clock phases.

3 | PROPOSED DESIGN

Comparator is a module where two numbers are compared. It is a combinational logic circuit and widely used in the core of microprocessor units. It has two inputs (A and B) and three outputs [A less than B (A_L_B), A equal to B (A_E_B), and A greater than B (A_G_B)]. The comparator outputs show the comparative relationship of the numbers. Comparison of the input numbers is performed for the less than (L), equal (E), and greater than (G) operations, as shown in Figure 5.

Three possibilities can occur in case of a two-number comparison. If the A_L_B condition is fulfilled, then the A_L_B output will be at logic high, whereas the A_E_B and A_G_B outputs will be at logic low. Similarly, in the A_E_B and A_G_B operations, the corresponding output will be at logic high. Therefore, one output will be at

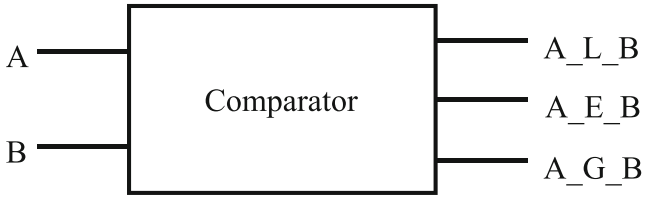

FIGURE 5 Comparator circuit representation

logic high while the other outputs will be at logic low at any given time. The truth table for the digital comparator circuit is listed in Table 1.

Two combinations of the inputs are possible where A_E_B is at logic high. The A_L_B and A_G_B outputs only have a single logic-high value for the total input combinations. The Boolean functions for the outputs are expressed in (2)–(4).

$$\mathrm{A\_L\_B} = \overline{\mathrm{A}}\mathrm{B}, \tag{2}$$

$$\mathrm{A\_G\_B} = \mathrm{A}\overline{\mathrm{B}}, \tag{3}$$

$$\begin{aligned}\mathrm{A\_E\_B} &= \left(\mathrm{AB} + \overline{\mathrm{A}}\,\overline{\mathrm{B}}\right) = \overline{\left(\overline{\mathrm{A}}\mathrm{B} + \mathrm{A}\overline{\mathrm{B}}\right)} \\ &= \overline{\left(\overline{\mathrm{A}}\mathrm{B}\right)} \cdot \overline{\left(\mathrm{A}\overline{\mathrm{B}}\right)} = \overline{(\mathrm{A\_L\_B})} \cdot \overline{(\mathrm{A\_G\_B})}.\end{aligned} \tag{4}$$

A digital comparator circuit can be designed using NOT, AND, and XNOR operations, as expressed in (2)–(4). Equation (4) expresses the NOR logic of the A_L_B and A_G_B outputs to obtain the XNOR logic. Here, the NOR logic is generated with the help of the NOT and AND logic, as provided in (4). Hence, the proposed comparator circuit is designed using three AND and four NOT logic. A schematic view of the proposed comparator circuit is shown in Figure 6.

The schematic view shown in Figure 6 serves as the basis for the proposed digital comparator circuit. The proposed circuit is implemented in such a manner that a minimum number of QCA cells and clock phases are required. The XNOR logic is implemented using the inverted input AND logic. The proposed QCA-based comparator circuit is shown in Figure 7. The proposed layout is verified using the QCA Designer-E tool for a bistable

TABLE 1 Truth table for the digital comparator circuit

A	B	A_L_B	A_E_B	A_G_B
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

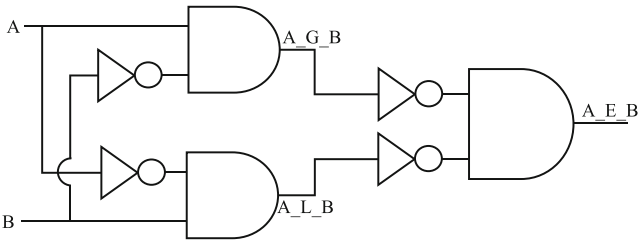

FIGURE 6 Schematic view of the proposed comparator circuit

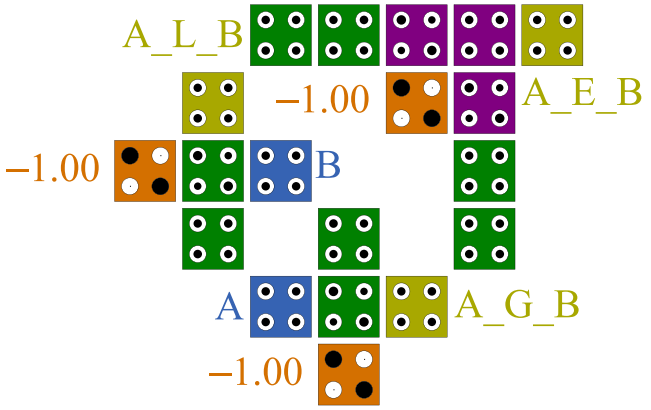

FIGURE 7 Proposed QCA-based comparator circuit

approximation engine [29]. The assumed cell size is 18 nm × 18 nm. The design is constructed using 19 QCA cells and two clock phases only.

Three MGs for the AND logic are utilized for the comparator circuit. Fixed polarization −1 for MG shows the AND operation. Here, one AND operation is needed for the A_L_B output, one AND operation for the A_G_B output, and one AND operation for the A_E_B output. The A_L_B and A_G_B outputs are generated in the first clock phase, whereas the A_E_B output is achieved in the second clock phase. Thus, the clock latency or delay in the layout is 0.50. The required cell area is $19 \times 18 \times 18 = 6156\ \mathrm{nm}^2$, and the total covered layout area is $6 \times 7 \times 18 \times 18 = 13\,608\ \mathrm{nm}^2$. No type of crossing of the wires is necessary in the proposed comparator, which enhances the simplicity and reliability of the circuit. The simulation results of the proposed comparator circuit are shown in Figure 8. The output results shown in Figure 8 can be easily verified with the help of Table 1.

The proposed comparator circuit is analyzed for fault tolerance due to missing cell. The missing-cell defect is investigated by sequentially eliminating the cells except the input, output, and fixed polarized cells. Faulty bits are observed to determine a cycle. Figure 9 shows the numbered cells of the proposed digital comparator, which are sequentially removed.

The correct output sequences are 0100 for A_L_B, 1001 for A_E_B, and 0010 for A_G_B, as listed in Table 1. Hence, faults are observed if any bit in the sequence deviates. Table 2 lists the fault tolerance due to a missing-cell defect.

Table 2 indicates that different faults are observed in the output sequences. Total fault represents the summation of faults in the three outputs. The outputs contain 12 bits in a particular missing cell. Thus, the overall fault percentage due to a missing cell is 22/132 = 16.67%. Hence, the fault-tolerant capability of the proposed digital comparator is 100% – 16.67% = 83.33%.

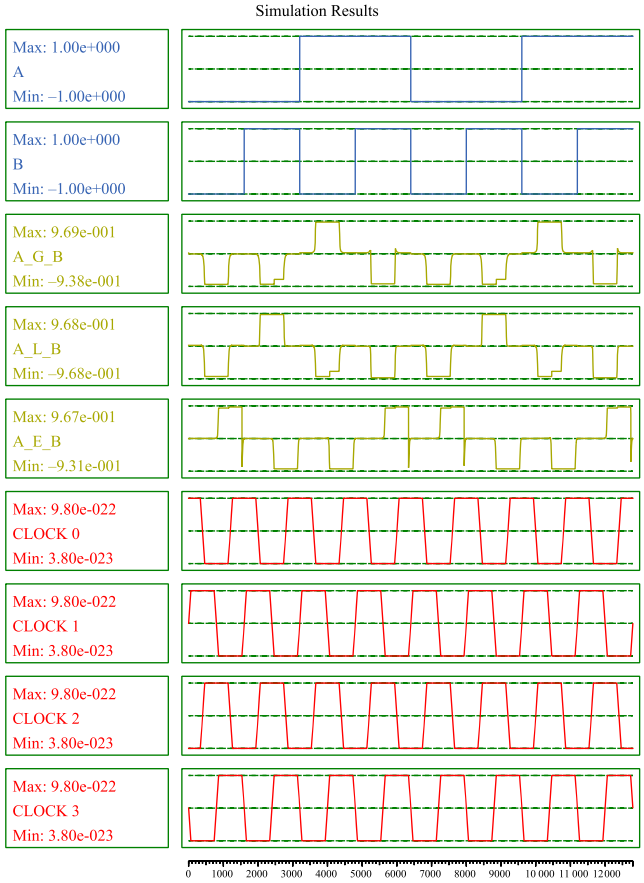

FIGURE 8 Simulation results of the proposed comparator circuit.

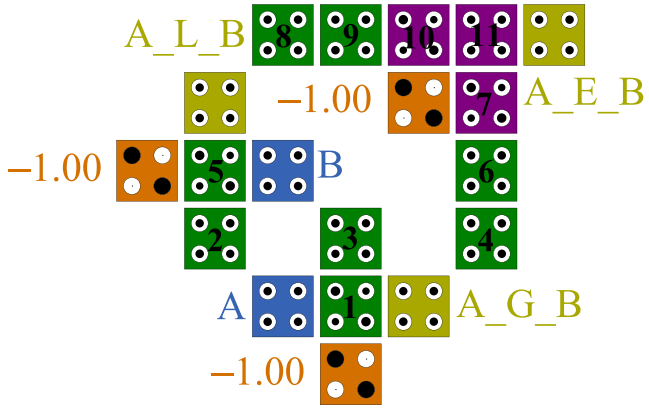

FIGURE 9 Numbered cells for the fault tolerance analysis

4 | COMPARISON ANALYSIS

This section explains the importance of the proposed comparator circuit compared with existing comparator circuits that use the QCA nanotechnology. The proposed circuit is simulated and evaluated using the QCA Designer-E tool for the default values of the bistable approximation engine [29]. Figure 10 shows the screenshot of the default values used in the engine.

The simulation engine runs for 12 800 samples with a 0.001 convergence tolerance. The considered radius of effect is 65 nm with a 12.90 relative permittivity. The value of the high clock is 9.80e−12, whereas that of the low clock low is 3.80e−23 with a zero clock shift. The clock amplitude factor is two. The layer separation is 11.50, and the maximum number of iterations per sample is 100.

TABLE 2 Fault-tolerant analysis for a missing-cell defect

Cell	Output			Total fault
	A_L_B	A_E_B	A_G_B	
1	0100	1011	0111	3
2	0000	1101	0010	2
3	0100	1000	0011	2
4	0100	0000	0010	2
5	1010	1101	0010	4
6	0100	0000	0010	2
7	0100	1011	0010	1
8	0100	0000	0010	2
9	0100	0000	0010	2
10	0100	1001	0010	0
11	0100	1111	0010	2

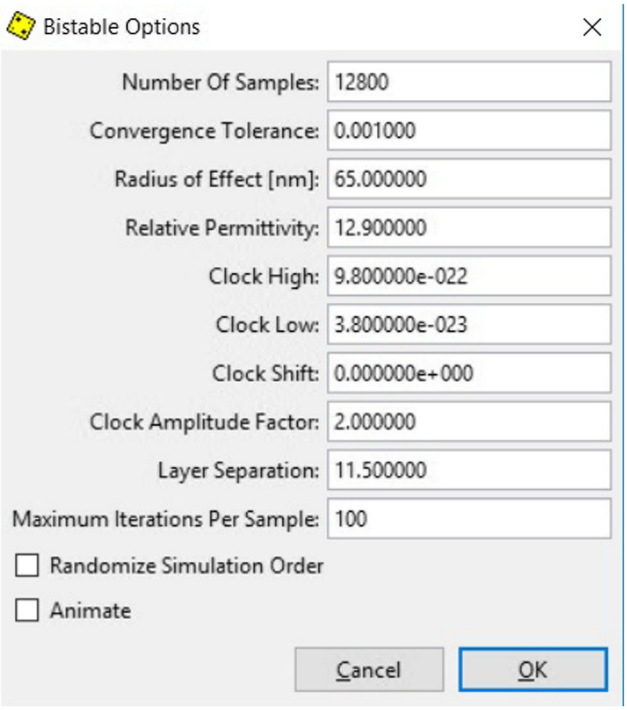

FIGURE 10 Bistable approximation engine values

The number of used QCA cell, clock phase, total cell area, total layout area, area utilization, layout cost, and nature of the layer are comparative parameters that are used in the performance evaluation of the different digital comparator circuits. Table 3 lists the importance of the proposed comparator circuit relative to existing similar designs.

The area-efficient circuit design is totally dependent on the QCA cells being used. Therefore, the focus of this research work is to use a minimum number of QCA cells. The QCA cell in comparative Table 3 shows the number of used QCA cells to design the comparator circuit. The proposed comparator circuit minimizes 24% of the QCA cells compared with the best reported similar design [20]. Hence, the proposed comparator circuit provides an area-efficient design. The used clock phase manages the high-speed operations. The number of clock phases represents a large delay and hence a lower speed. Minimum clock phases are desired for high-speed operations. The proposed comparator uses only two clock phases, hence providing a 0.50 clock delay. No previous work has reported a comparator circuit that used a single clock phase. One previous published research paper presented a comparator circuit that used two clock phases only, whereas other works required a minimum of three clock phases.

The total cell area is proportionally related to the employed QCA cells. It represents the product of the number of used QCA cells and dimension of a single cell. The proposed comparator consists of a minimum number of QCA cells, thus producing a smaller cell area than the other existing designs. The proposed design has a 25.00% smaller cell compared with the best reported available design [20]. Layout area represents the total captured area of the design. The maximum counts of horizontal and vertical cells are considered in the layout-area estimation. The counted horizontal and vertical cells are multiplied by the area of a single cell. The ratio of the cell area to the layout area represents the area utilization. Layout cost is a key evaluation parameter for investigating the design effectiveness. It can be considered as a figure of merit for QCA circuits, which manages the area–speed tradeoff. It represents the product of the layout area and square of the clock delay. The least value of the layout cost is mandatory for the best tradeoff. The proposed comparator circuit reduces the layout cost by 37.50% compared with the best reported layout cost of a similar design in the literature [24].

Energy efficiency of the design is another important characteristic of QCA circuits. A lower value of energy dissipation is an effective measurement of current portable systems. The proposed circuit is investigated for the energy-dissipation value using the QCA Designer-E and QCA Pro tools [29–32]. The bath for energy dissipation is measured in all coordinating systems of the design. A polarized cell pushes the neighboring cell to pass the QCA logic circuits after the application of the clocking system. We presume that no energy is lost in the environment during the logic pass. Therefore, the energy-dissipation error is negative. Energy-dissipation error represents the difference between the summation of the

TABLE 4 Total energy-dissipation estimation for a comparator circuit that uses the QCA Designer-E tool

Layout	Total energy dissipation (meV)
[20]	16.80
[27]	19.50
Proposed	19.00

TABLE 3 QCA-based digital comparator comparisons

Layout	QCA cell	Clock	Cell area (μm^2)	Layout area (μm^2)	% area utilization	Cost	Layer
[18]	42	0.75	0.014	0.05	28.00	0.028	Single
[19]	31	0.75	0.010	0.04	25.00	0.023	Single
[20]	25	0.75	0.008	0.02	40.00	0.011	Single
[21]	47	0.75	0.015	0.04	37.50	0.023	Single
[22]	33	0.75	0.011	0.04	27.50	0.023	Single
[23]	79	1.00	0.026	0.04	65.00	0.040	Multi
[24]	38	0.50	0.012	0.03	40.00	0.008	Single
[25]	37	0.75	0.012	0.06	20.00	0.034	Single
[26]	29	1.00	0.009	0.04	22.50	0.040	Single
[27]	44	1.00	0.014	0.04	35.00	0.040	Single
[28]	111	1.75	0.036	0.08	45.00	0.245	Multi
Proposed	19	0.50	0.006	0.02	30.00	0.005	Single

TABLE 5 Average energy-dissipation estimation of a comparator circuit that uses the QCA Pro tool

	Leakage (meV)			Switching (meV)			Total (meV)		
Layout	$0.5E_K$	$1.0E_K$	$1.5E_K$	$0.5E_K$	$1.0E_K$	$1.5E_K$	$0.5E_K$	$1.0E_K$	$1.5E_K$
[25]	23.91	75.38	136.29	124.69	106.58	89.43	148.6	181.96	225.72
[27]	-	-	-	-	-	-	71.87	44.78	-
Proposed	8.18	20.45	33.45	7.55	6.32	5.26	15.73	26.77	38.71

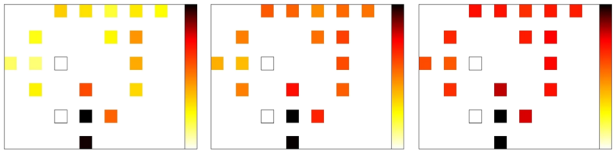

FIGURE 11 Power maps of the proposed comparator circuit at (A) 0.5 E_K, (B) 1.0 E_K, and (C) 1.5 E_K

environment and input-energy dissipation of the clock and the output-cell energy dissipation [33,34]. The coherence vector-simulation engine in the QCA Designer-E tool for the default values is applied to measure the energy dissipation [35]. Table 4 lists the total energy-dissipation (summation of the energy bath) estimation using the QCA Designer-E tool. Only two previous works have reported energy-dissipation estimation using the QCA Designer-E tool.

Another energy-dissipation tool for QCA circuits is QCA Pro. It performs an approximation process to compute the leakage and switching energy-dissipation values [31]. The QCA Pro tool computes the energy dissipation of the predefined three values of the Kink energy. Table 5 lists the energy-dissipation values for the different levels of Kink energy. Only two previous published research papers have reported energy-dissipation estimation using the QCA Pro tool. Hence, the proposed comparator is compared with the existing comparators. A previously published paper has reported the total energy dissipation at $0.5E_K$ and $1.0E_K$ energy levels, where E_K represents Kink energy level.

Table 5 shows that the proposed comparator is 78.11% energy efficient compared with the best reported work [27] at a 0.5-E_K level. Power maps of the proposed design are designed at 0.5, 1.0, and 1.5-E_K Kink energy levels and shown in Figure 11.

5 | CONCLUSION

CMOS technology will reach saturation in future ICs due to further scaling issues. QCA nanotechnology is an emerging design methodology with the capability of replacing the CMOS technology. Comparison is a key operation in the processing units of computers. This paper proposes a single-layer low-complexity QCA-based digital comparator circuit. The proposed comparator circuit is compared with existing similar designs based on the QCA cells, used clock, cell area, covered area, layout cost, and nature of the layer. The proposed comparator outperforms the existing comparators. Energy dissipation using the QCA Designer-E and QCA Pro tools is measured and compared with that of the available designs. Power maps are also presented for the proposed comparator circuit. The simulation analysis of the proposed comparator circuit demonstrates its importance in the ultra-nanoscale region. The proposed digital comparator is 83.33% fault tolerant. It reduces the number of cells by 24% and improves the layout cost by 37.50% compared with those of the best reported work.

CONFLICTS OF INTEREST

The author declares that there are no conflicts of interest.

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