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Low-clock-speed time-interleaved architecture for a polar delta–sigma modulator transmitter

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Abstract

The polar delta–sigma modulator (DSM) transmitter architecture exhibits good coding efficiency and can be used for software-defined radio applications. However, the necessity of high clock speed is one of the major drawbacks of using this transmitter architecture. This study proposes a low-complexity time-interleaved architecture for the polar DSM transmitter baseband part to reduce the clock speed requirement of the polar DSM transmitter using an upsampling technique. Simulations show that using the proposed four-branch time-interleaved polar DSM transmitter baseband part, the clock speed requirement of the transmitter is reduced by four times without degrading the signal-to-noise-and-distortion ratio.

KEYWORDS

delta–sigma modulator, long-term evolution, oversampling ratio, signal-to-noise-and-distortion ratio, software-defined radio

1 | INTRODUCTION

Power amplifier (PA) efficiency plays an important role in designing transmitter architectures. Modern wireless communication standards, for example, long-term evolution (LTE), are using signals with advanced modulation formats for the optimal utilization of bandwidth. These signals possess a high peak-to-average power ratio [1]. Therefore, a PA is forced to operate at power backoff to avoid distortion, and consequently, the PA efficiency decreases [2]. Moreover, these signals demonstrate a non-constant envelope nature and, thus, cannot drive switched-mode PAs (SMPAs).

Delta–sigma modulator (DSM) transmitter architecture can help solve the aforementioned problems. The DSM generates a constant envelope signal. Therefore, a PA can be operated using this signal without the need for power backoff. Moreover, this signal can be used to drive SMPAs [3–5]. Furthermore, the flexibility and reconfigurability of DSMs make them a good option for use in software-defined radio applications [6–11].

Several architectures have been proposed for the DSM transmitter. In previous works [9,12,13], two Cartesian DSMs are used for quantizing the quadrature components of the input signal (I and Q) to generate a constant envelope signal. The disadvantage of this architecture is the large amount of quantization noise generated by the DSM, which decreases the efficiency of the DSM transmitter. To solve this quantization noise problem, a polar DSM transmitter based on the envelope elimination and restoration architecture has been used in other works [14–17]. In this architecture, the envelope of the input signal is quantized by the DSM, and then, this signal is used to control the drain voltage of the SMPA. The main issue of this method is switching DC-supply current ON and OFF during high power generation. To solve this

issue, another polar DSM transmitter architecture has been proposed in other studies [18–20]. The envelope of the input signal is quantized by DSM using this architecture. Then, this quantized envelope signal is recombined with the input signal phase component, and the resulting signal drives the gate voltage of the SMPA. Therefore, the switching issue of the supply current can be solved using this architecture. However, the recombination of phase components with the quantized envelope causes the distribution of the quantization noise in the desired band and degrades the signal-to-noise-and-distortion ratio (SNDR). Therefore, this transmitter architecture requires a higher oversampling ratio (OSR) and consequently higher clock speed to possess the desired SNDR. However, the necessity of high clock speed is one of the main problems in using the polar DSM transmitter.

This study proposes a low-complexity time-interleaved architecture for the polar DSM transmitter baseband part to reduce the clock speed requirement of the polar DSM transmitter without degrading SNDR. Using this time-interleaved architecture with four parallel branches, the clock speed requirement of the polar DSM transmitter is reduced by four times while maintaining the SNDR.

The rest of the study is organized as follows: Section 2 describes the polar DSM transmitter architecture. Section 3 introduces a low-complexity time-interleaved architecture for the polar DSM transmitter baseband part to reduce the required clock speed of the polar DSM transmitter. Section 4 provides the simulation results of the proposed architecture. Section 5 concludes the study.

2 | POLAR DSM TRANSMITTER

The block diagram of the polar DSM transmitter is shown in Figure 1. In the transmitter baseband part, the envelope part of the input signal is quantized using the DSM. Then, this quantized envelope is recombined with the input signal phase component. The resulting signal exhibits a two-level envelope (0 and 1); therefore, this signal is suitable for driving SMPAs. The signal is up-converted to the desired frequency to drive the SMPA. Finally, a band-pass filter eliminates unwanted signal components, for example, quantization noise. In this polar DSM transmitter, which is based on a low-pass DSM, the frequency up-converting process is performed in the analog domain (unlike the previous parts that can be implemented in the digital domain). However, the benefit of this approach is the reduced requirements of the operating frequency. In another type of transmitters, which are based on band-pass DSMs, the frequency up-converting process is performed in the digital domain [21]; however, this method suffers from high operating frequency, which is hard to achieve in enhanced radio frequency (RF) applications with a carrier frequency in the gigahertz range [20].

Coding efficiency (CE) is a metric to study the DSM quantization noise effect on the DSM transmitter efficiency and can be expressed as follows [22,23]:

$$\mathrm{CE} = \frac{\mathrm{SignalPower}}{\mathrm{TotalPower}(\mathrm{SignalPower} + \mathrm{QuantizarionNoisePower})}. \quad (1)$$

The DSM transmitter efficiency is the product of CE and SMPA efficiencies [22–24]. As the efficiency of an ideal SMPA is theoretically 100% [2,3], the overall efficiency of the DSM transmitter is approximately equal to the CE efficiency.

As described before, in the polar DSM transmitter baseband part, quantization is not performed on the phase component of the input signal, and only the envelope of the input signal is quantized using the DSM.

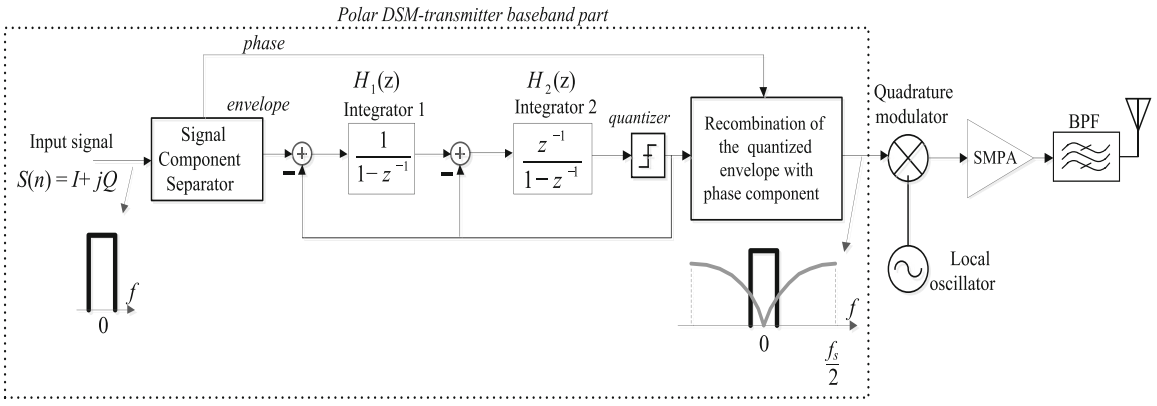

FIGURE 1 Polar delta–sigma modulator (DSM) transmitter

TABLE 1 Performance comparison between the polar DSM transmitter and Cartesian DSM transmitter baseband parts

Input signal	BW (MHz)	OSR	Transmitter topology	Phase quantization	CE (%)	SNDR (dB)
LTE	7.68	32	Polar	No	41.65	41.14
		16	Cartesian	Yes	9.65	41.17

Abbreviations: BW, bandwidth; CE, coding efficiency; DSM, delta–sigma modulator; LTE, long-term evolution; OSR, oversampling ratio; SNDR, signal-to-noise-and-distortion ratio.

However, in the Cartesian DSM transmitter baseband part (where the quantization is performed on the quadrature components of the input signal [I and Q]), the phase component of the input signal is quantized into four different phases ($\pi/4$, $3\pi/4$, $5\pi/4$, and $7\pi/4$) [9,12,22]. Therefore, the polar DSM transmitter baseband part generates lower quantization noise and, thus, higher CE compared with the Cartesian DSM transmitter baseband part.

However, as shown in Figure 1, in the polar DSM transmitter baseband part, the quantized envelope is recombined with the phase component of the input signal. This recombination is equal to the convolution of the quantized envelope and phase component spectra in the frequency domain and distributes the quantization noise in the desired band and degrades the SNDR. Therefore, the polar DSM transmitter baseband part requires higher OSR and consequently higher clock speed compared with the Cartesian DSM transmitter baseband part to achieve the same SNDR.

Table 1 compares the performance of the polar DSM transmitter and Cartesian DSM transmitter baseband parts based on the MATLAB simulation. This simulation has used a 7.68-MHz LTE signal as an input. The polar DSM transmitter baseband part has higher CE than the Cartesian DSM transmitter baseband part; however, it requires higher OSR to achieve the same SNDR (~41 dB). Therefore, the clock speed requirement of the polar DSM transmitter should be reduced for better performance.

3 | TIME-INTERLEAVED ARCHITECTURE FOR THE POLAR DSM TRANSMITTER BASEBAND PART

One of the parallel processing techniques that can be used to reduce the clock speed requirement of DSM is the time-interleaved DSM architecture. In Embrahimi and others and Khoini-poorfard and others [10,25], the polyphase multirate technique was used to design the time-interleaved DSM. As shown in Figure 2, the clock speed of polyphase equivalents in the polyphase multirate technique is M times lower than the original blocks, where M is the number of parallel branches in polyphase equivalent circuits. The polyphase equivalents of DSM integrators were obtained in Embrahimi and others and Khoini-poorfard and others [10,25] using the polyphase multirate technique to reduce the clock speed requirement of the DSM. Using the same technique for the integrators of the polar DSM transmitter baseband part, as shown in Figure 1, the time-interleaved equivalent of the polar DSM transmitter baseband part can be obtained. The block diagram of the polar DSM transmitter baseband part by replacing its integrators with their two-branch polyphase equivalents ($\overline{H}_1(z)$ and $\overline{H}_2(z)$) after simplification is shown in Figure 3. The clock speed of the blocks in this two-branch time-interleaved polar DSM transmitter baseband part is two times lower than the original polar DSM transmitter baseband part. Moreover, these polyphase equivalent blocks can be obtained and used to design the time-interleaved polar DSM transmitter baseband part with additional branches.

Despite the advantage of reducing clock speed requirement in this time-interleaved polar DSM transmitter baseband part, a large number of hardware blocks caused by the $M - 1$ cross-connections between parallel branches create an issue. The hardware growth of this time-interleaved polar DSM transmitter baseband part becomes proportional to M^2 by increasing the number of parallel branches (M).

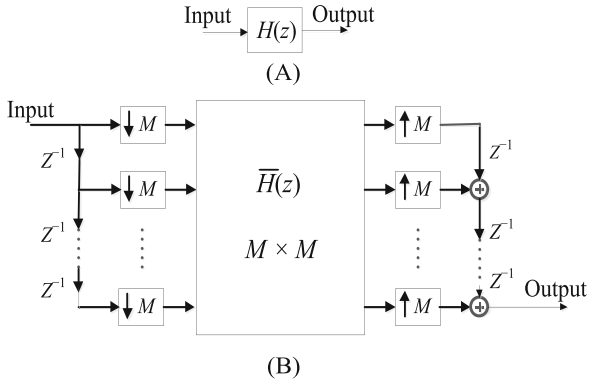

FIGURE 2 Polyphase multirate technique (A) original block $H(z)$. (B) Polyphase equivalent of $H(z)$ [10,25]

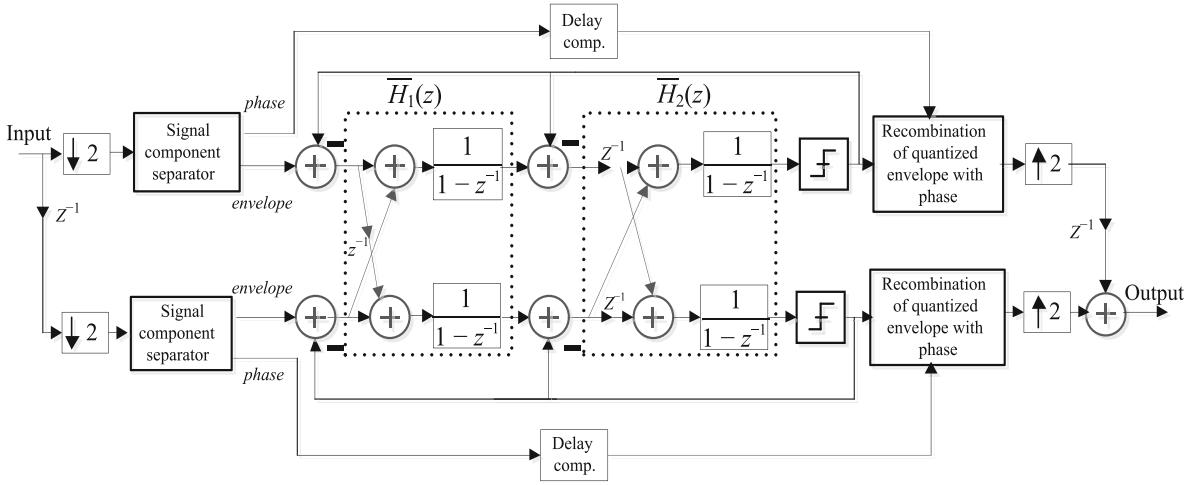

FIGURE 3 Two-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part based on the polyphase multirate parallel processing technique described in Embrahimi et al. and Khoini-poorfard et al. [10,25]

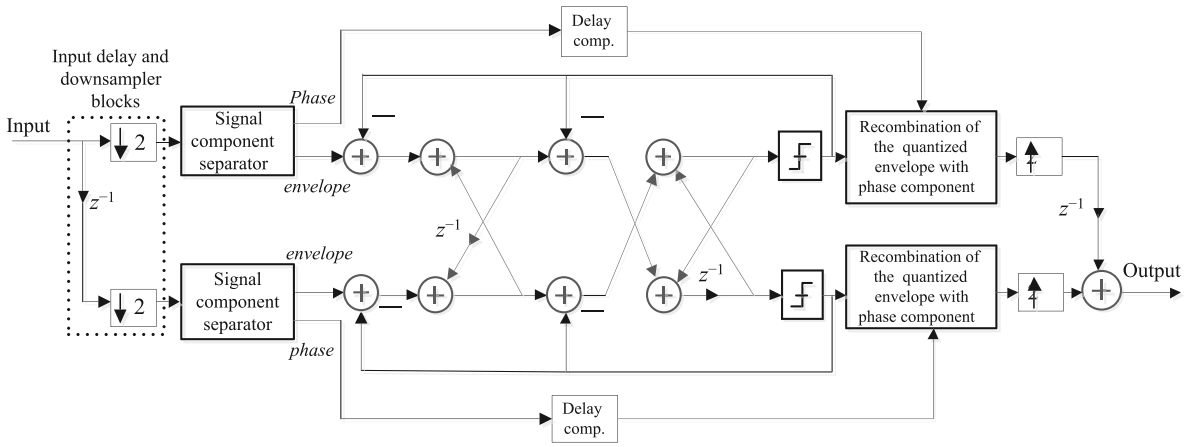

FIGURE 4 Two-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part based on the feedforward and feedback matrices and parallel processing technique described in Embrahimi et al. and Khoini-poorfard et al. [26,27]

In Kozak and others and Erfani Majd and others [26,27], this high hardware complexity problem is reduced by deriving the polyphase equivalent transfer functions of DSM integrators based on feedforward and feedback matrices.

$$\overline{H}(z) = \left(I - \overline{B}(z)\right)^{-1}\overline{A}(z), \tag{2}$$

where $\overline{A}(z)$ and $\overline{B}(z)$ are the feedforward and feedback matrices, respectively. This technique can be applied to the integrators of the polar DSM transmitter baseband part. The architecture of the time-interleaved polar DSM transmitter baseband part based on the parallel processing technique described in Kozak and others and Erfani Majd and others [26,27] is shown in Figure 4. This architecture does not include integrators. The integrators in this time-interleaved polar DSM transmitter baseband part are shaped by interconnections between branches with feedforward and feedback matrices. Therefore, the number of hardware blocks of this architecture reduces more compared with the time-interleaved polar DSM transmitter baseband part of Figure 3. The increase in the hardware blocks of this architecture is proportional to M.

We can further decrease the number of hardware blocks of the time-interleaved polar DSM transmitter baseband part of Figure 4 using an upsampling technique. As shown in Figure 4, the samples of the input signal (with the sampling rate of f_s) are distributed between the M branches (in this case $M = 2$) of the time-interleaved polar DSM transmitter baseband part using delay and downsampler blocks. Now, it is possible to use a single input signal (with the sampling rate of f_s/M) and apply it to the parallel branches. In this

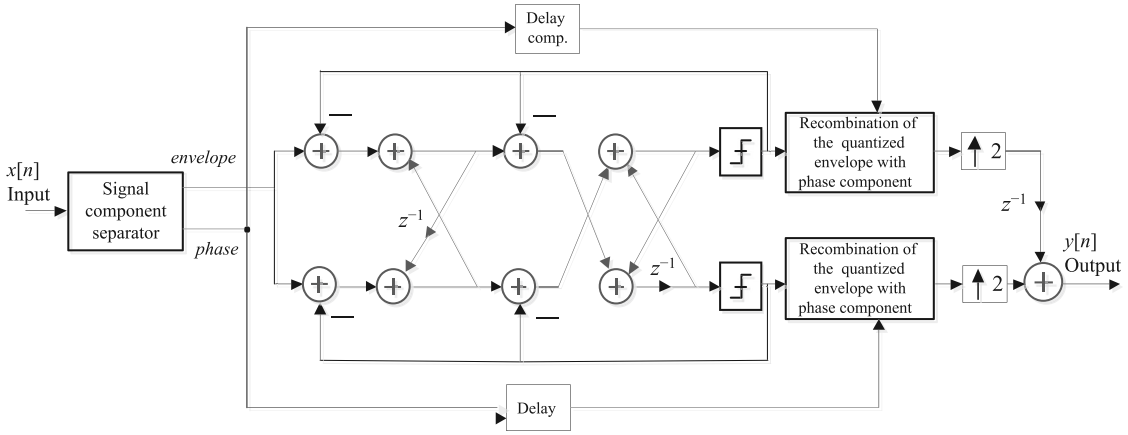

FIGURE 5 Proposed two-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part architecture

way, the input signal becomes equal for all the M branches, and its sampling rate reduces by M times. Therefore, in this case, there is no need for delay and downsampler blocks at the input of the time-interleaved polar DSM transmitter baseband part, and the input signal will be applied to all the branches with the lower sampling rate of f_s/M.

The proposed time-interleaved polar DSM transmitter baseband part with two parallel branches is shown in Figure 5. In this structure, the complexity of the time-interleaved polar DSM transmitter baseband part is reduced by one delay and two downsampler blocks compared with the structure shown in Figure 4. The number of blocks will further reduce in time-interleaved polar DSM transmitter baseband parts with additional parallel branches. For instance, in the four-branch architecture, the transmitter baseband part is reduced by three delays and four downsampler blocks compared with the time-interleaved architecture shown in Figure 4. For the M-branch time-interleaved polar DSM transmitter baseband part, the reduction rate is equal to M – 1 delay and M downsampler blocks. Additionally, as the single input signal is applied to all the M parallel branches, one signal component separator block is required, and therefore, the number of signal component separator blocks is reduced by M – 1 compared with the time-interleaved architecture illustrated in Figure 4.

In the proposed architecture, the upsampling process of the input signal from the sampling rate of f_s/M to f_s is performed by repeating input signal samples and applying them to all the M parallel branches. Therefore, the sampling rate of each branch is equal to f_s/M, and delay and downsampler blocks can be eliminated. The impulse response of the upsampling process is shown in Figure 6. It acts as a sample and holds impulse response ($h_{SH}[n]$). The equation of $h_{SH}[n]$ is as follows:

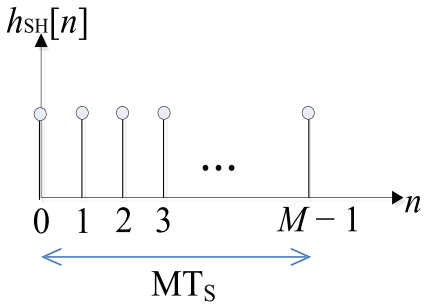

FIGURE 6 Impulse response of the upsampling process from the sampling rate of f_s/M to f_s by repeating input signal samples (sample and hold impulse responses)

$$h_{SH}[n] = \begin{cases} 1, & 0 \le n \le M-1 \\ 0, & \text{Otherwise} \end{cases}. \tag{3}$$

The upsampled signal can be described as

$$x_{up}[n] = \sum_k x[k] h_{SH}[n - kM], \tag{4}$$

where $x[n]$ is the transmitter baseband part input signal. Moreover, (4) can be expressed in the convolution form as follows:

$$x_{up}[n] = \left(\sum_k x[k]\, \delta[n - Mk] \right) * h_{SH}[n]. \tag{5}$$

The expanded form of input signal $x[n]$ is enclosed in parentheses. The equivalent system of the signal (indicated in parentheses) is defined as

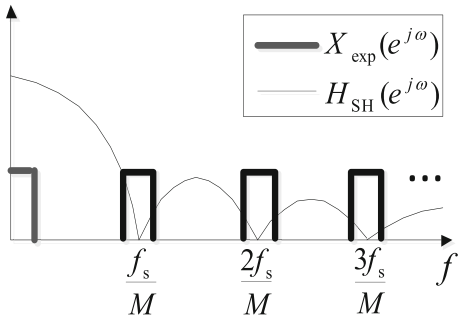

FIGURE 7 Suppression of the aliases caused by $X_{\exp}(e^{j\omega})$ with zero frequencies of $H_{SH}(e^{j\omega})$

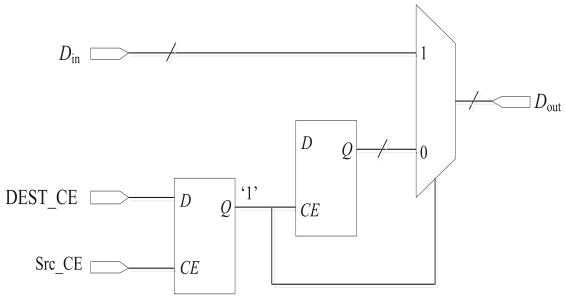

FIGURE 8 Hardware implementation of the zero-latency downsampler block

$$x[n]\ x_{\exp}[n] = \sum_k x[k]\delta[n-Mk]\Big), \tag{6}$$

where $x_{\exp}[n]$ is the expanded form of the input signal. The discrete time Fourier transform (DTFT) of (5) can be defined as follows.

$$X_{up}(e^{j\omega}) = X_{\exp}(e^{j\omega}).H_{SH}(e^{j\omega}). \tag{7}$$

As described before and expressed in (6), $x_{\exp}[n]$ is the expanded form of input signal $x[n]$. Therefore, the DTFT of $x_{\exp}[n]$ is equal to $X(e^{j\omega M})$. Therefore, $X_{\exp}(e^{j\omega})$ includes the repeated images of the DTFT-based input signal and causes aliases of the input signal occurring at frequencies n (f_s/M), $n = \pm 1, \pm 2, \ldots$. However, these aliases can be suppressed by the DTFT of $h_{SH}[n]$ $(H_{SH}(e^{j\omega}))$ in (7). The DTFT of rectangular signal $h_{SH}[n]$ can be derived as

$$H_{SH}(e^{j\omega}) = e^{-j\omega(M-1)/2}\frac{\sin(\omega M/2)}{\sin(\omega/2)}. \tag{8}$$

Therefore, (7) can be expressed as

$$X_{up}(e^{j\omega}) = X_{\exp}(e^{j\omega}).e^{-j\omega(M-1)/2}\frac{\sin(\omega M/2)}{\sin(\omega/2)}. \tag{9}$$

The magnitude form is expressed as

$$|X_{up}(e^{j\omega})| = |X_{\exp}(e^{j\omega})|.\left|\frac{\sin(\omega M/2)}{\sin(\omega/2)}\right|. \tag{10}$$

As expressed in (10), $H_{SH}(e^{j\omega})$ is the sinc function and its zero frequencies are at n (f_s/M), $n = \pm 1, \pm 2, \ldots$. Therefore, the frequencies of the aliases that are arising from $X_{\exp}(e^{j\omega})$ are matched with zero frequencies of $H_{SH}(e^{j\omega})$. Therefore, the aliases are suppressed by $H_{SH}(e^{j\omega})$ (Figure 7). Although, this suppression (unlike ideal low-pass filters) does not completely eliminate the aliases but maintains their magnitudes below the quantization noise level of the output signal. Therefore, they do not affect the SNDR of the proposed time-interleaved architecture. Therefore, this upsampling technique in the polar DSM transmitter baseband part can eliminate the use of input delay and downsampler blocks without degrading the signal quality and SNDR.

The proposed time-interleaved polar DSM transmitter baseband part mainly uses the upsampling technique by applying the same input signal (with M times lower sampling rate) to all the M parallel branches. Therefore, in this case (unlike the time-interleaved polar DSM transmitter baseband part based on techniques presented in Kozak and others and Erfani Majd and others [26,27]), there is no need for delay and downsampler blocks at the input. Each input delay block in the architecture based on Kozak and others and Erfani Majd and others [26,27] includes one register. If we consider the N-bit input signal, each input delay block is included in the N 1-bit register. Moreover, the architecture that is used to implement the downsampler block (architecture based on Kozak and others and Erfani Majd and others [26,27]) is shown in Figure 8. This is the zero-latency downsampler block and must be configured to sample the first value of the frame. The first sample in the input frame passes through the multiplexer (MUX) to the output port. A register samples this value during the first sample duration, and the MUX switches to the register output at the start of the second sample of the frame. The result is that the first sample in a frame is present on the output port for the entire frame duration. A single bit register adjusts the timing of the destination clock enable signal (DEST_CE), so that it is asserted at the initiation of the sample period instead of the end period. As shown in Figure 8, each downsampler block comprises one N-bit MUX (which includes N 1-bit MUXs) and two registers. Therefore,

TABLE 2 Simulation results of the proposed time-interleaved polar DSM transmitter baseband part and time-interleaved polar DSM transmitter baseband parts based on the methods described in Embrahimi et al. and Khoini-poorfard et al. [10,25] (Figure 3) and in Kozak et al. and Erfani Majd et al. [26,27] (Figure 4) for the 7.68-MHz LTE input signal (M is the number of parallel branches, and $M = 1$ means nontime-interleaved architecture)

				Proposed time-interleaved polar DSM transmitter baseband part		Time-interleaved polar DSM transmitter baseband part based on the method described in Kozak et al. and Erfani Majd et al. [26,27]		Time-interleaved polar DSM transmitter baseband part based on the method described in Embrahimi et al. and Khoini-poorfard et al. [10,25]	
Input signal	**BW (MHz)**	***M***	**Clock speed (MHz)**	**OSR**	**SNDR (dB)**	**OSR**	**SNDR (dB)**	**OSR**	**SNDR (dB)**
LTE	7.68	1	245.76	32	41.14	32	41.14	32	41.14
		2	122.88	16	41.13	32	41.14	32	41.13
		4	61.44	8	41.13	32	41.13	32	41.13

Abbreviations: CE, coding efficiency; DSM, delta–sigma modulator; LTE, long-term evolution; OSR, oversampling ratio; SNDR, signal-to-noise-and-distortion ratio.

eliminating delay and downsampler blocks from all the parallel branches in the proposed time-interleaved polar DSM transmitter baseband part significantly reduces the design hardware complexity. Moreover, as shown in Figure 4 (architecture based on Kozak and others and Erfani Majd and others [26,27]), these blocks operate at a higher sampling rate (f_s); therefore, their removal can help considerably reduce dynamic power consumption. Unlike the architecture based on Kozak and others and Erfani Majd and others [26,27], the proposed architecture requires only one signal component separator block instead of M signal component separator blocks. This is because the same input signal is applied to all the parallel branches in this architecture. The signal component separator block is implemented using the CORDIC algorithm (as explained in Section 4), which includes input and output registers and adder–subtractor (AddSub) stages between them. The number of internal AddSub stages is automatically determined using an implementation software tool (Xilinx system generator software, which will be described in Section 4) based on the required accuracy of the output. Therefore, removing $M - 1$ N-bit signal component separator blocks in the proposed architecture can help significantly reduce hardware complexity and power consumption compared with that in the architecture based on Kozak and others and Erfani Majd and others [26,27]. Additionally, as the input signal of the proposed architecture is applied to all the branches with the sampling rate of f_s/M (instead of f_s in the architecture based on Kozak and others and Erfani Majd and others [26,27]), the required input signal OSR of this architecture is M times lower than that of the architecture based on Kozak and others and Erfani Majd and others [26,27]. Consequently, the upsampling technique that is used in the proposed architecture can considerably improve its performance compared with that of previous architectures.

4 | SIMULATION RESULTS

To evaluate the performance of the proposed time-interleaved polar DSM transmitter baseband part, a simulation is performed using MATLAB Simulink. In this simulation, the LTE signal with a bandwidth of 7.68 MHz is used as an input. This signal is applied to the polar DSM transmitter baseband part with different numbers of parallel branches (M). The results are listed in Table 2. The clock speed requirement of the proposed time-interleaved polar DSM transmitter baseband part reduces with an increase in the number of parallel branches. For instance, the clock speed requirement of the proposed time-interleaved polar DSM transmitter baseband part reduces four times (from 245.76 MHz to 61.44 MHz) using the four-branch time-interleaved structure while maintaining the signal quality (~41 dB).

Furthermore, the comparison results of the proposed time-interleaved polar DSM transmitter baseband part and time-interleaved polar DSM transmitter baseband parts based on the methods described in Embrahimi and others and Khoini-poorfard and others [10,25] (Figure 3) and Kozak and others and Erfani Majd and others [26,27] (Figure 4) are listed in Table 2. They have exhibited almost the same SNDR performance for different numbers of parallel branches. As described in Section 3, this is due to the suppression of the aliases in the proposed

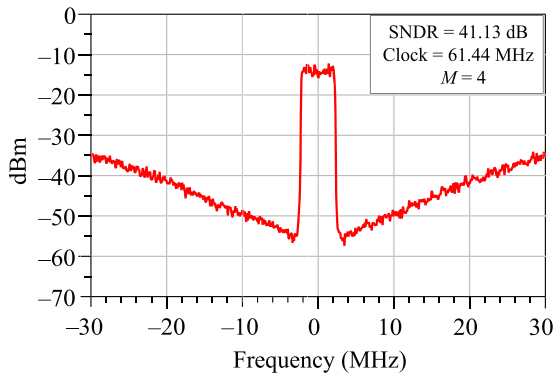

FIGURE 9 Output signal spectrum of the proposed four-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part for the 7.68-MHz long-term evolution (LTE) input signal with an oversampling ratio (OSR) of 8

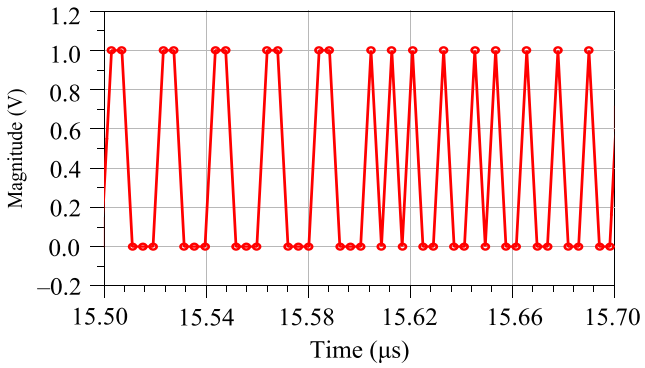

FIGURE 10 Output signal envelope magnitude of the proposed four-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband for the 7.68-MHz long-term evolution (LTE) input signal with an oversampling ratio (OSR) of 8

architecture, which keeps the magnitude of the aliases below the quantization noise level; therefore, their impact on the SNDR performance is negligible. The lower OSR in the proposed two-branch and four-branch architectures is caused by the lower input signal sampling rate in these structures (as described in Section 3). The output signal spectrum of the proposed four-branch time-interleaved polar DSM transmitter baseband part for the 7.68-MHz LTE input signal is shown in Figure 9. The SNDR of this signal is 41.13 dB (Table 2). The output signal envelope magnitude of the proposed four-branch time-interleaved polar DSM transmitter baseband part for the 7.68-MHz LTE input signal is shown in Figure 10. This signal possesses a two-level format (0, 1) and is suitable for the SMPA input signal.

For the verification of the proposed time-interleaved polar DSM transmitter baseband part, the digital implementation of this architecture is performed on a field programmable gate array (FPGA) using the Xilinx system generator and Xilinx ISE design suite software tools. The Xilinx system generator helps implement digital systems on FPGAs. The hardware model of the digital system can be implemented with the synthesizable blocks of the Xilinx system generator in the Simulink environment. The implementation model of the proposed four-branch time-interleaved polar DSM transmitter baseband part in the Xilinx system generator is shown in Figure 11. Gateway-In and Gateway-Out ports are interfaces between analog and digital environments, and only Xilinx system generator blocks can be used between these ports. The analog signal is converted into a 16-bit digital signal at the input. This number of bits is used to minimize the quantization error and resources used on the FPGA. One-bit quantizers are implemented using relational operators and multiplexer blocks. The CORDIC processor is used as the signal component separator to transform quadrature components (I and Q) from the Cartesian coordinate into envelope and phase components in polar coordinates and vice versa. The Xilinx time-division multiplexer block is also used at the output of the CORDICS blocks to upsample and multiplex the quadrature components of all the parallel branches to a single output stream. The rest of the circuit is deployed using delay and AddSub blocks in the Xilinx system generator.

Next, the Verilog hardware code is extracted from the Xilinx system generator and imported to the Integrated Synthesis Environment (ISE) design suite to implement the proposed architecture on the FPGA. The place and route (digital layout) stage is performed in the ISE design suite to implement the proposed architecture and route different parts between the blocks on the FPGA. However, before evaluating the performance of the place and route model of the proposed architecture, a timing analysis should be performed to ensure the appropriate operation of this model. In digital circuits, the delay between two consecutive registers should be lower than the time period of that part of the circuit. In this case, the register inputs are stable at the rising edge of the clock, and thus, the digital circuit behavior can be predicted. Otherwise, the performance of the digital circuit can be affected. The Xilinx system generator helps perform the timing analysis. This software tool, after conducting the place and route operation, identifies the slowest paths between two consecutive registers and determines the amount of their delay, and finally, if the delay is greater than the time period, it is marked in red. The used FPGA is Kintex7. The place and route model timing analysis results of the proposed four-branch time-interleaved polar DSM transmitter baseband part demonstrated that the delay value between two registers is less than the time period and the circuit operates appropriately.

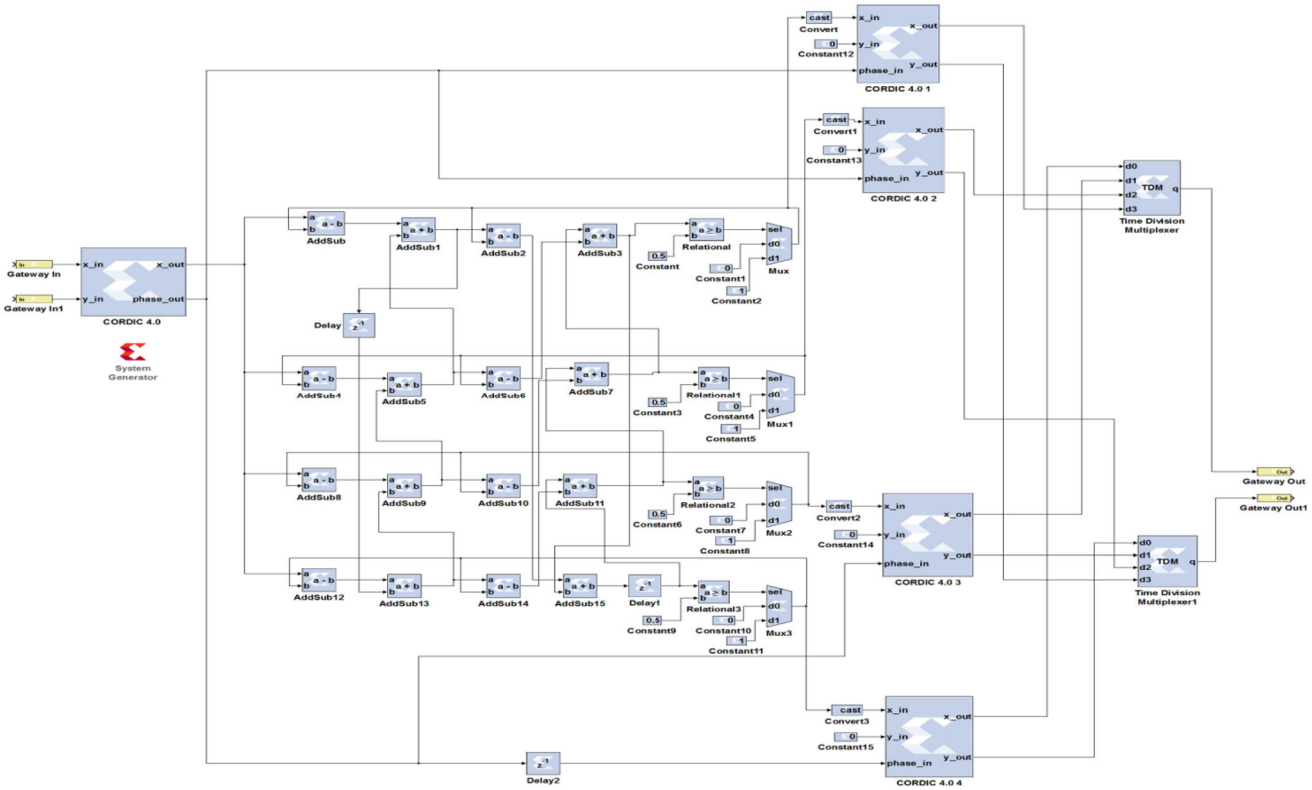

FIGURE 11 Hardware implementation model of the proposed four-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part in the Xilinx system generator

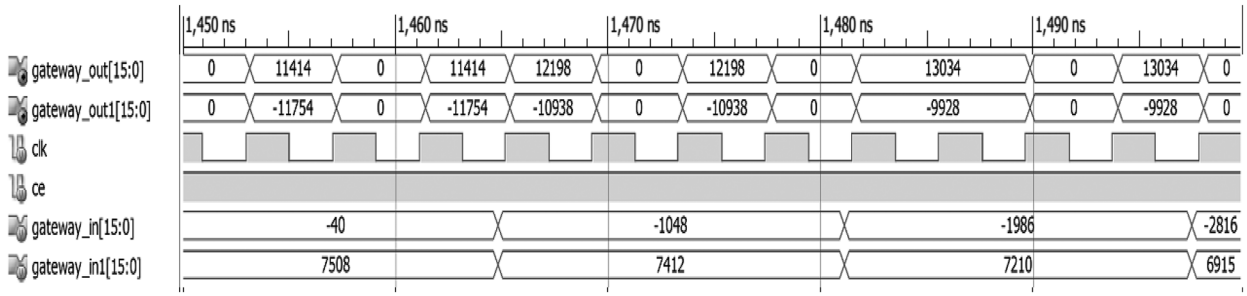

FIGURE 12 Input and output signals of the place and route model of the proposed four-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part for the 7.68-MHz long-term evolution (LTE) input signal with an oversampling ratio (OSR) of 8

After performing the timing analysis, the place and route model of the proposed architecture in the ISE design suite can be generated and evaluated with regard to performance. The input and output signals of the place and route model of the proposed four-branch time-interleaved polar DSM transmitter baseband part are shown in Figure 12. Gateway_in and gateway_in1 are the quadrature components (I and Q) of the input signal, and gateway_out and gateway_out1 are the quadrature components of the output signal. These are 16-bit digital signals (1 bit for sign, 1 bit for the integer part, and 14 bit for the fractional part of the signal).

These signals are depicted in the decimal format (Figure 12). The input signal is the 7.68-MHz LTE signal with an OSR of 8. The sampling rate of the input signal is 61.44 MHz, and it is four times lower than that of the original polar DSM transmitter baseband part (as described in Section 3). Moreover, the output quadrature components are such that the output signal envelope component is 0 or 1. Therefore, the output signal is suitable for driving SMPAs.

The output signal spectrum of the proposed architecture with regard to the place and route model for the 7.68-MHz LTE input signal with an OSR of 8 is shown in Figure 13. The SNDR of this signal is 41.12 dB. This

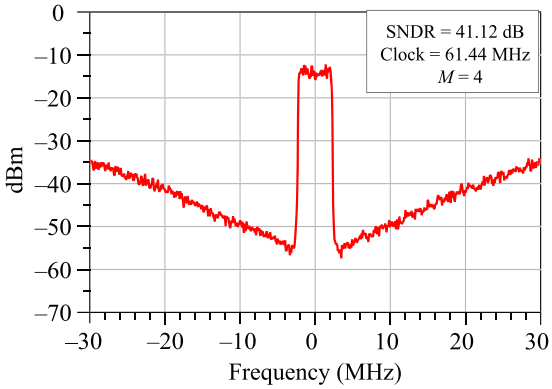

FIGURE 13 Output signal spectrum of the place and route model of the proposed four-branch time-interleaved polar delta–sigma modulator (DSM) transmitter baseband part for the 7.68-MHz long-term evolution (LTE) input signal with an oversampling ratio (OSR) of 8

SNDR is approximately equal to the SNDR listed in Table 2.

The number of resources used on the FPGA and the power consumption of the FPGA for implementing the proposed four-branch time-interleaved polar DSM transmitter baseband part and four-branch time-interleaved polar DSM transmitter baseband part based on the techniques presented in other studies [10,25–27] are summarized and compared in Table 3. The power consumption of the FPGA is determined using the Xilinx Xpower analyzer of the Xilinx system generator. As listed in Table 3, in the proposed four-branch time-interleaved polar DSM transmitter baseband part, the number of used registers reduces from 619 to 364, the number of used look-up tables reduces from 1698 to 1470, and the number of occupied slices reduces from 611 to 458 compared with those in the four-branch time-interleaved polar DSM transmitter baseband part based on the techniques presented in Kozak and others and Erfani Majd and others [26,27] (the best among the time-interleaved techniques before the proposed architecture in terms of performance). Moreover, the power consumption reduces from 65 mW to 49 mW in the proposed architecture. Consequently, eliminating the input delay, downsampler, and $M - 1$ (in this case, three blocks) signal component separator blocks (CORDIC processors) helps considerably reduce the design hardware complexity and power consumption in the proposed architecture.

In the next step, to evaluate the polar DSM transmitter performance with regard to the proposed time-interleaved polar DSM transmitter baseband part, a simulation is performed using the ISE design suite and advanced design system (ADS) (Figure 14). In this simulation system, the place and route model of the proposed four-branch time-interleaved polar DSM transmitter baseband part, which was designed in the FPGA (as described before), is included in the ISE design suite. The output data of this part (gateway_out and gateway_out1 in Figure 12) were extracted and used as the input of the second part, which includes a frequency up converter and SMPA in the ADS. To up-convert the signal into RF (850 MHz), an RF modulator block in the ADS is used. Inverse class F (F^{-1}) is used as the SMPA. The architecture of the used class F^{-1} SMPA, which is based on transmission lines, is shown in Figure 15. The load network that is analyzed at fundamental frequency in this architecture is shown in Figure 16A. In this case, the series transmission line ($TL_1 + TL_2$), along with an open circuited capacitive stub (TL_4) with an electrical length of 30°, is used to match the optimum output device impedance (Z_{opt}) and load resistance (R_L) by tuning the transmission line characteristic impedances Z_1 and Z_2. (L_{out} and C_{out} are the device output series inductance and shunt capacitance, respectively.) Figure 16B shows the load network analyzed using the device at the second harmonic. In this case, TL_3 with an electrical length of 90° is short circuited.

TL_1 forms a second harmonic tank with C_{out} and L_{out} and provides an open-circuit condition at the device output. Figure 16C shows the load network at the third harmonic. In this case, TL_3 is open circuited, and TL_4 is short circuited. Therefore, the series transmission line $TL_1 + TL_2$ with L_{out} provides a short-circuit condition at the device output. As the impedance, which is analyzed using the device, at the second and third harmonics should be infinite and zero, respectively, the electrical lengths of TL_1 and TL_2 (θ_1 and θ_2) can be expressed as follows:

$$2\omega_0 C_{out} - \frac{1}{2\omega_0 L_{out} + Z_1 \tan 2\theta_1} = 0, \tag{11}$$

$$3\omega_0 L_{out} - Z_1 \tan 3(\theta_1 + \theta_2) = 0. \tag{12}$$

According to (12), the total electric lengths of TL_1 and TL_2 can be defined as the functions of L_{out} and C_{out}.

$$\theta_2 + \theta_1 = \frac{\pi}{3} - \frac{1}{3}\tan^{-1}\frac{3\omega_0 L_{out}}{Z_1}. \tag{13}$$

As expressed in (13), the maximum total electrical length of TL_1 and TL_2 ($\theta_1 + \theta_2$) is 60° at the fundamental frequency and 180° at the third harmonic (occurs when $L_{out} = 0$) [28].

The nonlinear model of the GaN transistor (CGH40010, Cree Inc.) has been used to design class F^{-1}

TABLE 3 Number of resources used on the FPGA and the power consumption of the FPGA for implementing the proposed four-branch time-interleaved polar DSM transmitter baseband part and four-branch time-interleaved polar DSM transmitter baseband part based on the techniques presented in previous studies [10,25–27]

	Resources used on the FPGA						
	Slices		Registers		LUTs		Power consumption (mW)
Structure	Used	Total	Used	Total	Used	Total	
Embrahimi et al. and Khoini-poorfard et al. [10,25]	842 (1.65%)	50 950	1072 (0.263%)	407 600	2004 (0.983%)	203 800	86 (at 25°C)
Kozak et al. and Erfani Majd et al. [26,27]	611 (1.199%)		619 (0.151%)		1698 (0.833%)		65 (at 25°C)
Proposed architecture	(0.898%) 458		(0.0893%) 364		(0.721%) 1470		49 (at 25°C)

Abbreviations: DSM, delta–sigma modulator; LUTs, look-up tables.

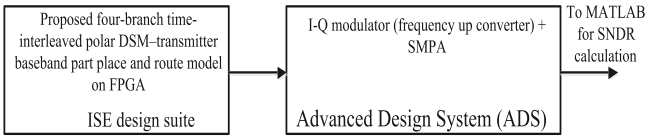

FIGURE 14 Simulation system of the polar delta–sigma modulator (DSM) transmitter

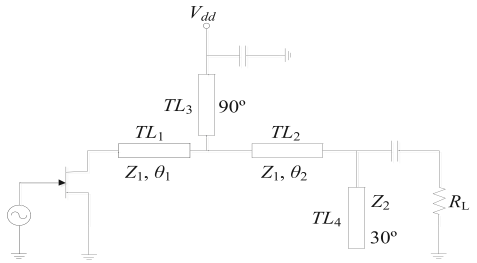

FIGURE 15 Transmission-line-based inverse class F switched-mode power amplifier (SMPA)

SMPA in the ADS. The bias voltages of the transistor are $V_{DS} = 28$ V and $V_{GS} = -3$ V.

Other parameters of the designed SMPA are listed in Table 4. The output signal of class F^{-1} SMPA was extracted from the ADS and used to evaluate SNDR. The SNDR calculation for this signal was performed using MATLAB codes.

The output signal spectrum of the polar DSM transmitter with the proposed four-branch time-interleaved polar DSM transmitter baseband part for the 7.68-MHz LTE signal and OSR of 8 is shown in Figure 17. The SNDR of this signal is 41.12 dB. Moreover, as described before, the output signal envelope of the proposed time-interleaved polar DSM transmitter baseband part

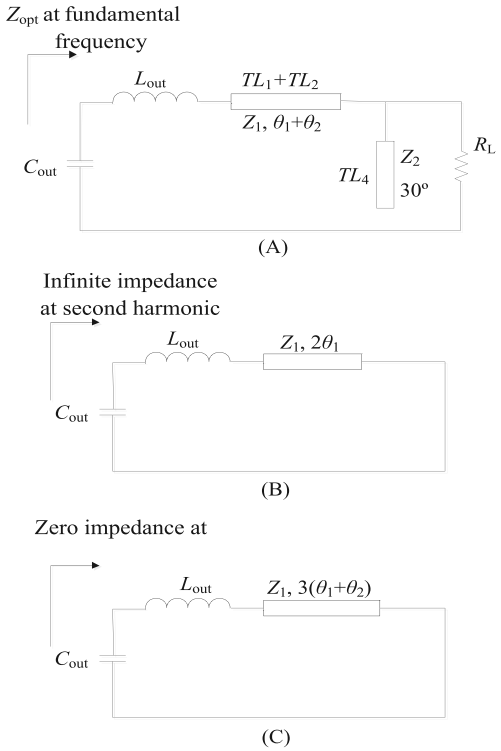

FIGURE 16 Load networks analyzed at different harmonics

includes a two-level format (0, 1). Therefore, this signal is suitable for driving SMPAs without any distortion. For this reason, the SNDRs of the output signals of the transmitter and proposed time-interleaved polar DSM transmitter baseband part are the same.

In addition to the clock speed reduction benefit, this architecture helps increase the bandwidth of the input signal if required. In this case, the required clock speed increases to have the desired OSR. Therefore, this architecture can help reduce the clock speed.

TABLE 4 Parameters of the used SMPA

Class	Frequency (MHz)	V_{DS} (V)	V_{GS} (V)	Output power (dBm)	Gain (dB)	PAE (%)
F^{-1}	850	28	−3	39.6	14	78

Abbreviations: PAE, power added efficiency; SMPA, switched-mode power amplifier.

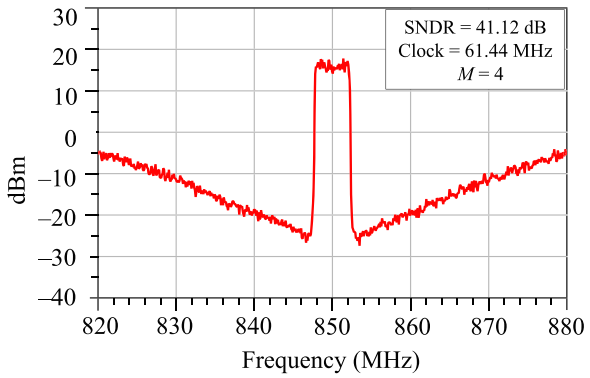

FIGURE 17 Output signal spectrum of the polar delta–sigma modulator (DSM) transmitter and proposed four-branch time-interleaved polar DSM transmitter baseband part for 7.68-MHz long-term evolution (LTE) signal with an oversampling ratio (OSR) of 8

5 | CONCLUSIONS

The main disadvantage of using the polar DSM transmitters is the necessity for high clock speed to have the desired SNDR. This study used an upsampling technique to introduce a low-complexity time-interleaved polar DSM transmitter baseband part to reduce the clock speed requirement of the polar DSM transmitter. The simulation results indicated that the clock speed requirement of the polar DSM transmitter is reduced by four times using the proposed four-branch time-interleaved polar DSM transmitter baseband part while maintaining the SNDR.

CONFLICT OF INTEREST

The authors declare that there are no conflicts of interest.

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