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Single-balanced Direct Conversion Quadrature Receiver with Self-oscillating LMV

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Abstract

This paper proposes two kinds of single-balanced direct conversion quadrature receivers using self-oscillating LMVs in which the voltage-controlled oscillator (VCO) itself operates as a mixer while generating an oscillation. The two LMVs are complementary coupled and series coupled to generate the quadrature oscillating signals, respectively. Using a 65 nm CMOS technology, the proposed quadrature receivers are designed and simulated. Oscillating at around 2.4 GHz frequency, the complementary coupled quadrature receiver achieves the phase noise of –28 dBc/Hz at 1KHz offset and –109 dBc/Hz at 1 MHz offset frequency. The other series coupled receiver achieves the phase noise of –31 dBc/Hz at 1KHz offset and –109 dBc/Hz at 1 MHz offset frequency. The simulated voltage conversion gain of the two single-balanced receivers is 37 dB and 45 dB, respectively. The double-sideband noise figure of the two receivers is 5.3 dB at 1 MHz offset. The quadrature receivers consume about 440 μW dc power from a 1.0-V supply.

Keywords: *CMOS, Double-sideband Noise Figure, Double-balanced Mixer, Phase Noise, Quadrature, Single-balanced Mixer, Series LC Tank, LMV Cell, Voltage-controlled Oscillator*

1. Introduction

Single stage circuits combining oscillator and mixer have been designed for the purpose of a higher degree of chip integration and reducing power consumption. For the highly integrated and low power radio frequency (RF) receiver front-end, a current reuse technique is generally adopted among different functional blocks. A popular method is cascoding the mixer on top of the low-noise RF input stage, while less frequent is stacking the mixer above the voltage-controlled oscillator (VCO) [1-5]. The other method is to run the 'VCO as a mixer' presented in [6]. Several examples of single stage RF front-ends based on the fundamental local oscillation (LO) frequency are introduced for the direct conversion receiver. The direct conversion receiver has significant advantage for higher integration compared to the superheterodyne receiver. However, it has several disadvantages such as LO self-mixing, which can critically degrade the receiver performances. Since the RF frequency is directly translated to near dc, any dc offset created by the self-mixing can distort the desired signal.

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A double-balanced mixer is stacked on top of the VCO by using the current reuse topology. The RF input signal is applied to the input of the mixer, and the oscillator signal is applied to the source nodes of the mixer. Since the differential oscillator nodes are connected to the source nodes of the RF transistors, the impedance at the LC tank is quite low and it is difficult to run the oscillation with low power consumption [1].

The RF front-end merges low-noise amplifier (LNA), mixer, and VCO (called the LMV cell) in a single stage. This topology stacks VCO on top of the mixer. The current source of the mixer is modified as the LNA with inductor degeneration. This topology performs RF amplification, mixing, and LO generation while sharing the same dc bias current and the same devices among all the blocks of the RF front-end, resulting in a very low power and small-area chip solution. Since the intermediate frequency (IF) outputs are connected to the source nodes of the VCO, the voltage gain is limited due to the low impedance at the source nodes. Also, this topology is single-balanced and has a large LO leakage to IF output through parasitic capacitances of the switching transistors [2]. The mixer itself can be double-balanced to reduce the LO leakage to IF output by modifying the single-balanced topology [5]. All the topologies adopted the stacking method to implement the self-oscillating mixer. The VCO itself plays the role of mixer while generating the oscillation frequency. Instead stacking the separate LNA, mixer and VCO, this topology adopts the concept of 'VCO as a mixer' by exploiting the series inductor-capacitor (SLC) tank resonator [6].

In this paper, a single-balanced direct conversion quadrature receiver using a self-oscillating LMV is proposed. The proposed quadrature self-oscillating LMV truly plays the role of 'VCO as a mixer' with dual functions of mixer and differential VCO. Two self-oscillating LMVs are complementary quadrature coupled to implement the receiver which includes four coupling transistors as in the conventional QVCOs. The quadrature low frequency IF or baseband signal can be directly extracted from the drain outputs of the two differential VCOs through the simple first-order RC low-pass filter (LPF).

This paper is organized as follows. In Section 2, the concept of cross-coupled mixer and the self-oscillating LMV is described. In Section 3, direct conversion quadrature receivers with single-balanced self-oscillating LMV is described and experimental performances are given based on the simulation using 0.18 μm CMOS technology. Finally, a conclusion is given.

2. Self-oscillating Quadrature LMV

Figure 1 shows the SLC LMV proposed in [7].

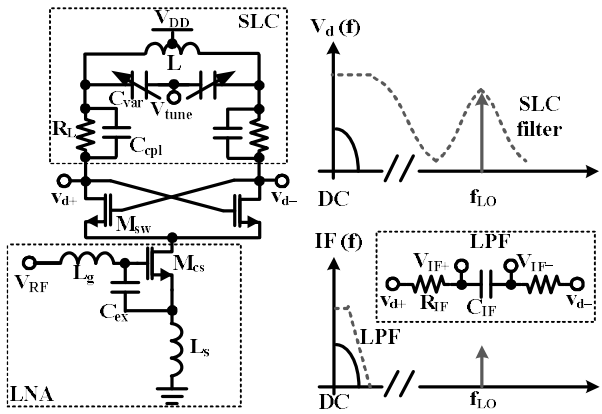


Figure 1. Differential SB-LMV.

At the RF, the LMV is exactly the same with the conventional parallel LC VCO. At the IF, the LMV is exactly the same with the single-balanced mixer (SBM). Based on this SLC LMV, quadrature receiver can be implemented using the quadrature VCO coupling techniques. Figure 2 shows several topologies for quadrature

signal generation using two VCOs [8, 9].

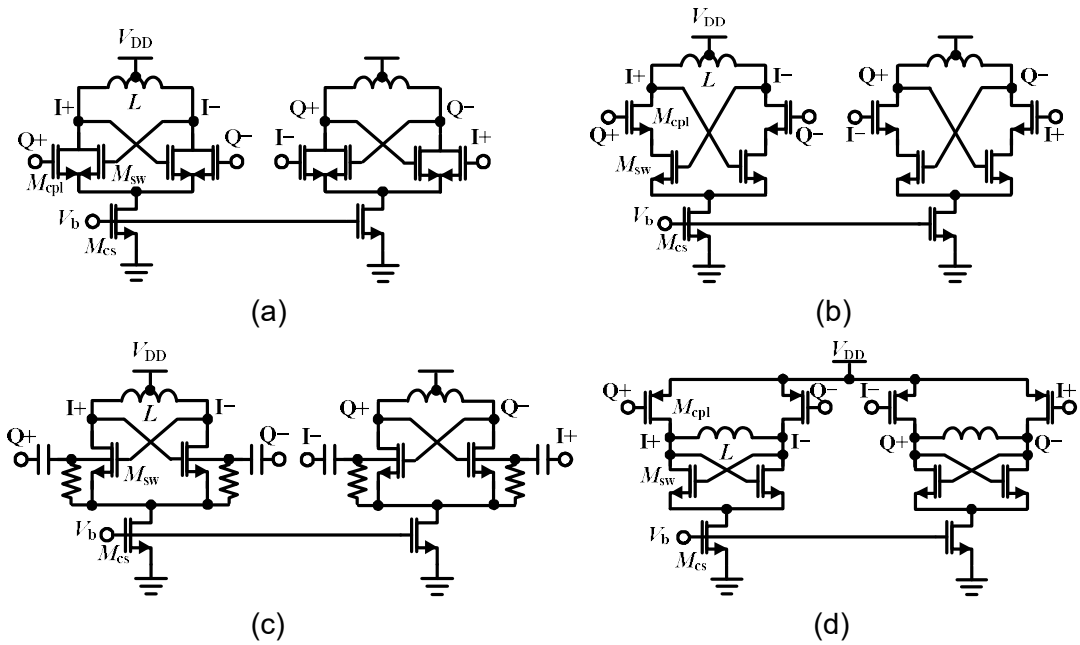


Figure 2. Several QVCO topologies. (a) P-QVCO, (b) S-QVCO, (c) BG-QVCO, and (d) C-QVCO.

Figure 2(a) shows the P-QVCO in which two VCOs are coupled through the parallel transistor M_{cpl}. The parallel coupling transistor contributes large phase noise to the output. Figure 2(b) shows the S-QVCO in which two VCOs are coupled through the series coupling transistor in a cascode-like fashion. The S-QVCO displays an excellent phase noise performance. The other method as shown in Figure 2(c) is called BG-QVCO in which the two VCOs are coupled through the body terminal (or back-gate) of the switching transistor. The BG-QVCO also shows an excellent phase noise behavior. In terms of phase and amplitude errors of QVCO, the simulation results show that the BG-QVCO has large phase and amplitude errors compared to P-QVCO and S-QVCO. Figure 2(d) shows the complementary QVCO (C-QVCO) in which two differential VCOs are quadrature coupled using the complementary PMOS transistors. This topology has lower phase noise compared to that of the S-QVCO since the quadrature coupling is made through the PMOS FETs which has much lower flicker noise than that of the NMOS FETs.

Figure 3 shows the phase noise performance of C-QVCO and S-QVCO.

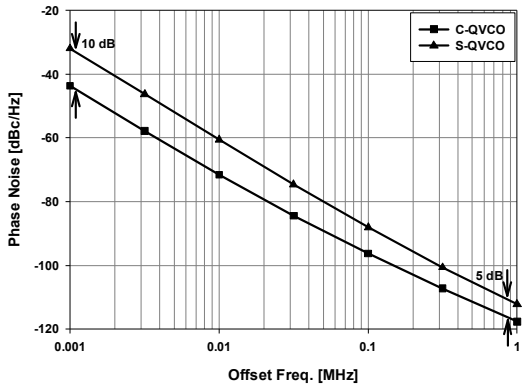


Figure 3. Phase noise performance of C-QVCO and S-QVCO.

The C-QVCO has good phase noise and better in-phase (I) and quadrature (Q) imbalance compared to that of the S-QVCO. For the same dc current flow, simulation results show that the phase noise of the C-QVCO compared to that of the S-QVCO has about 10 dB and 5 dB lower at 1 kHz and 1 MHz offset frequencies, respectively. Considering 0.5% inductor mismatch, the IQ phase error of the C-QVCO and S-QVCO is about 2 degrees. The amplitude error of C-QVCO is much lower (0.02 dB) compared to that of the S-QVCO (0.7 dB).

Based on the quadrature coupling of VCOs in Figure 2, the quadrature LMVs can be implemented. Figure 4 shows the proposed single balanced quadrature LMVs (SB-QLMVs).

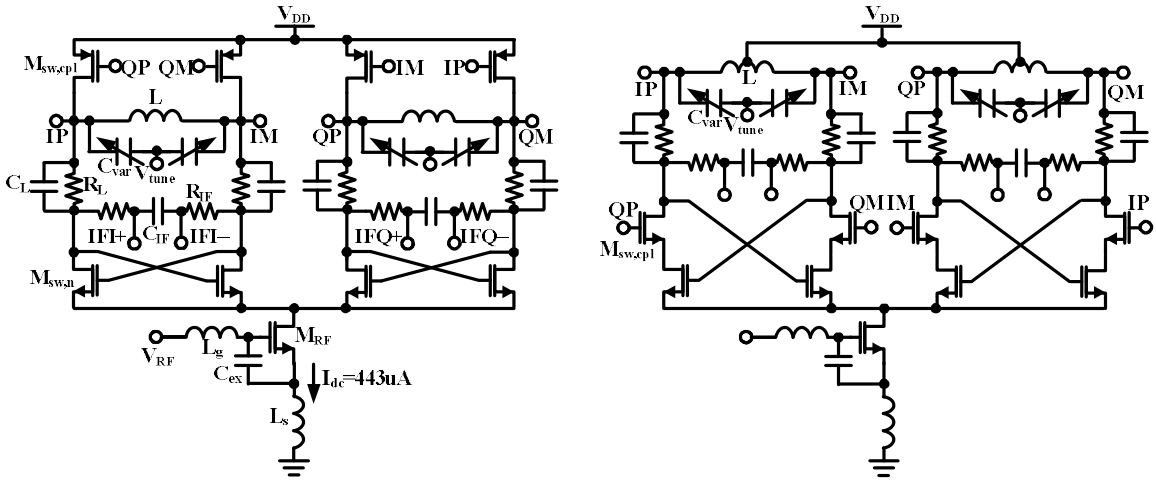


Figure 4. Proposed SB-QLMVs (a) complementary coupled and (b) series coupled.

Compared to the QLMVs previously reported, the proposed SB-QLMVs have much larger LO swing and simplicity, thereby results in lower noise figure performances of the receiver [10].

Figure 5 shows the small-signal equivalent circuit of the RF input transistor. The size of L_g and L_s are chosen using the simultaneous noise and input matching (SNIM) technique to match the signal source impedance of 50 ohm [11].

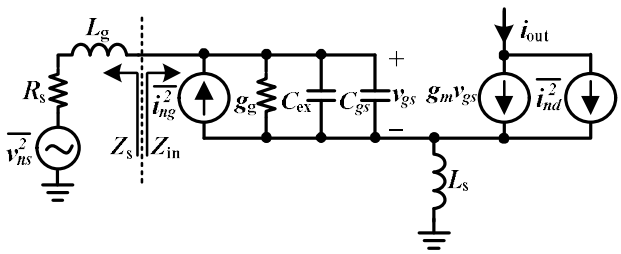


Figure 5. Small-signal equivalent circuit of the LNA.

To verify the performances of the proposed SB-QLMVs, they are designed and simulated using a 65 nm CMOS technology. An octagonal shape symmetric inductor is used to have higher Q (larger than 10) factor for better phase noise performance. The inductor is realized with thick copper top metal (thickness is 3.4 um). The switching transistors are implemented with the NMOS and PMOS FETs. The PMOS transistors are sized to have 120 μm/0.18 μm. The capacitors are implemented with metal-insulator-metal (MIM) capacitors. The tuning range (TR) covers 2.4 GHz wireless local area network (WLAN) frequencies and can be varied with

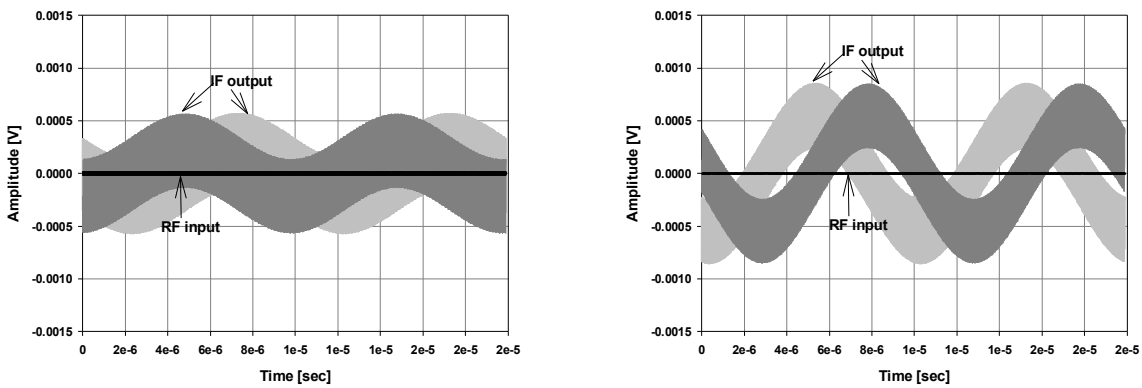
the MOS varactors.

Table 1 shows the device parameters of the proposed SB QLMV.

Table 1. Device Parameters

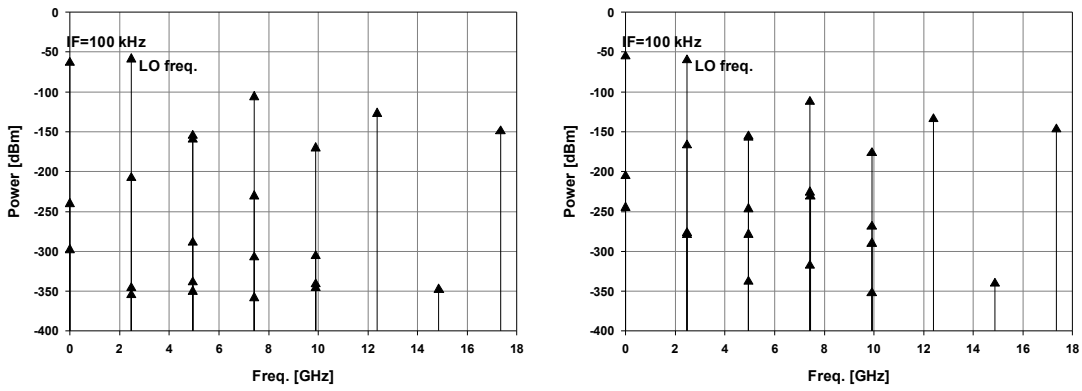
Devices	Complementary coupled	Series coupled
$M_{sw,cpl}$ (μm/μm)	32/0.06	32/0.06
$M_{sw,n}$ (μm/μm)	32/0.06	32/0.06
M_{RF} (μm/μm)	64/0.06	28/0.06
C_L (pF)	4	4
R_L (Ohm)	2545	2545
C_{IF} (pF)	4	4
R_{IF} (kOhm)	5	5
L (nH)	11.5	12

Figure 6 shows the RF input and IF output signal swing of the complementary coupled and series coupled SB-QLMVs with RF input power of -100 dBm. Figure 7 shows the IF output spectrum of the complementary coupled and series coupled SB-QLMVs.



(a) (b)

Figure 6. RF input and IF output swing (a) complementary coupled and (b) series coupled

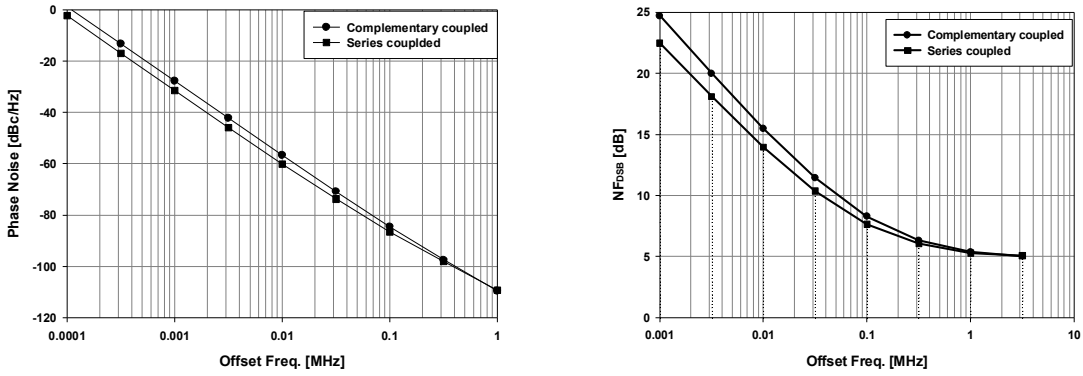


(a) (b)

Figure 7. IF output spectrum with (a) complementary coupled and (b) series coupled

As expected, the quadrature IF output signals of the SB-QLMVs are seriously contaminated by the LO leakage even with the large capacitors in the IF LPF. The voltage gain of the series coupled SB-QLMV is quite larger than that of the complementary coupled one.

Figure 8 shows the phase noise and double-sideband (DSB) noise figure (NF) of the SB-QLMVs. The dc current of the SB-QLMVs is about 440 μA from a 1.0 V supply voltage.



(a) (b)

Figure 8. The performance of QLMV (a) phase noise and (b) double sideband noise figure.

Table 2. Performance Summary of the SB-QLMV

Specification	Complementary coupled	Series coupled
Oscillation frequency (GHz)	2.48	2.48
P_{DC} (μW)	442	443
Phase noise (dBc/Hz) @1kHz	–28	–31
@1MHz	–109	–109
DSB NF (dB) @1kHz	24.7	22.4
@1MHz	5.3	5.3
Voltage gain (dB)	37	45

Table 2 summarizes the performance of the proposed SB-QLMVs. From the simulation results, the QLMVs are expected to be successfully integrated for the direct conversion receiver such as smartphone, WLAN, global positioning system (GPS), satellite communication receiver, medical body area network (BAN), and cable TV (CATV) set-top box while consuming low power with just one integrated block.

4. Conclusion

By utilizing differential VCO with series LC resonator, this paper proposes two kinds of fully integrated quadrature RF front-end single-balanced LMVs by merging LNA, mixer and QVCOs. The QVCOs play the dual role of mixer and oscillator, truly operating 'VCO as a mixer'. The QLMVs are designed and simulated using 0.18 μm CMOS technology. The quadrature coupling of the two VCOs are achieved by complementary coupling using PMOS FETs and series coupling techniques using NMOS FETs. The quadrature IF signals are extracted at the drain nodes of the cross-coupled NMOS pairs through the LPFs. Operating at around 2.4 GHz

WiFi band the two QLMVs have similar phase noise and noise figure performance. The series coupled QLMV has better voltage gain compared to that of the complementary coupled QLMC. The proposed QLMVs can be easily integrated on a single chip, and applied for low-power high-performance direct conversion RF receiver front-end.

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