Original Article

Thermal-annealing behavior of in-core neutron-irradiated epitaxial 4H–SiC

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A B S T R A C T

The effect of thermal annealing on defect recovery of in-core neutron-irradiated 4H–SiC was investigated. Au/SiC Schottky diodes were manufactured using a 4H–SiC epitaxial wafer that was neutron-irradiated at the HANARO research reactor. The electrical characteristics of their epitaxial layers were analyzed under various conditions, including different neutron fluences (1.3×10^{17} and 2.7×10^{17} neutrons/cm^2) and annealing times (up to 2 h at 1700 °C). Capacity–voltage measurements showed high carrier compensation in the neutron-irradiated samples and a recovery tendency that increased with annealing time. The carrier density could be recovered up to 77% of the bare sample. Deep-level-transient spectroscopy revealed intrinsic defects of 4H–SiC with energy levels 0.47 and 0.68 eV below the conduction-band edge, which were significantly increased by in-core neutron irradiation. A previously unknown defect with a high electron-capture cross-section was discovered at 0.36 eV below the conduction-band edge. All defect concentrations decreased with 1700 °C annealing; the decrease was faster when the defect level was shallow.

1. Introduction

It is now well-known that silicon carbide (SiC) devices can frequently outperform devices based on conventional semi-conductors such as silicon [1]. SiC is particularly suitable for application in harsh environments, exhibiting excellent temperature and radiation resistance because of its wide band gap and strong silicon–carbon bonds. However, the material also poses various difficulties. The processes of single-crystal growth and etching in SiC are fundamentally difficult. Moreover, certain device processes, e.g., ion-implantation doping of the SiC epi-layer for junction formation, can raise the risk of radiation damage [2–6].

Recently, the technique of neutron transmutation doping (NTD) has been applied to uniform doping of wide-band-gap semi-conductors such as SiC [7,8]. The doping is conducted in a research reactor. In the in-core area of the reactor, not only thermal neutrons, but also epithermal neutrons, fast neutrons, and gamma rays are present; these various types of radiation affect the electrical properties of SiC through lattice damage. For recovery from such lattice damage and for activation of the semiconductor material, post-implantation thermal annealing is performed, typically at 1600–1800 °C. However, detailed studies of in-core neutron-irradiated SiC have not been conducted.

In this study, neutron damage and recovery in the SiC epitaxial layer were investigated using a 4H–SiC Schottky diode. The 4H–SiC epitaxial wafer was irradiated by in-core neutrons in the vertical irradiation hole of the High Flux Advanced Neutron Application Reactor (HANARO) at the Korea Atomic Energy Research Institute (KAERI), and the change in electrical characteristics with neutron fluence and annealing process was observed.

2. Materials and methods

Samples consisted of N-type epitaxial 4H–SiC (TYSiC Co., Ltd.) diced at 1 cm × 1 cm. The thickness and doping density of the epitaxial layer were 30 μm and 9.55×10^{14} cm^{-3}, respectively. The doping density of the n-type substrate and the thin buffer layer was 1.0×10^{18} cm^{-3}, and a total thickness of the wafer, including the epi-layer, was 373 μm.

The sample was irradiated in the NAA1 vertical irradiation hole at HANARO using a pneumatic transfer system [9]. Fig. 1(a) is a top view of the HANARO core showing the location of NAA1. During irradiation, reactor power was maintained at 15 MW$_{th}$. The
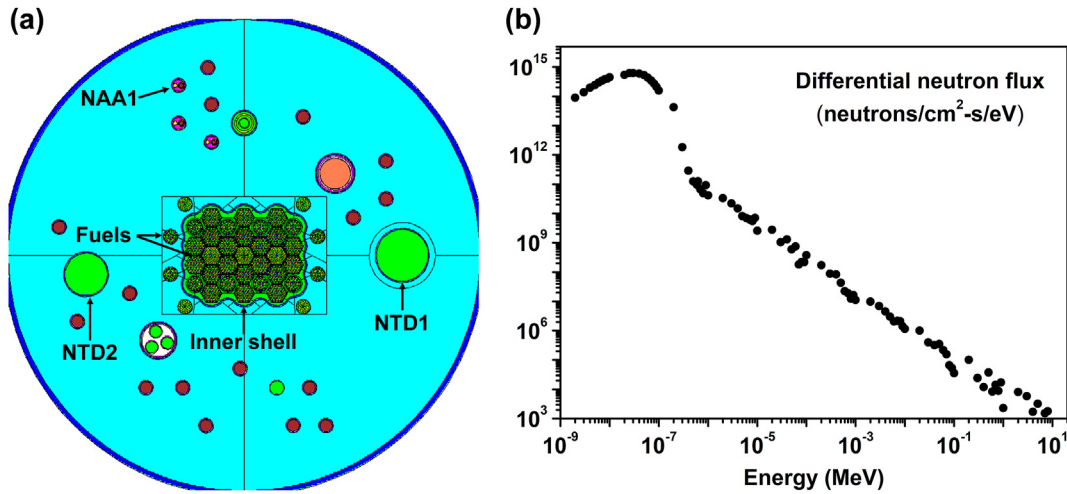
Fig. 1. (a) Location of the NAA1 vertical irradiation hole in the HANARO reactor. (b) Calculated differential neutron flux in NAA1. (NAA, neutron activation analysis; NTD, neutron transmutation doping).

thermal-neutron flux at the NAA1 irradiation hole (measured by the cobalt-wire activation method) was 1.33×10^{13} neutrons/cm^{2}s. The neutron-energy spectrum at NAA1 was calculated by Monte Carlo simulation using the Monte Carlo N-particle (MCNP) code. Fig. 1(b) shows the calculated energy-differential neutron spectrum in the hole. The thermal- and fast-neutron fluxes were calculated to be 4.39×10^{13} and 2.31×10^{10} neutrons/cm^{2}s, respectively, and the thermal-to-fast-neutron-flux ratio was 99.95%.

The in-core neutron-irradiated samples were annealed in a graphite furnace (Setaram Inc.) at 1700 °C with a heat rate of 50 K/min. During annealing, the samples were installed in the sample holder of an alumina (Al_2O_3) crucible, with contact between sample and sample holder minimized for uniform heating. The Ar-gas flow rate was maintained at 30 ml/min. The neutron-irradiated samples were annealed for times ranging from 30 to 120 min. The in-core neutron-irradiation and annealing processes are summarized in Table 1. Fig. 2 defines the annealing profiles and shows a photograph of the SiC sample in the alumina crucible of the heating furnace.

Next, the samples were washed with acetone and ethanol for 5 min and 49% hydrofluoric acid for 10 s, then washed with deionized water. To fabricate the Schottky barrier diodes (SBDs), Au and Ag were sputter-deposited on opposite sides of the samples using a CCU-010 coating unit (Safematic Co., Ltd.). The diameter and thickness of the Au Schottky electrode were 3 mm and 100 nm, respectively. A 65-μm-thick polyimide mask was used to form the circular Schottky electrode at the center of the sample. The Ag ohmic electrode was formed on the entire back side of the sample

with thickness of 100 nm.

$C–V$ (current–voltage) measurement was performed on the annealed samples using an MFIA capacitance meter (Zurich Instrument Co., Ltd.). The amplitude of the AC signal was 300 mV; the frequency was 100 kHz. The $I–V$ (current–voltage) characteristics of each sample were measured using a Keithley 2612A source meter (Keithley Tektronix, Inc.). All $C–V$ and $I–V$ measurements were carried out at room temperature. In addition, deep-level-transient spectroscopy (DLTS) was performed to evaluate neutron damage to the crystal structure. The DLTS measurement system, which was developed by KAERI, consists of a vacuum chamber for sample mounting, a helium compressor, and a Lake Shore 335 temperature controller (Lake Shore Cryotronics, Inc.), including a capacitance meter. The temperature was scanned from 80 to 330 K in 1 K steps. The total scan time was 22 h. The capacitance-transient signal at each temperature was measured using the MFIA capacitance meter.

3. Results and discussion

Fig. 3 presents the $C–V$ curves of diode samples with different neutron fluences and annealing profiles. In samples A$_2$, A$_3$, and E (the bare sample), the capacitance increased as the reverse bias decreased. In the $C–V$ curves of samples A$_1$, A$_2$ and A$_3$ (which had progressively longer annealing times) the recovery effect is visible: as the annealing times grew longer, the corresponding curves approached that of the bare sample (E) more closely. It is inferred that crystal recovery in 1700 °C heat treatment was continuously performed up to 120 min of annealing time. For samples A$_1$, B$_1$, B$_2$,

Table 1

In-core neutron-irradiation and annealing processes in the experiment.

Sample	Irradiation time (sec)	Neutron fluence (neutrons/cm^2)	Annealing		
			Temperature (°C)	Time (min)	Profile[a]
A$_0$	9999	1.33×10^{17}	no annealing		
A$_1$			1700	30	Ann1
A$_2$				60	Ann2
A$_3$				120	Ann3
B$_0$	19998	2.66×10^{17}	no annealing		
B$_1$			1700	30	Ann1
B$_2$				60	Ann2
B$_3$				120	Ann3
E	no irradiation		no annealing		

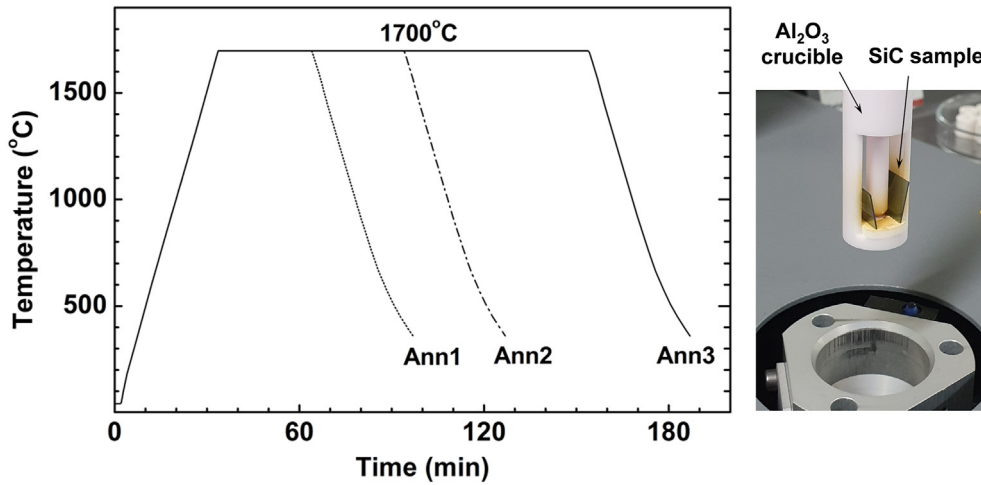[a] Annealing profiles for each sample are given in Fig. 2.

Fig. 2. The four annealing profiles used in the experiment (Left) and photograph of an SiC sample in the alumina crucible of the heating furnace (Right).
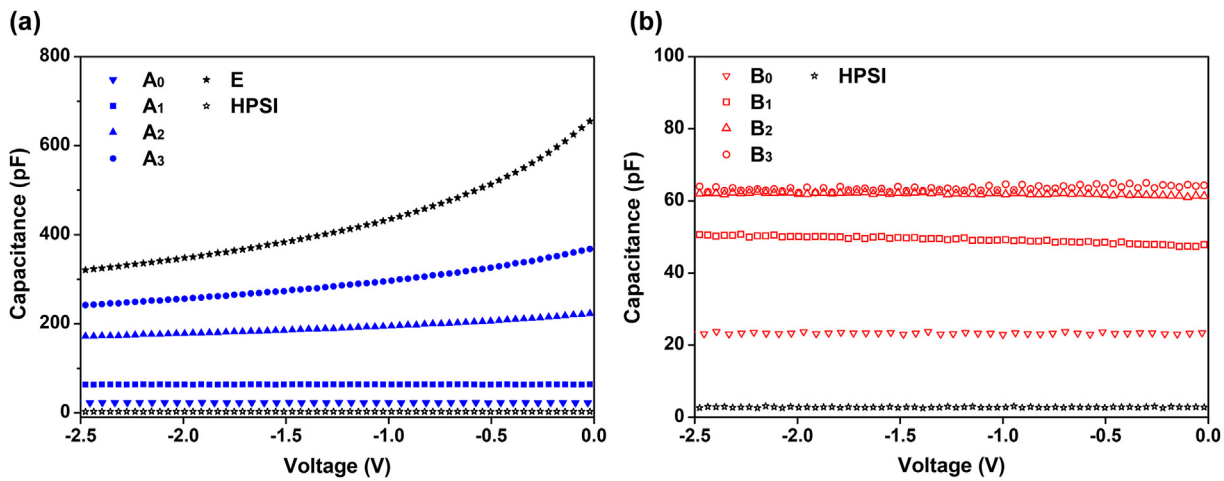

Fig. 3. $C-V$ curves for the (a) A-group and E samples, and (b) B-group samples. (Neutron fluence and annealing profiles for each sample are listed in Table 1).

and B_3, the capacitances were constant in the range 50—65 pF independently of the reverse bias. Thus, no charge movement occurred at the boundary of the depletion layer in the SiC formed by the Schottky metal: either the SiC became amorphous because of excessive lattice damage, or there was not enough time for lattice recovery. In addition, the $C-V$ curves of diode sample which was annealed at 800 °C for 30 min after irradiation with 1.33×10^{17} cm^{-2} of neutron fluence was measured to investigate the effect of thermal annealing at low temperature. The measured capacitance was constant around 22.4 pF which was almost the same as that of the as-irradiated sample, A_0 and B_0 (not shown in the figure). Thus, apparent defect recovery was not achieved at the annealing temperature of 800 °C.

Fig. 4(a) shows the $1/C^2$ plots of samples A_2, A_3, and E. Using the Mott-Schottky equation [10], carrier concentration (N_d) and built-in potential (V_{bi}) were evaluated (Table 2). It can be seen that N_d of the neutron-irradiated samples increased with annealing time, becoming closer to that of the bare sample. Built-in potential also increased after neutron-irradiation, but was decreased by thermal annealing. As the voltage changed from −2.5 V to 0 V, the depletion widths of A_2, A_3, and E changed by approximately 1000 nm. Because $d(1/C)^2/dV$ showed little change, it can be inferred that the defects in the epi-layer were distributed uniformly. The $1/C^2$ plots for A_1, B_1, B_2, and B_3 are shown in Fig. 4(b); because of the abnormal

forms (almost flat or rising with voltage) of these curves, N_d and V_{bi} cannot be calculated.

The zero-bias capacitances of samples in the A and B groups are shown in Fig. 5. For both groups of samples (even the B group, for which N_d could not be calculated), larger zero-bias capacitance corresponded to longer annealing time. For samples A_2 and A_3, the increase rate of the capacitance was different from that of N_d. Carrier concentrations of the A_2 and A_3 samples were evaluated to be 53% and 77% of that of the bare sample, respectively; their zero-bias capacitances were 34% and 56% of that of the bare sample.

Theoretically, the zero-bias capacitance (C_D) of a metal−semiconductor (MS) junction is

$$C_D = \varepsilon_s / W_D = \sqrt{q \varepsilon_s N_d / 2(V_{bi} - kT/q)} \qquad (1)$$

where ε_s is the dielectric constant, W_D is the width of the depletion layer, q is the electric charge, k is the Boltzmann constant, and T is the temperature. According to Equation 1, C_D is proportional to $[N_d/(V_{bi} - kT/q)]^{1/2}$. This agrees with the data: for samples A_2, A_3, and E, there was a simultaneous increase in N_d and decrease in the built-in potential, and also an increase in C_D as predicted. The same may be true in the B samples, although for them C_D could not be evaluated.

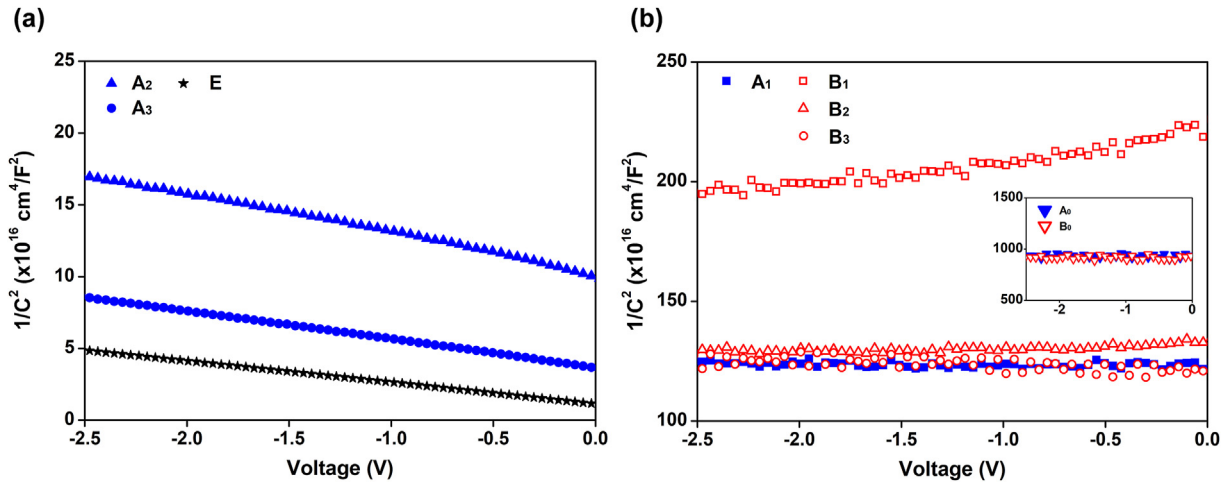Fig. 6 shows the forward-bias $C-V$ curves for the samples in

(a)

(b)

Fig. 4. Inverse square of capacitance for (a) A-group and E samples, and (b) A_1 and B-group samples. Data for non-annealed samples (A_0 and B_0) are shown in the box of (b). The curves in (b) are considered abnormal.

Table 2
Calculated carrier concentration and built-in potential for each sample.

Sample	Carrier concentration (cm^{-3})	Built-in potential (V)
A_1	-	-
A_2	5.13×10^{14}	3.62
A_3	7.43×10^{14}	1.89
B_1	-	-
B_2	-	-
B_3	-	-
E	9.69×10^{14}	0.76

Table 1. $C-V$ data for 500-μm-thick high-purity semi-insulated (HPSI) 4H–SiC are also shown in the figure. The same fabrication and measurement procedures (dicing and metallization, etc.) were used for the HPSI as for the other samples. In the cases of the HPSI, A_0, and B_0, no capacitance change was found, because there could be no carrier flow up to 3 V. On the other hand, A_1, B_1, B_2, and B_3 showed slight increasing capacitance beyond 0.5–1.0 V. Perhaps carrier flow occurred at the MS junction because the crystal structure in the epi-layer was partially recovered for the corresponding samples. The order of the capacitance-increase rates of the A and B groups is consistent with the order of high zero-bias capacitance in Fig. 5; i.e., the level of crystal recovery is high in the order $A_3 > A_2 > B_3 > A_1 > B_2 > B_1$.
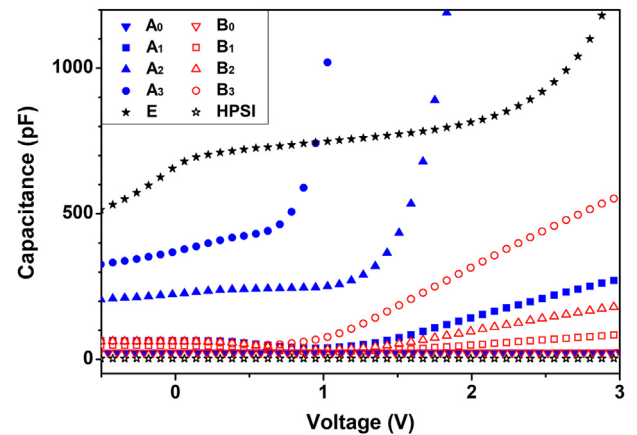

Fig. 6. Forward-bias $C-V$ characteristics for samples (see Table 1; HPSI: high-purity semi-insulated 4H–SiC).

Fig. 7 shows the forward bias $I-V$ curve for all samples. In the case of sample A_0 and B_0, the current hardly changed with respect to the voltage. This is not significantly different from the results for the HPSI sample; the wafer may become semi-insulated because of
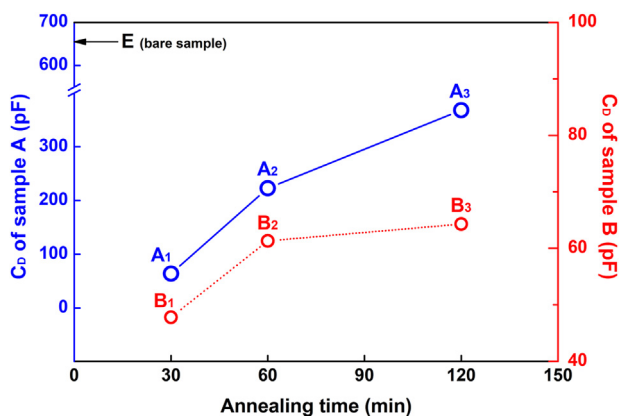

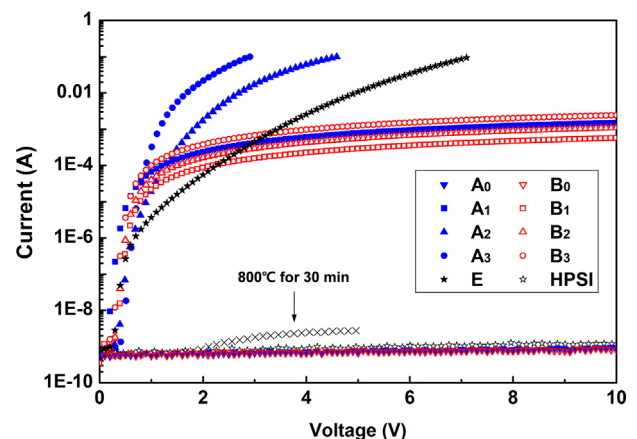**Fig. 5.** Measured zero-bias capacitance C_D for irradiated and annealed samples (A and B groups).

Fig. 7. Forward bias $I-V$ curves for all samples (see Table 1; HPSI: high-purity semi-insulated 4H–SiC).
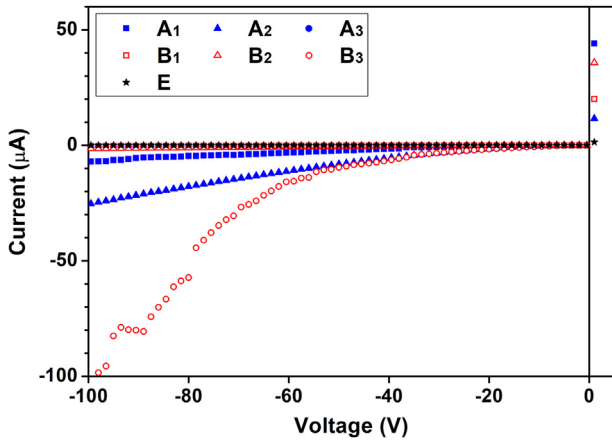
Fig. 8. Reverse bias *I*–*V* curves for the A- and B-group samples and bare sample (E).

neutron damage. On the other hand, sample which was annealed at 800 °C for 30 min after irradiation with 1.33×10^{17} cm^{-2} of neutron fluence, showed weak thermal emission of carriers, with a turn-on voltage at ~2 V. The resistances of HPSI and non-annealed samples were 1.52×10^{10} Ω and 1.10×10^{10} Ω, respectively, corresponding to almost the same resistivity (~2×10^{10} Ω-cm). In the other samples, by contrast, typical diode *I*–*V* curves were found. For 1700 °C-annealed samples other than A$_2$ and A$_3$, similar slopes were observed at the region of high forward bias (>1 V) where the series-resistance component had an effect.

The reverse bias *I*–*V* curves for A-group, B-group and E, shown in Fig. 8, are all typical diode curves, suggesting functionality in terms of device performance. The degree of increase in leakage current was irrelevant to the degree of crystal recovery. However, breakdown phenomena and a non-negligible increase in leakage with reverse bias were observed in A$_1$, A$_2$, and B$_3$. As the size of the electrode in the experiment was quite large (3 mm diameter), this seems to have been due to external factors such as the surface conditions, not to differences in irradiation or annealing conditions.

Fig. 9 shows forward bias *I*–*V* curves in a low voltage range for the diode samples in Fig. 8. The turn-on voltage of each sample was in the range 0.1−0.4 V. The region of logarithmic increase for each set of data is where the thermionic emission of carrier occurred; using thermionic emission theory [10], the ideality factor (*n*), barrier height (Φ_B), and reverse saturation current (I_0) were calculated (Table 3).

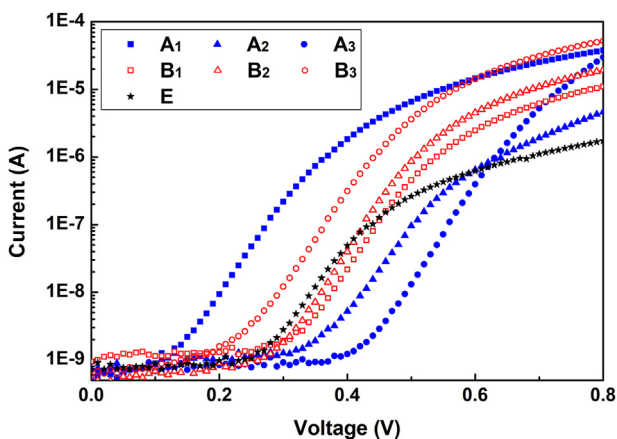**Fig. 9.** Forward bias *I*–*V* curves in a low voltage range for A- and B-group samples and bare sample (E).

Table 3
Ideality factor *n*, barrier height Φ_B, and reverse saturation current I_0 for each sample.

Sample	Ideality factor	Barrier height (V)	Reverse saturation current (A)
A$_1$	1.20	1.03	1.51E-11
A$_2$	1.31	1.18	3.49E-14
A$_3$	1.13	1.30	4.59E-16
B$_1$	1.17	1.18	4.28E-14
B$_2$	1.10	1.19	3.13E-14
B$_3$	1.16	1.11	5.45E-13
E	1.26	1.13	2.87E-13

No dependence of *n* and Φ_B on the neutron fluence or annealing time was apparent. The Φ_B values were much lower than the known value [11], perhaps because the metallization in the experiment was carried out using sputtering at room temperature. Although Φ_B tends to be inversely proportional to *n* [12], no relationship at all between them was observed; the epitaxial surface may have changed under the influence of neutron irradiation or annealing.

Fig. 10 shows the DLTS measurement results of samples A$_2$ and A$_3$. In the DLTS spectrum, three defect peaks (#1, #2, and #3) appeared near 130, 230, and 285 K, respectively. The energy level and electron capture cross-section of each peak were calculated by exponential fitting in the Arrhenius plot of Fig. 10, based on the method in Ref. [13]. Calculated defect parameters are shown in Table 4. Peaks #1, #2, and #3 had energy levels of E$_C$ − 0.36, E$_C$ − 0.47, and E$_C$ − 0.68 eV, respectively, where E$_C$ corresponds to the edge of the conduction band. Peak #3 is Z$_{1/2}$, which is the main defect of the 4H−SiC epi-layer and is known to originate in carbon vacancies. Considering that the concentration of as-grown epi-layer was $0.3-2 \times 10^{13}$ cm^{-3} [12], the Z$_{1/2}$ concentration of samples was increased by in-core neutron irradiation. Peak #2 is the same kind
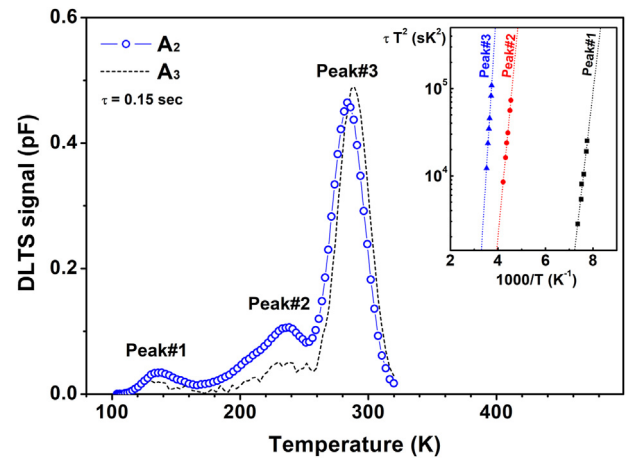

Fig. 10. Deep-level-transient spectra (DLTS) of samples A$_2$ and A$_3$. Arrhenius plot is shown in box.

Table 4
Defect parameters of in-core neutron-irradiated 4H−SiC.

Peak	Defect energy level (eV)	Electron-capture cross-section (cm−2)	Defect label
#1	E$_C$–0.36	$5.4 \times 10{-}11$	
#2	E$_C$–0.47	$7.8 \times 10{-}16$	E5 [14], EH1 [15].
#3	E$_C$–0.68	$2.0 \times 10{-}14$	Z1/2 [16,17]

Table 5
Defect densities of samples A_2 and A_3.

Sample	Defect density (10^{14} cm^{-3})		
	Peak #1	Peak #2	Peak #3
A_2	1.16	4.42	4.08
A_3	0.40	3.04	3.70

of defect as E_5 in Ref. [14] and EH1 in Ref. [15], taking into account their similar parameters; it is an intrinsic structural defect due to the displacement of Si or C atoms. Peak #1 has very high cross-section and has never been previously reported in experiments using electron- or ion-beam-irradiated 4H–SiC. It may be related to the phosphorus generated by the reaction $^{30}Si(n,\gamma)^{31}Si \rightarrow {}^{31}P + \beta^-$ ($T_{1/2} = 2.62$ h). This would be a major contributor to carrier-density reduction after in-core neutron irradiation. Table 5 shows the estimated defect densities of A_2 and A_3. The concentration of all defects was reduced with the 1700 °C heat treatment. As the annealing time doubled, the defect densities of peaks #1, #2 and #3 decreased to 34%, 68%, and 91%, respectively. This proves that defect recovery by thermal annealing is faster when the defect level is shallower.

4. Conclusion

In this study, recovery of neutron-induced defects on a 4H–SiC epitaxial layer by thermal annealing was investigated. The reverse-bias C–V characteristics confirmed strong charge compensation caused by uniformly distributed defects in a 4H–SiC epitaxial layer irradiated by neutrons with fluence 1.3–2.7 $\times$ 10^{17} cm^{-2}. The compensation was reduced by 1700 °C annealing, and the electrical characteristics became somewhat closer to those of the bare sample. The zero-bias capacitance and forward bias C–V showed time-dependent recovery behavior with annealing time. Every irradiated and 1700 °C-annealed sample showed a typical diode I–V curve, implying little or no functional degradation as a diode.

In addition, we used DLTS measurements to analyze neutron-induced damage to the crystal structure of the epi-layer and the effects of annealing. Three defect-state energy levels were found, with energies $E_C - 0.36$ (peak #1), $E_C - 0.47$ (peak #2), and $E_C - 0.68$ eV (peak #3), respectively. Peaks #2 and #3 were identified as intrinsic defects; peak #1, reported here for the first time, is probably phosphorus-related defect. The concentration of all defects decreased with 1700 °C annealing and showed a faster recovery tendency at shallower defect levels. However, even the samples annealed at 1700 °C for 2 h still had many defects, inducing a carrier reduction of ~50% compared to a non-irradiated sample.

For in-core application of SiC, further study of annealing recovery at temperatures >1700 °C is required. The present experimental results lay the groundwork for such follow-up studies.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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