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Design of A High-Speed Data Transmission System for Satellite Ground Inspection Trial

Hao Sun, Dae-Ki Kang*

Department of Computer Engineering, Dongseo University, Busan, Korea
sunhao5129@gmail.com, dkkang@dongseo.ac.kr

Abstract

A high-speed data transmission system is designed for the ground inspection equipment of satellite measurement and control. Based on USB2.0, the system consists of interface chip CY7C68013A, programmable logic processing unit EP4CE30F23C8, analog/digital and digital/analog conversion units. The working principle of data transmission is analyzed, and the system software logic and hardware composition scheme are detailed. The system was utilized to output/capture and store specific data packets. The results show that the high-speed data transmission speed can reach 38MB/s, and the system is effective for satellite test requirements.

Keywords: *Data Transmission, FPGA, LabVIEW, Measurement Equipment of Satellite.*

1. Introduction

An essential aspect of space communications, satellites provide a variety of voice, image, and data communication services. Satellites are widely used in weapons systems, remote sensing systems, navigation and positioning systems, manned spaceflight, and deep space exploration missions [1]. They provide high confidentiality, robust jamming resistance, and high survivability in wartime environments. Ground-based telemetry and control (G/T) equipment play a vital role in the development and testing of satellites. They enable the testing and exchange of specific remote commands, uplink data, telemetry signals, and range, velocity, and orbit tracking information before the satellite is launched into orbit. The functioning of the ground-based telemetry and control equipment can reflect the health status of the satellite post-deployment, to an extent.

With the development of large-scale integrated circuits, micro-electro-mechanical technologies, new materials and processes, the trend today is to miniaturize, quantify, shorten development cycles and increase functionality [2]. Currently, G/T equipment for satellite models is shifting towards universality due to

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Corresponding Author: dkkang@dongseo.ac.kr
Tel: +82-51-320-1724, Fax: + 82-51-327-8955
Professor, Department of Computer Engineering, Dongseo University, Busan, Korea

challenges such as maintenance, extended development cycles and lack of scalability [3]. The data transmission system serves as a critical component of ground-based telemetry and control equipment, which is integral to universal development processes. Its attributes include high speed, electromagnetic shielding, hot-swapping capabilities, and distortion-free performance. Technical term abbreviations will be explained upon their first use. Citations will follow a consistent format, adhering to the style guide and footnote style. Our language choice remains united in its formality and objectivity, demonstrating the balanced and value-neutral approach of academic writing.

Currently, the primary data transmission methods for ground telemetry and control (G/T) equipment are serial and network interfaces. RS-422/485 is the most widely used option for serial interfaces. The maximum transmission rate for data on serial ports is often limited to 100 Mb/s or below, and they can usually only connect to around 30 devices [4]. In contrast, Ethernet has a transmission rate of up to 1 Gbit/s and can cover distances of up to 500m [5]. Nonetheless, neither Ethernet nor serial ports support hot-swapping. USB 2.0 is a new type of serial port connection. It has become widely used in various fields due to its fast data transfer, plug-and-play capability, small size, portability, and easy expandability. With a maximum data transfer rate of 5 Gb/s, it can connect up to 126 devices via interfaces. Compared to other computer buses, USB 2.0 offers numerous advantages in various aspects.

2. Related Theory

2.1 The principle of data transmission system

Ground-based telemetry and control (G/T) equipment obtains information about the working conditions and various operational parameters of each subsystem of the satellite through telemetry, telecommand, and data transmission. Pulse Code Modulation (PCM) is commonly used for satellite telemetry/telecommand. The PCM telemetry/telecommand system formed by the interaction between the satellite and ground-based telemetry and control equipment is illustrated in Figures 1 and 2.

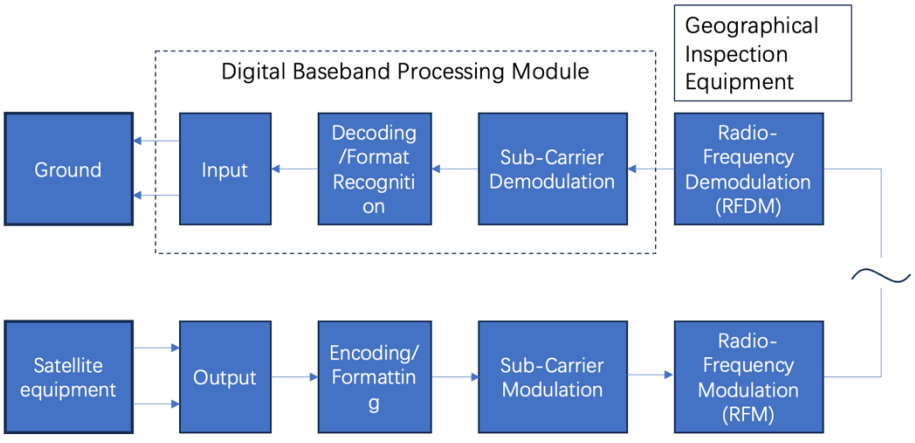

Figure 1. PCM telemetry system for satellite and ground inspection

The onboard computer on the satellite preprocesses telemetry information received from various subsystems and sensors. Subsequently, it frames this information and sends it to the onboard telemetry and

control unit via a serial port. The telemetry and control unit organizes the formatted data into a unified format and transmits it after modulation through the radio frequency (RF) channel [6]. Ground-based telemetry and control equipment receive the uplink and downlink data from the satellite through wired or wireless means.

After signal reception, the ground-based telemetry and control equipment utilize their own front-end radio frequency module to filter and perform corresponding low-noise amplification operations on the signal. Following down-conversion processing, the signal enters the filtering and automatic gain control module in the intermediate frequency (IF) form. Through signal processing, the data ultimately enters the baseband section of the ground-based telemetry and control equipment for analog-to-digital conversion (ADC) sampling.

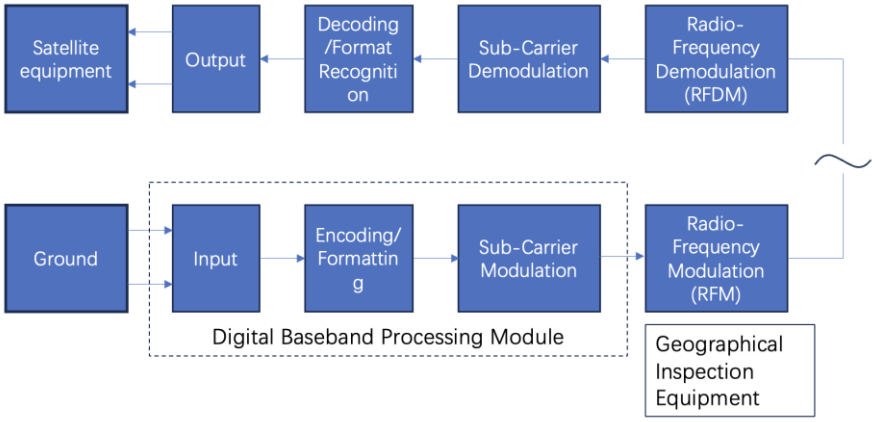

Figure 2. PCM Remote Control System for Satellite and Ground Inspection

Within the ground-based telemetry and control equipment, specific commands or data signals are sent to the digital baseband processing module of the equipment via the host computer. The ground-based telemetry and control equipment encode and output baseband signals, and the intermediate-frequency (IF) carrier is modulated by a modulator (either digital or analog) and then up-converted to a microwave radio frequency signal. The radio frequency signal is ultimately transmitted to the satellite through wired or wireless means after passing through a power amplifier.

The high-speed data transmission system is implemented based on the digital baseband processing module of the ground-based telemetry and control equipment. In addition to data transmission, the digital baseband processing module is also used for data encoding/decoding, modulation/demodulation, etc. Here, we will specifically analyze the functionality related to high-speed data transmission.

2.2 Design of data transmission system

The hardware of the data transmission system consists of analog-to-digital and digital-to-analog conversion circuits, programmable logic processing units, USB2.0 interface circuits, etc. The software includes firmware programs within the interface chip, computer-connected host software, interface chip driver programs, and applications on the host computer for controlling data transmission and collection. The uplink and downlink analog signals from the satellite are affected by external physical factors and are converted into a usable analog electrical signal according to a certain pattern [7], as illustrated in Figure 3.

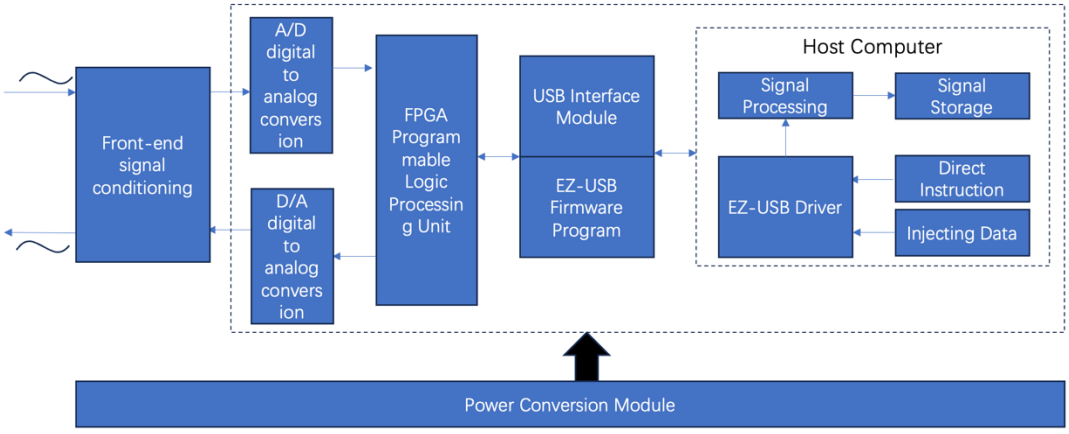

Figure 3. Block diagram of data transmission system structure

2.3 Hardware Circuitry Design

■ **A/D analog-to-digital converter circuit**

The analog-to-digital conversion circuit used in the high-speed data transmission system is constructed based on the AD7606 chip, which has a 16-bit resolution and a sampling rate of 200 kSPS (thousand samples per second). The design of this successive approximation-type ADC chip is characterized by high conversion speed and low power consumption. It allows synchronous sampling of 8 analog input channels. The chip integrates a 2.5V reference voltage source, analog multiplexer, input amplifier, overvoltage protection circuit, and second-order analog anti-aliasing filter. It also features high-speed serial and parallel interfaces for convenient communication with the CPU. With a 200 kSPS sampling rate, the chip exhibits a 40 dB anti-aliasing suppression characteristic, and its flexible digital filters can effectively improve signal-to-noise ratio (SNR) and reduce bandwidth. This type of ADC chip is commonly applied in high-speed data acquisition systems, instruments, and control systems.

The AD7606 features true bipolar analog inputs with ranges of ±10 V, ±5 V, analog input clamp protection, input buffers with 1 MΩ analog input impedance and second-order anti-alias analog filters, on-chip precision reference voltage sources and reference buffers, and digital filter oversampling. The ESD rating on the analog input channels is 7kV, the SNR value is 95.5dBSNR, the THD value is -107dB, and the power consumption is 100 MW in low-power mode and 25 MW in standby mode.

■ **D/A digital-to-analog converter circuit**

The digital-to-analog conversion circuit is constructed using the AD9708 chip introduced by AD. This chip is an 8-bit, 125 MSPS (million samples per second) low-power digital-to-analog converter with a built-in 1.2V reference voltage and differential current output. The digital-to-analog conversion circuit, centered around the DA chip, achieves the conversion of digital signals through a 7th-order Butterworth filter, amplitude adjustment circuit, and output interface. The bandwidth of the 7th-order Butterworth filter is 40 MHz. After the filtering process, two AD8056 chips are used to implement functions such as differential-to-single-ended conversion and amplitude adjustment, thereby maximizing the performance of the conversion circuit. Currently, this chip is commonly used in communication, signal acquisition, and other applications.

The AD9708 offers the following advantages: fast update rates up to 125 MSPS, linearity up to 1/4 LSB

for DNL and 1/4 LSB for INL, differential current output SINAD (5MHz output) up to 50dB, and power consumption of only 175 mW (5V to 45mW at 3V).

■ **Programmable Logic Processing Unit**

The FPGA chosen for this application is from ALTERA's Cyclone IV series. This series of FPGAs is developed by ALTERA as a low-cost, low-power programmable logic processing unit with abundant logic resources. It features approximately 30k logic elements, 594k bits of embedded memory, 66 embedded 18x18 multipliers, 4 PLLs (Phase-Locked Loops) for general use, 20 global clock networks, 8 I/O blocks, and a maximum of 532 user I/O. Considering the specific requirements of this project, the selected FPGA model is EP4CE30F23C8. Given the characteristics of SRAM-based FPGAs, this chip can achieve different logic functions by configuring different data. Considering the actual needs of this project, the specific model of FPGA selected is EP4CE30F23C8. Given the characteristics of SRAM-type FPGAs, the chip can be configured with different data to achieve different logic functions.

■ **USB interface circuit**

The EZ-USB FX2LP (CY7C68013A) from Cypress Semiconductor is a highly integrated, low-power USB 2.0 microcontroller. The controller integrates multiple units, including an 8051 microcontroller, USB 2.0 transceiver, programmable peripheral interface, serial interface engine (SIE), and more. This integration enables a compact size, low power consumption, high transfer rates, and a shortened development cycle. The communication process between EZ-USB and the FPGA involves asynchronous Slave FIFO read and write operations. The specific interface is illustrated in Figure 4.

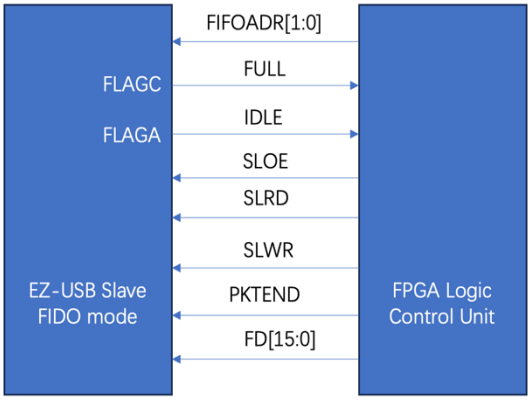

Figure 4. EZ-USB Interface Pin Diagram

The write clock is generated by the SLWR pin, and FD is the data bus. The FPGA controls the FIFOADR and PKTEND pins and can simultaneously read the FIFO FULL and EMPTY flags from EZ-USB during data writing [8]. The read clock is generated by the SLRD pin, and FD is the data bus. The FPGA controls the FIFOADR, SLOE, and SLRD pins, and can also read the FIFO FULL and EMPTY flags from EZ-USB during data reading. The FIFOADR address register selects the use of EP2 for Bulk out and EP6 for Bulk in.

2.4 Software design

■ **FPGA software**

To perform asynchronous Slave FIFO reads and writes, the external FPGA needs to process a series of

events, Figure 5 shows the asynchronous Slave FIFO read/write state machine for the external host.

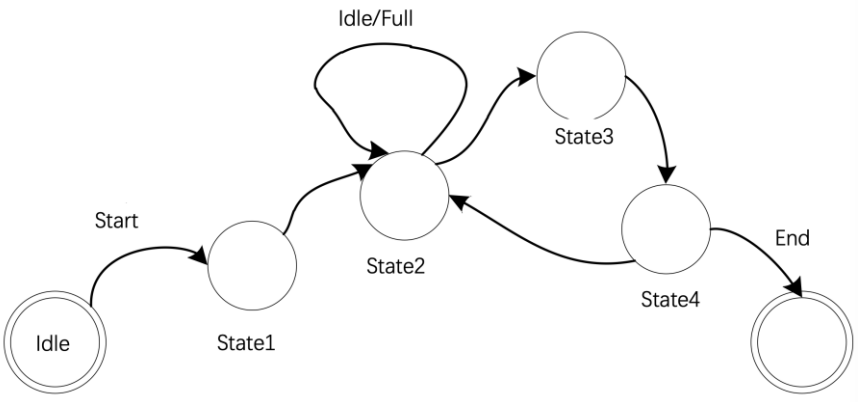

Figure 5. Schematic diagram of asynchronous read/write state machine

The FPGA is initially in an idle state. If a read/write condition occurs, it transitions to State 1. State 1 points to the OUT FIFO or IN FIFO, triggers FIFOADR, and transitions to State 2. In State 2, it checks the empty/full flags. If the flag is false, it transitions to State 3; otherwise, it stays in State 2. State 3, triggered by SLRD/SLWR, collects/drives data on the data bus and then transitions to State 4. In State 4, if there is more data to read/write, it transitions to State 2; otherwise, it transitions to the idle state.

■ Firmware program

In USB interface design, firmware programming is at the core of the design tasks [6]. The firmware program is responsible for tasks such as computer recognition of USB devices, communication between the host computer and the USB device, handling USB device requests, and re-enumeration. When the device is connected to the computer, the firmware is loaded according to the process shown in Figure 6.

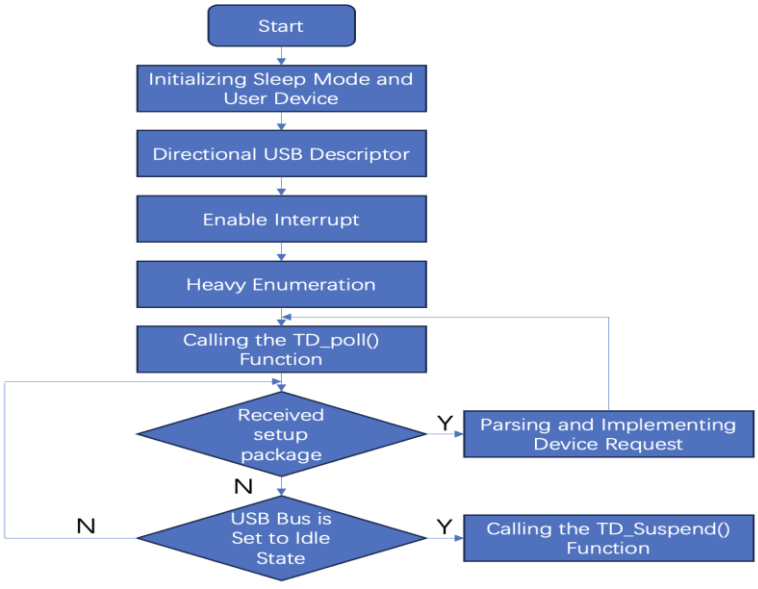

Figure 6. Firmware program framework flowchart

To achieve control over the USB device, loading a custom firmware program is necessary. Setting IFCONFIG to 0xCB uses the internal 48MHz clock, configuring EP2CFG and EP6CFG to 0xA0 and 0xE0 respectively activates Endpoint 2 for output and Endpoint 6 for input. Setting PINFLAGSAB and PINFLAGSCD to 0x98 and 0xFE, respectively, configures FLAGA as the empty flag for Endpoint 2 and FLAGC as the full flag for Endpoint 6.

■ **Program driver**

Driver installation is guided by INF files. INF files serve as a medium to record USB device information in the computer system registry. USB device driver files typically appear in the .sys format. After installing the corresponding driver, this file and its associated INF file are mapped into the relevant folders. When a USB device is connected to the computer, the operating system detects the connection and sequentially locates INF files that match the connected device.

NI-VISA is a software tool developed by National Instruments (NI) for users working with LabVIEW, a graphical interface design software. NI-VISA facilitates the creation of various drivers and supports testing. It can control two types of USB devices: USB INSTR and USB RAW. Utilizing NI-VISA to create USB driver settings is illustrated in Figure 7.

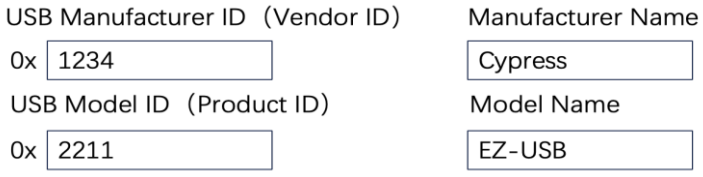

Figure 7. USB Device Information

Using the Cypress Control Panel EZ-USB Control Panel to download the firmware program into the USB chip, and creating a driver with NI-VISA, communication between the host computer and the high-speed data transmission system can be achieved through a LabVIEW program. The program flow is illustrated in Figure 8.

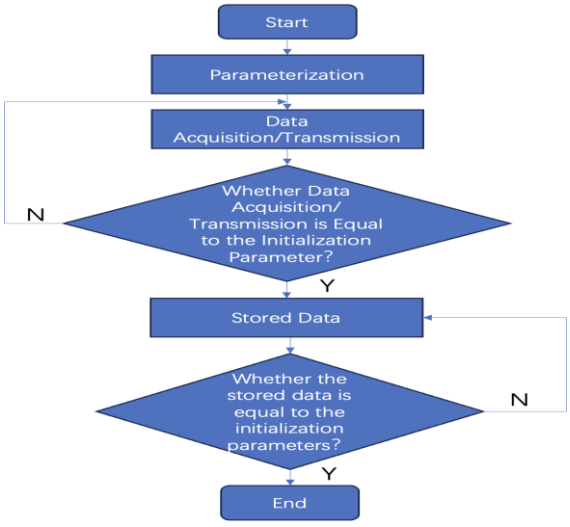

Figure 8. Flow chart of high-speed data transmission

Execution of the upper computer program, the first parameter settings, including the selection of USB devices, the storage path, USB acquisition/sending device number, factory number and so on. Based on the set parameters, the data high-speed transmission system begins to work, the work process, you can perform the corresponding instructions or data sent, but also the lower computer uploaded data for high-speed acquisition, the data collected or sent with the set value of the data is consistent with the data to save, and then close the process.

3. Experiments and analysis of results

Figure 9. Schematic of the ground test system

As shown in Figure 9, the wireless electromagnetic wave signal transmitted from the ground is received through the antenna, and the signal is received by the ground terminal and then entered into the high-speed data transmission system after demodulation and descrambling of the signal. The operation of the equipment is operated remotely through the ground test software, and the data is directly stored in the upper computer after data acquisition. Among which, the USB connection mode is set as EZ-USB2.0 in the data acquisition system, the connection device is selected, the data length is selected as 1024 bits, and the Slave FIFO is selected for continuous acquisition.

Through the Bulkloop loop, the transfer speed of EZ-USB was tested. Using the host computer, 60,000 data packets were transmitted via USB2.0 to the digital-to-analog converter (DA). The analog-to-digital converter (AD) then transmitted the source data back to the host computer via USB2.0 input. After calculation, the transfer rate was found to be above 38MB/s, as shown in Figure 10.

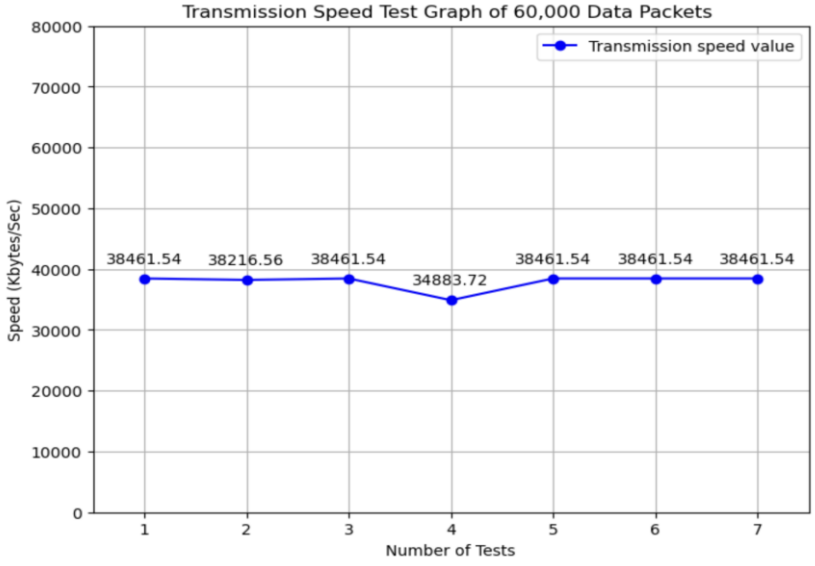

Figure 10. Transmission speed test graph

4. Conclusion

A high-speed data transmission system is designed for ground inspection of satellite measurements and control. The system possesses small size, scalability, and generalization. The device operates based on the principle of data transfer between the satellite and ground inspection equipment. The controller uses FPGA software algorithm to design the data acquisition board as the core and realize the development of portable satellite ground inspection equipment with general-purpose functionality. These improvements have been made through simple interface editing and support for functional expansion to reduce electromagnetic interference. Technical terms are explained when first used. To improve the data transmission rate, the system firmware program implements USB2.0 endpoint parameter configuration. Additionally, the NI-VISA driver provides a programming interface to control the USB interface in the NI application development realm, which offers interface independence, platform portability and ease of use. Consistent citation style and grammar accuracy have been ensured. The VISA commands are identical, irrespective of whether the instrument uses a serial, GPIB, or USB interface, as long as the ASCII string is written to the message-based instrumentation. Therefore, the NI-VISA driver facilitates the data transfer between the LabVIEW program and the lower computer more efficiently, and provide a stronger foundation for future research in the field of high-speed data transmission for satellite inspection systems.

Acknowledgement

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