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Simulation-based P-well design for improvement of ESD protection performance of P-type embedded SCR device

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Abstract

Electrostatic discharge (ESD) protection devices of P-type embedded silicon-controlled rectifier (PESCR) structure were analyzed for high-voltage operating input/output (I/O) applications. Conventional PESCR standard device exhibits typical SCR characteristics with very low-snapback holding voltages, resulting in latch-up problems during normal operation. However, the modified device with the counter pocket source (CPS) surrounding N^+ source region and partially formed P-well (PPW) structures proposed in this study could improve latch-up immunity by indicating high on-resistance and snapback holding voltage.

Key words : Electrostatic discharge (ESD), P-type embedded silicon-controlled rectifier (PESCR), counter pocket source (CPS), partially formed P-well (PPW), latch-up immunity, snapback holding voltage

Ⅰ. Introduction

When the electrostatic discharge (ESD) occurs in microchips for display driver, problems such as electronic devices causing malfunctions and physical damage can lead to degradation of thermal and electrical performance in the microchips such as LDI (LCD driver IC) and DDIC (display driver IC) chip. Various MOSFET structures have been introduced for stable ESD protection performance, among which N-type MOSFET devices with double diffused drains (DDDNMOS) are difficult to realize the stable ESD protection characteristics at high voltages. This is reported to be due to non-uniform current flow within the device [1, 2]. Very strong snapback characteristics cause current crowding, resulting in melting damage. Therefore, the self-protection techniques using DDDNMOS devices are practically impossible and alternatives need to be studied.

Among the ESD protection devices reported so far, the silicon-controlled rectifier (SCR) device operating at high voltages has a high current immunity level and is an attractive candidate for ESD protection device [3, 4]. However, the high-voltage operating SCR device has the disadvantages of being very vulnerable to latch-up during normal operation. Various studies, such as gate coupled SCR (GCSCR), high holding current SCR (HHI-SCR) and low voltage triggering SCR (LVTSCR), have been reported to solve these

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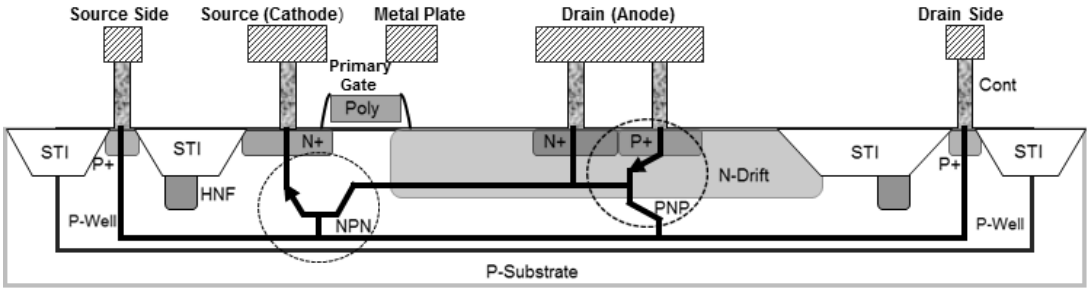


Fig. 1. Structural and SCR behavior mechanisms for high-voltage operating STD device. The P^+ diffusion (BF_2, 25 KeV, 3.0×10^{15} cm^{-3}) area was embedded to the right of the N^+ drain to form a part of the anode (drain) electrode. PNPN-SCR device consisting of a vertical PNP-BJT and a horizontal NPN-BJT as indicated by a round circle.

problems [5, 6]. The SCR device is vulnerable to latch-up because the on-resistance (R_{on}) in the high-current region is too low for the snapback holding voltage. Thus, a method is needed to increase the on-resistance in the high-current region. The author suggested that the addition of counter-pocket source (CPS) structures to SCR standard devices could increase snapback holding voltage and on-resistance in previous studies [7].

In general, the PESCR device acts as an inter-connected SCR between NPN-BJT (bipolar junction transistor) in the horizontal direction and PNP-BJT behavior in the vertical direction, responding to ESD stress currents. When the PESCR device is operated, a low-resistance current path is formed between the drain (anode) and the source (cathode) that is widely distributed in vertical direction. These low-resistance current paths result in a smaller on-resistance, so that both snapback holding voltage (V_h) and thermal breakdown voltage (V_{tb}) represent very small values. These characteristics cause the snapback holding voltage of the PESCR device to be lower than the operating voltage, resulting in a problem that is susceptible to latch-up. There is also a problem with poor linearity at the level of current immunity because the thermal breakdown voltage is less than the triggering voltage. This problem is caused by on-resistance of the PESCR device being too small. Therefore, the work of making the snapback holding voltage greater than the operational voltage by increasing the on-resistance (V_{op}+V〈V_h), and increasing the thermal breakdown voltage above the triggering voltage (V_{tr}=V_{tb}) must first be carried out in order to achieve stable ESD protection performance using PESCR devices.

In this paper, the author propose the PESCR devices with optimal P-well structure through simulation analysis to solve the above-mentioned problems of these devices, and to satisfy the necessary sufficient conditions (V_{op}+V〈V_h, V_{tr}=V_{tb}) for stable ESD protection after the modification of P-well structure in the PESCR standard device.

II. Device structure and simulation method

2.1 Device structures

Fig. 1 illustrates the schematic diagram and SCR behavior mechanisms of the PESCR_Std standard device (*hereafter referred to as* STD). The NPN-BJT in the horizontal direction and the PNP-BJT in the vertical direction act as an inter-connected SCR device to show the operating mechanism corresponding to the ESD stress current as an arrow.

Fig. 2 shows the structure of the PESCR_CPS devices (*hereafter referred to as* CPS) to be considered in this study based on the STD devices. Fig. 2(a) shows a structure in which the process of counter pocket source (CPS) ion implantation (boron, 180 KeV, 8.5×10^{13} cm^{-3}) of P-type has been added to surround the source (cathode) of the N^+ diffusion area, which increases the on-resistance to make the snapback holding

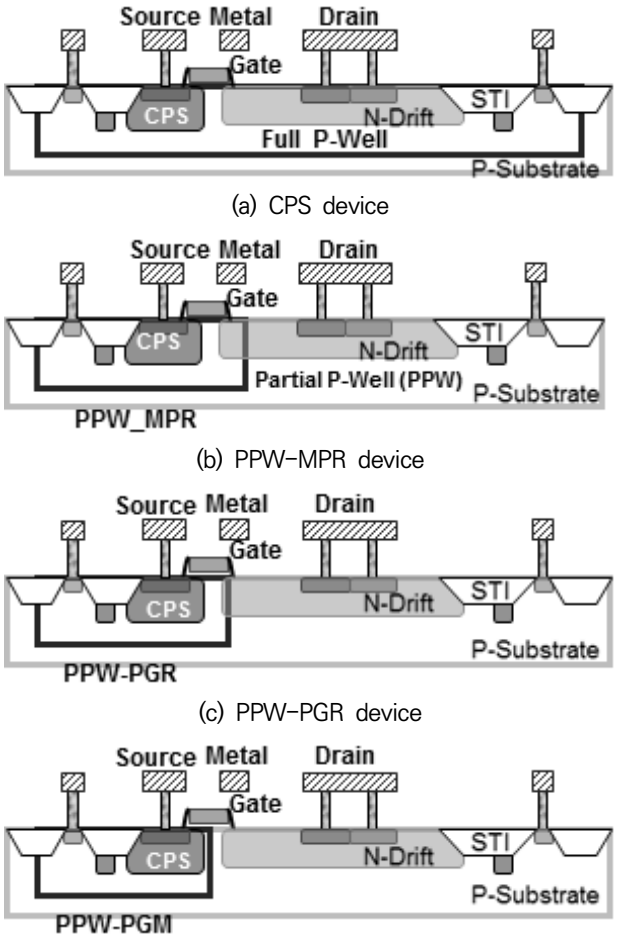


Fig. 2. Schematic diagrams of modified devices with different partial P-well (PPW) structure in the CPS device.

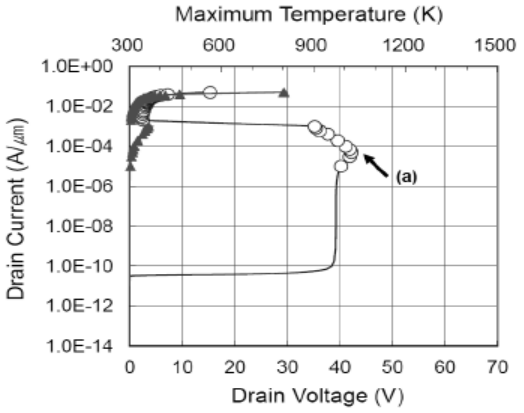
voltage greater than the operational voltage, and the thermal breakdown voltage can also be increased beyond the triggering voltage. Fig. 2(b), (c) and (d) are designed to modify the device structure according to where the right edge of the partial P-well (*hereafter referred to as* PPW) is located (or the size of PPW area), which is partially formed based on the CPS device. This is an attempt by the prediction that changing the full P-well structure to a PPW structure could increase triggering voltage, snapback holding voltage, and thermal breakdown voltage, where MPR is the structure in which the right end of PPW is located on the right side of the metal plate *(hereafter referred to as* PPW-MPR*),* the PGR is the right end of the PPW is located on the right end of the primary gate *(hereafter referred to as* PPW-PGR*),* and the PGM is the structure in which the right end of the PPW is located on the middle of the primary gate (*hereafter referred to as* PPW-PGM*).*

2.2 Method of simulation analysis

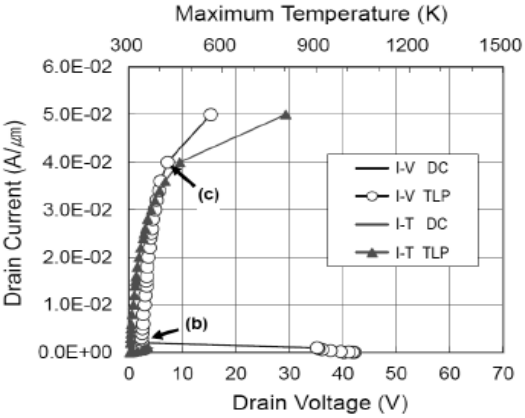
The simulation methods used in this study were the same as those previously published by this research team [1-2], and the current-voltage (*I-V*) characteristics of PESCR devices were analyzed by two-dimensional process and device simulation. The device was constructed by applying to the high voltage (HV) process technology (@ 0.18um_30V, active width = 200um) using the process simulator TSUPREM-4. Device characteristics were analyzed using DESSIS device simulator. Non-thermal DC simulation without considering 2D thermal effects was performed in low current regions with lower current density than 1×10^{-5} A/μm. In high current regions with higher current density than 1×10^{-5} A/μm, 2D simulation of the mixed mode transient (MMT) with thermal effects was analyzed. To simulate the ESD stress of the human body model (HBM), the MMT simulation was performed by applying trapezoidal current pulses with a rise time of 10 ns and a duration of 100 ns. The transmission line pulse (TLP) test system, Barth 4002, was used to monitor the high-current response of devices. During the measurement, the rise time and duration time of pulse were maintained at 10 ns and 100 ns, respectively.

Ⅲ. Results and discussion

Table 1 compares the typical I-V results of the proposed PESCR devices with different partial P-well (PPW) structures and the conventional standard SCR device. The positions of the triggering and snapback holding voltages can be confirmed on the I-V curve using this table. Fig. 3 shows the DC simulation and TLP test results



(a) off-state leakage current. [a: triggering]



(b) on-state high current.
[b: snapback holding, c: thermal breakdown]

Fig. 3. Comparison of Simulation and TLP test of the STD device.

of the STD device divided into (a) off-state leakage current and (b) on-state high current regions. The TLP *I-V* characteristics data shown in Fig. 3(b) showed a high current immunity level, which shows the excellent characteristics of the ESD protection. However, this device showed very low snapback holding voltage and low on-resistance. For STD devices, because the on-resistance was small during NPN-BJT operation, no voltage drop occurred until the PNPN-SCR operation started in the first snapback holding point of NPN-BJT device. Therefore, only the first triggering appeared in the overall I-V characteristics, and the second triggering did not. Meanwhile, for the current-temperature *I-T*) curve shown in Fig. 3 (b), at a maximum temperature of 300 to 500 K, the drain current increased rapidly and stopped at 50 mA near 800 K. This value of 50 mA corresponds right before the thermal breakdown occurs, and the distribution of the electric field is shown in Fig. 4(c).

Fig. 4 shows the contour distribution of the current density and the electric field within the high current limits at the (a) triggering point, (b) snapback holding point, and (c) thermal breakdown point of the STD device. At the triggering point corresponding to Fig. 4(a), the high field region induced by the depletion of carrier was formed along the boundary area of N^- drift/high P-type well. It could be seen that only the lateral NPN-BJT behavior is occurring from the beginning of the triggering point. This is judged to interfere with the surface current path between the N^+ drain (anode) and the N^+ source (cathode) diffusion region. However, when the STD device entered the (b) snapback holding point or (c) high current region, PNP-BJT behavior in the vertical direction was also initiated and combined with NPN-BJT behavior in the lateral direction resulted in PNPN-SCR behavior. Thus, the current path represented a widely distributed U-type path. High density electrons were injected into the channel region from the N^+ cathode diffusion

Table 1. Comparison of conventional standard SCR device and proposed PESCR devices with partial P-well (PPW) structures.

Description of TLP Parameters [Unit]	(a) STD		(b) CPS	(c) MPR	(d) PGR	(e) PGM
	Simulate	TLP				
1-st Triggering Voltage [V]	41.9	37.0	45.1	43.5	-	-
1-st Snapback Holding Voltage [V]	2.3	6.6	43.3	43.3	-	-
2-nd Triggering Voltage [V]	-	-	46.3	57.8	61.4	70.8
2-nd Snapback Holding Voltage [V]	-	-	37.5	46.7	52.7	58.3

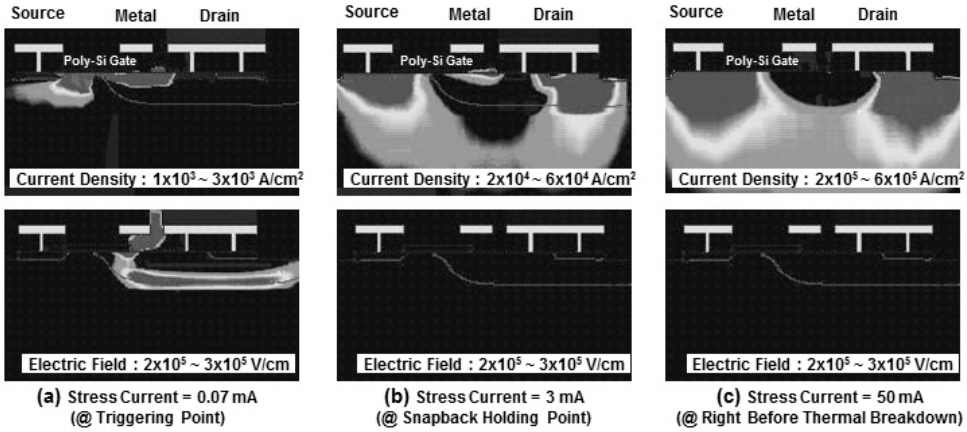
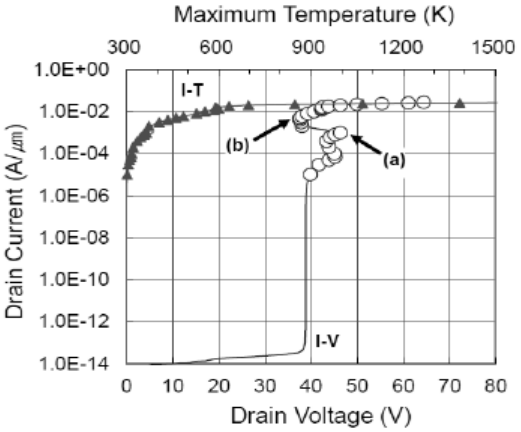


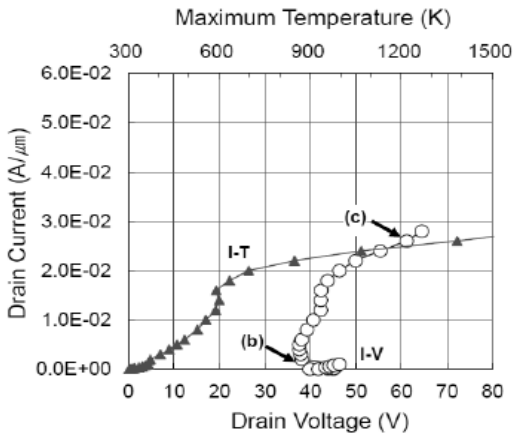
Fig. 4. Contour distribution of the current density and electric field of the STD device. (a) triggering point, (b) snapback holding point, and (c) thermal breakdown point. These points correspond to a, b, and c marked in Fig. 3, respectively.

region to induce deep electronic channeling under the gate. Thus, the boundary area of P-well and N^- drift, which was originally doped at low concentrations, was completely blocked by injected free electrons, indicating that the boundary line of N^- drift/P-well had almost disappeared. As shown in the contour distribution (Fig. 4b and 4c) of the electric field, the field-free regions were formed in the entire current path between the cathode and anode. In other words, the low holding voltage and the low on-resistance are described in terms of the wide distribution of current paths between the two electrodes, where no field is formed. Base push out (or Kirk effect) induced by high electron injection and resulting low V_h and low R_{on} have already been published in the preceding work [7].

Fig. 5 shows the *I-V* characteristics of modified CPS device. The first triggering point and the second triggering point are clearly indicated by the double snapback phenomenon. As described earlier, the avalanche breakdown voltage did not increase significantly, but it was able to reduce the leakage current, and the snapback holding voltage could be increased above the operating voltage and the thermal breakdown voltage could be increased above the triggering voltage, therefore inhibiting the occurrence of latch-up. In other words, the effect of the additional CPS ion implantation on the STD device will result in a higher on-resistance, higher snapback holding voltage, and higher thermal breakdown voltage than the STD device because of the presence of



(a) off-state leakage current [a: triggering]



(b) on-state high current
[b: snapback holding, c: thermal breakdown]

Fig. 5. Current-voltage characteristics of CPS device.

a strong high electric field area on the path of current flow in the high current region. For the *I-T* curve shown in Fig. 5 (b), the drain current tended to increase linearly in the maximum temperature range from 300 K to 600 K, then slowly increasing from 20 mA to 26 mA after 600 K. This value of 26 mA corresponds just before the thermal breakdown occurs, and the distribution of the electric field is shown in Fig. 6(c).

Fig. 6 shows the current density and electric field distribution of the CPS device. Here, the contour distribution data corresponding to the high current region near the (a) triggering point, (b) snapback holding point and (c) thermal breakdown point provide a phenomenological explanation of the changes that are significantly different from the STD devices shown in Fig. 4.

In the BJT triggering point shown in Fig. 6 (a), the high field region induced by the depletion was formed along the boundary of the N^- drift/P-well area. This was qualitatively identical to the distribution observed in the STD devices. However, when the CPS device enters the snapback holding point corresponding to Fig. 6 (b), it can be seen that the high field region in the lateral direction which had disappeared from the STD device still remains due to CPS ion implantation. In other words, the high-density electrons in the lateral direction suddenly increased from the N^+ source region were weakened or blocked by CPS ion implantation, so no more base push-out phenomena occurred. The widely distributed U-type current path causes PNP-BJT behavior, so the PNPN-SCR behavior characteristics were initiated. However, the snapback holding voltage did not significantly decrease, as the high field region remained in the direction of the current path. As shown in Fig. 6 (c), when the anode current further increased to 26 mA/μm after the snapback holding state, the high electric field region along the N^- drift/P-well boundary line in the direction of the bottom gradually disappeared. However, it could be seen that the high field region along the lateral N^- drift/P-well boundary line has never disappeared. In addition, the newly created high field region was formed in the direction of the U-type main current path. These results may be explained by the effect of an abrupt increase in local maximum temperature and relatively high R_{on} in the high field region near the thermal breakdown point (c).

Fig. 7 compares the *I-V* characteristics of the PPW devices with different PPW structures proposed in this study. For the PPW_PGM devices shown in Fig. 7(c), the effects of CPS and PPW ion implantation caused the on-resistance of NPN-BJT to be increased again. As a result, the first snapback holding point during NPN-BJT operation may appear very weak or the snapback behavior itself disappears. In addition, it could

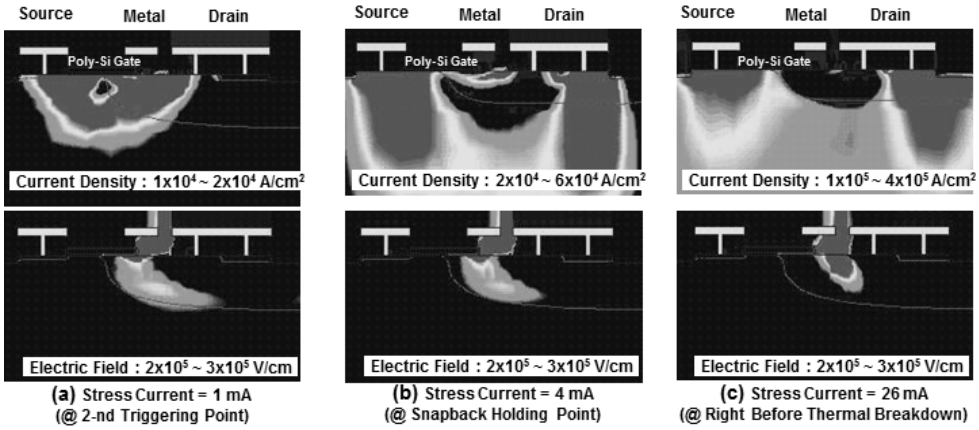
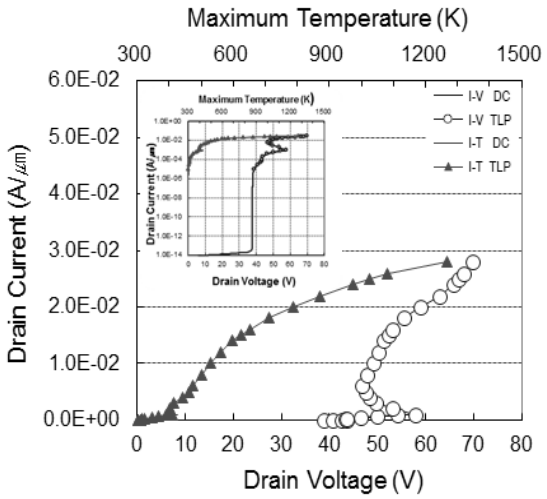
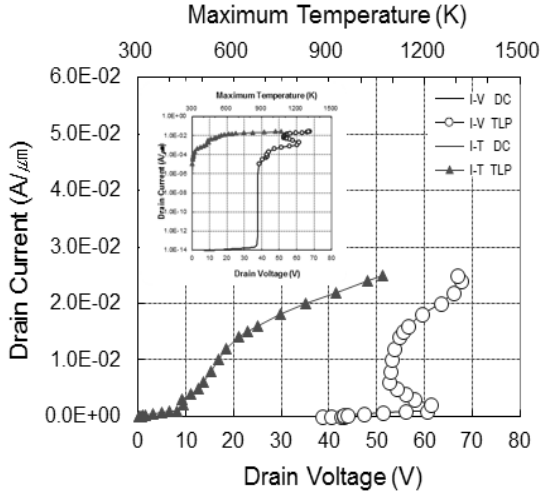


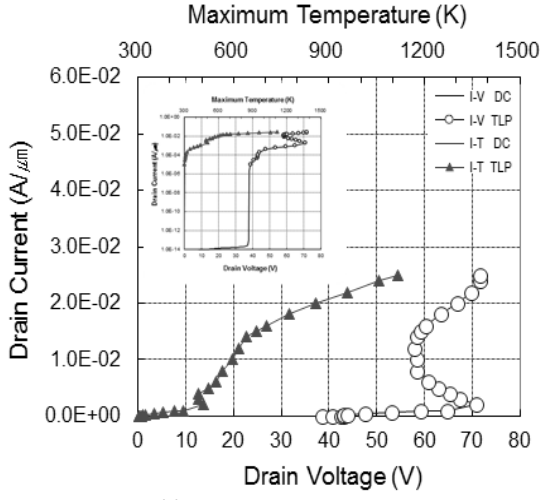
Fig. 6. Contour distribution of the current density and electric field of the CPS device. These points correspond to a, b, and c marked in Fig. 5, respectively.



(a) PPW_MPR device



(b) PPW_PGR device



(c) PPW_PGM device

Fig. 7. I-V characteristics of CPS_PPW device with different partial P-wells. The off-state graph is inserted into the on-state graph for comparison.

be seen that the voltage drop increases abruptly at the first snapback holding point when the PNPN-SCR behavior is initiated. As the above-entioned causes, it can be predicted that the double snapback phenomenon has disappeared from the PGR and PGM structures.

This can be clearly confirmed from the contour distribution of the current density and electric field shown in Fig. 8 and can be summarized as follows: In the overall *I-V* characteristics, it can be seen that the first triggering point is hidden, and the second triggering voltage is represented by a significant increase. For the case of *I-T* curve shown in Fig. 7 (c), the drain current in the maximum temperature range of 300 to 500 K showed a value close to zero. The drain current increased linearly and stopped at 24 mA near 1,100 K. This value of 24 mA corresponds right before the thermal breakdown occurs, and the distribution of the electric field is shown in Fig. 8(c).

Fig. 8 illustrates the current density and electric field distribution of PPW_PGM device. Fig. 8 (a) shows the stage of the transition from NPN-BJT behavior to PNPN-SCR behavior as a triggering point with a stress current of 2 mA. The triggering point at the PPW_PGM device corresponds to the secondary triggering point that appears at the CPS device. The high electric field region occurs along the N^- drift/P-well boundary, but it could be seen that the electric field in the horizontal direction remains stronger than in the vertical direction. The voltage drop between the drain and the source near the secondary triggering point is thought to have increased due to a high electric field region in the horizontal direction that exists while the NPN-BJT current is flowing. Fig. 8 (b) correspond to a snapback holding point with a stress current of 10 mA, and the contours of the current path and the high electric field region near the snapback holding point of the PPW_PGM device have shown qualitatively similar results to the CPS device. Fig. 8 (c) correspond to the stage before a thermal breakdown with a stress current of 24 mA, and

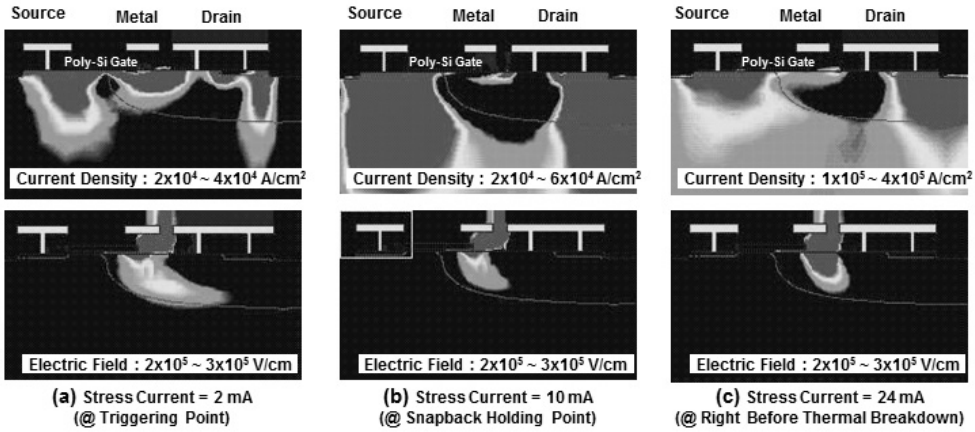


Fig. 8. Contour distribution of current density and electric field at PPW_PGM device with partial P-wells.

the contour distributions of the current path and the high electric field region of PPW_PGM device have shown qualitatively similar results to the CPS device.

In summary, the CPS device and PPW_PGM device were observed to have no qualitative difference in the contour distribution of the high electric field region and the current path in the high current region. The reasons why the voltage drop between the drain and the source of the PPW_PGM device is generally greater than the voltage drop of the CPS device are as follows: The PPW_PGM device shows that the high electric field in the horizontal direction remains relatively stronger in the high current region. It is estimated that this is due to the deeper distribution of the U-type current path, the main current path of the PNPN-SCR device in the high current region, which leads to a longer current path.

Ⅳ. Conclusion

In this paper, the P^+ diffusion layer was embedded to the right of the N^+ drain region to create the PNPN-SCR structure, and the ESD characteristics of CPS_PPW device with the different PPW structure were studied in order to solve the latch-up problem of the conventional STD device. The simulation results of the CPS_PPW device with changes in PPW area demonstrated that latch-up can be avoided by indicating significantly greater on-resistance and higher snapback holding voltages than the conventional STD device.

The simulation-based design methodology presented in this study shows that it is likely to be a solution to overcome the problems of high voltage operating ESD protection device based on the DDDNMOS structure. It was therefore confirmed that the modified devices of the CPS_PPW structure could be used as an ESD protection device for the I/O application of the high-voltage operating microchip used in display electronics. It is thought that attempts to verify and practicalize the methodology proposed in this study through TLP test pattern analysis with various technologies will be necessary in the future.

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