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Design of DC-DC Boost Converter with RF Noise Immunity for OLED Displays

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ABSTRACT

In this paper, we design a DC-DC boost converter with RF noise immunity to supply a stable positive output voltage for OLED displays. For RF noise immunity, an input voltage variation reduction circuit (IVVRC) is adopted to ensure display quality by reducing the undershoot and overshoot of output voltage. The boost converter for a positive voltage Vpos operates in the SPWM-PWM dual mode and has a dead-time controller using a dead-time detector, resulting in increased power efficiency. A chip was fabricated using a 0.18 um BCDMOS process. Measurement results show that power efficiency is 30% ~ 76% for load current range from 1 mA to 100 mA. The boost converter with the IVVRC has an overshoot of 6 mV and undershoot of 4 mV compared to a boost converter without that circuit with 18 mV and 20 mV, respectively.

KEY WORDS

DC-DC converter, boost, OLED, dead time controller, dual-mode switching.

1. INTRODUCTION

As the number of battery-operated mobile devices, such as smartphones, smart watches, and so forth, has rapidly increased, it has been necessary to develop highly efficient power management ICs (PMICs) to ensure long battery life. Among these PMICs, DC-DC converters are widely used in portable devices because they provide high efficiency [1–3].

Some techniques to increase power efficiency over a wide-load current range have been suggested using a dual mode, such as pulse frequency modulation (PFM) - pulse width modulation (PWM), pulse skip modulation (PSM) - PWM, and set-time variable PWM (SPWM) - PWM [3–5].

Current fluctuations due to periodic transmission and reception are introduced in wireless communication devices, which causes RF noise [6,7]. Voltage fluctuations due to RF noise cause overshoot and undershoot in the output voltage of the DC-DC converter, thereby degrading the output quality of the OLED display. Therefore, DC-DC converters for mobile devices are required to have RF noise immunity.

Furthermore, it is important to reduce power loss due to shoot-through current and body-diode conduction related to dead time. A conventional fixed dead-time controller has long enough dead time to prevent shoot-through current. However, dead time longer than necessary causes body-diode conduction, which in turn causes additional power loss [8,9]. Therefore, the optimal dead time is required to achieve high power efficiency over a wide load range.

In this paper, we design an RF noise-immune DC-DC boost converter with a dead-time controller for OLED displays. A positive voltage

Vpos is designed as a boost converter using the SPWM-PWM dual mode [5] to improve light load efficiency, and improves the efficiency in a small area by applying the dead-time controller using the dead-time detector. In addition, the overshoot and undershoot of the output voltage due to the inflow of RF noise are reduced by using an input voltage variation reduction circuit.

This paper is organized as follows: Section 2 presents the design of the proposed DC-DC boost converter with RF noise immunity for OLED displays. Section 3 shows the chip implementation and measurement results for the circuits. Section 4 draws conclusions.

2. Design of RF Noise-Immune DC-DC Boost Converter

In this section, an RF noise-immune DC-DC boost converter with a dead-time controller for OLED displays is proposed.

Figure 1 shows a block diagram of the proposed DC-DC converter with RF noise immunity for OLED displays.

The proposed converter is basically a SPWM-PWM dual-mode boost converter to increase power efficiency over a wide load range [5]. A dead-time controller in the gate driver block is combined to minimize the dead time of a P-N power transistor to improve power efficiency. In addition, an RF noise-reduction circuit is adopted to suppress the undershoot and overshoot of the output voltage.

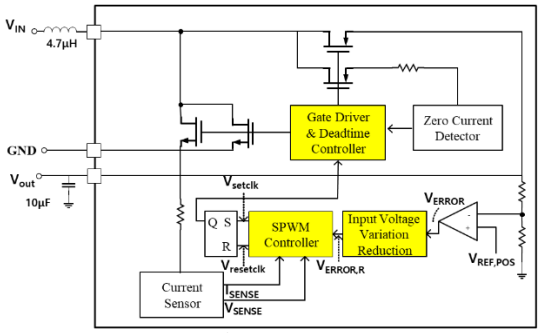


Figure 1. Block diagram of proposed DC-DC boost converter.

A. INPUT VOLTAGE VARIATION REDUCTION CIRCUIT

The fluctuation of the input voltage due to RF noise causes overshoot and undershoot of the output voltage, which deteriorates the output quality of the OLED display. In this subsection, an input voltage variation reduction circuit (IVVRC) is designed to attenuate input voltage fluctuations.

Figure 2 and Figure 3 show a circuit diagram and operation waveform of a proposed IVVR circuit, respectively. The proposed IVVRC consists of three current mirrors. A current proportional to the output of error amplifier is copied to the first current mirror, and a current proportional to the input voltage is copied to the second and third current mirrors. The voltage V_{ERROR} is generated by canceling the input current that has caused the fluctuation in the copied error amplifier's current.

$V_{ERROR-R}$ is used as a signal for generating the reset clock of the power transistor instead of V_{ERROR}, and when the input voltage is changed, the fluctuation range is reduced compared to V_{ERROR}. Due to this, the pulse width fluctuation of the switching signal of the power transistor is reduced compared to when V_{ERROR} is used, thereby reducing overshoot and undershoot of the output voltage.

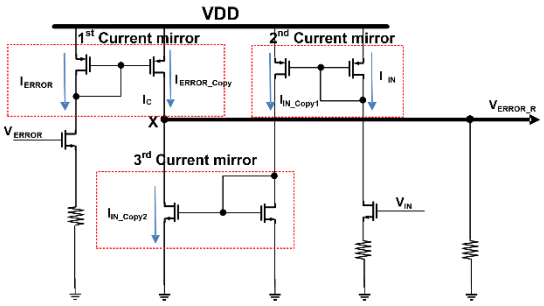


Figure 2. Proposed input voltage variation reduction circuit.

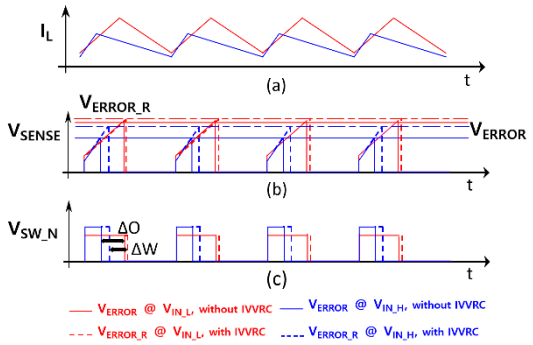


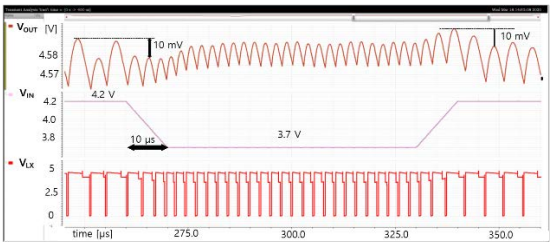
Figure 3. Timing diagram of input voltage variation reduction circuit: (a) inductor current (b) inductor current sensing voltage (c) switching voltage of NMOS power transistor.

Figure 3 shows timing diagrams of the RF noise-reduction circuit when a typical RF noise enters.

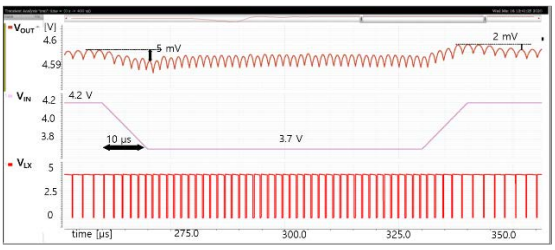
Figure 3(a) shows a variation of the inductor current I_L from V_{IN_H} (blue line) to V_{IN_L} (red line). When an RF noise does not enter, only high voltage V_{IN_H} is applied. Figure 3(b) shows the timing diagram of V_{SENSE}, the sensed voltage from the current sensor, and V_{ERROR}, the output voltage of the error amplifier. When RF noise enters, the error voltage V_{ERROR} and the sensed voltage V_{SENSE} are changed from the blue line to the red line if the converter has an RF noise-reduction circuit, they will be changed from solid lines to broken lines. Thus, var-

iation of the reset time of the clock is reduced. Figure 3(c) shows the switching voltage of the NMOS, in which variation of the pulse width is reduced with the RF noise-reduction circuit. It reduces the undershoot and overshoot of the output voltage.

Figure 4 shows simulation results under a load current condition of 100 mA, showing the operation of the boost converter to which the ICVVRC is applied. RF noise represents the output voltage of the boost converter when the input voltage is reduced from 4.2 V to 3.7 V with a slope of 10 µs and increased to 4.2 V with a slope of 10 µs, assuming transmission from a mobile device. When there is no IVVRC, the undershoot and overshoot of the output voltage are 10 mV. When there is an IVVRC, the undershoot is reduced to 5 mV and the overshoot is reduced to 2 mV, and it is confirmed that the voltage stably outputs using the IVVRC.



(a)



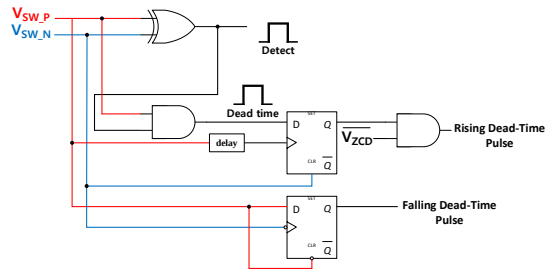
(b)

Figure 4. RF noise simulation: (a) output voltage V_{OUT} without IVVRC; (b) output voltage V_{OUT} with IVVRC @ I_{LOAD} = 100 mA.

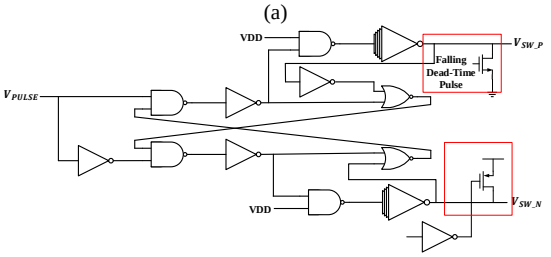
B. DEAD-TIME CONTROLLER USING DEAD-TIME DETECTOR

Dead time in a CMOS circuit is defined as the time interval between the off-time of the PMOS transistor and the off-time of the NMOS transistor. Although the dead time is needed to prevent shoot-through current, if the dead time is too long, body-diode conduction loss occurs, resulting in power efficiency reduction. It is important to have the optimal dead time to increase the power efficiency of the DC-DC converter.

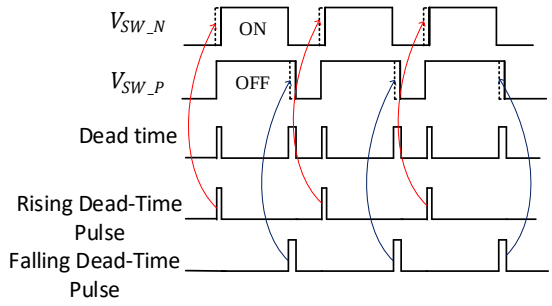
Figure 5 shows a proposed dead-time controller using a dead-time pulse generator to reduce the dead time of a P-N power transistor. Figure 5(a) shows a dead-time pulse generator, which detects the rising (falling) edge of a P (N) power transistor to generate a rising (falling) dead-time pulse. Figure 5(b) and (c) show a gate driver with the dead-time controller using the dead-time pulse generator and a timing diagram, respectively. When a rising dead-time pulse occurs, it immediately turns on the NMOS power transistor. When a falling dead-time pulse occurs, it immediately turns off the PMOS power transistor. This leads to minimum dead time.



(a)



(b)



(c)

Figure 5. Proposed dead-time controller: (a) dead-time pulse generator; (b) gate driver with dead-time controller using a dead-time pulse generator; (c) timing diagram of dead-time controller.

Figure 6 shows simulation results depending on whether the dead-time controller is applied when the load current is 20 mA. In result (a), the dead time was 5.5 ns, and the dead-time controller In result (b) when applied, the dead time was reduced to 1 ns. Figure 6 shows that the dead time is reduced under each condition as a result of the dead time simulation at FF at the same load current.

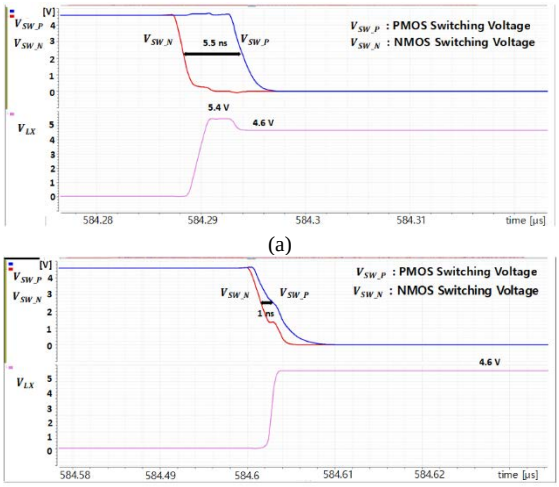


Figure 6. Switching voltage of power transistors: (a) without the dead-time controller; (b) with the dead-time controller.

C. SPWM-PWM DUAL-MODE

In this subsection, the PWM–SPWM dual-mode method is presented; it was used to reduce the switching loss under light loads [5]. Under heavy loads, PWM–SPWM dual-mode operates in PWM mode; this controls the duty at a fixed switching frequency. Under light loads, the dual mode operates in SPWM mode to reduce switching loss, which controls the frequency of the set signal for switching power transistors in proportion to output current using a voltage-controlled oscillator (VCO). Figure 7 shows the switching frequency based on the output current of the PWM–SPWM dual-mode switching method. For heavy loads greater than the mode change current I_{MC}, the method operates in PWM mode with a fixed switching frequency; however, in the case of light loads smaller than I_{MC}, it operates in SPWM mode with variable frequency. Additionally, the dual-mode method can change the frequency of the VCO output signal based on the output current; therefore, it is possible to change the I_{MC} for switching between the PWM mode and SPWM mode.

Since the method operates like a PFM that changes the switching frequency in proportion to the output current under light loads, switching loss is reduced and improved power efficiency is obtained. The method only adds a VCO and a clock selection circuit to vary the frequency of the set pulse based on the PWM mode, thereby reducing the overhead of the circuit configuration in the dual mode. The PWM-based circuit has a structure in which only the set pulse is variable through the VCO; this allows it to respond without delay while changing modes. It is also fairly simple to change the SPWM operation range considering the power efficiency and the output voltage ripple, based on the resolution and size of the display panel by changing the mode conversion output current.

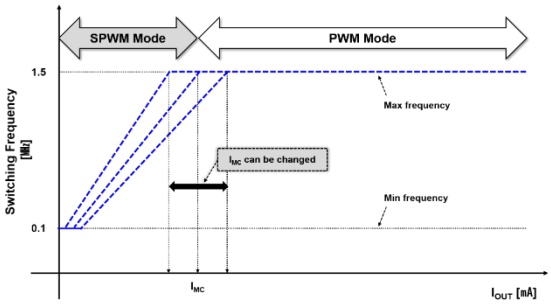


Figure 7. Switching frequency vs. output current of the SPWM–PWM dual-mode switching method.

3. EXPERIMENTAL RESULTS

Figure 8 is the layout of the proposed DC-DC converter for OLED displays with RF noise immunity. It is designed using a 0.18 μm BCDMOS process, and the total area of the circuit is 1.4 mm x 0.7 mm. The boost converter, clock generation block, and reference voltage and bias current generation block are divided and designed. The area of the proposed dead-time controller is 0.12 mm x 0.07 mm.

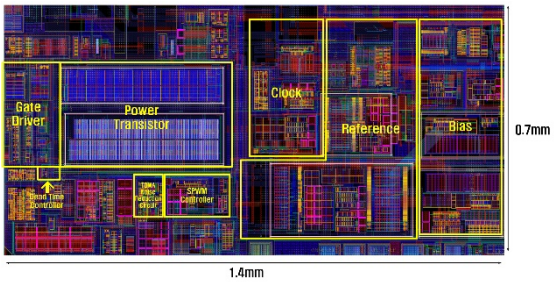


Figure 8. Layout of the proposed DC-DC converter.

Figure 9 shows the output voltage with ripple when the input voltage is 3.7 V and the load current is 20 mA. The DC-DC boost converter outputs 4.6 V with a ripple voltage of 6 mV.

Figure 10 shows the dead time according to the load current. It has a dead time of 3 ns or less when the load current is 20 mA by having the minimum dead time through the dead-time controller using the dead-time detector. This shows that the dead-time controller controls to have the minimum dead time.

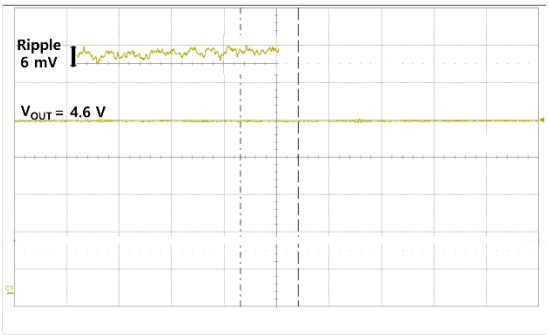


Figure 9. Figure DC output voltage with ripple @V_{IN}=3.7V and I_{LOAD}=20mA.

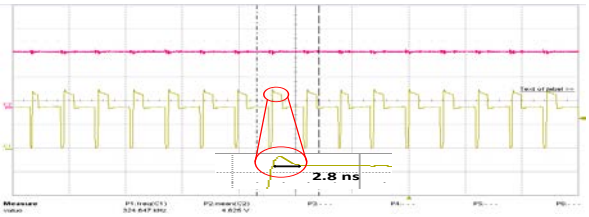


Figure 10. Dead time with ripple @V_{IN}=3.7V and I_{LOAD}=20mA.

Figure 11 is the measurement results of the RF noise characteristics of the boost converter at the maximum output current. Figure 11(a) is the measurement result of the boost converter in [10] without the IVVRC circuit. Undershoot was measured to be 20 mV and overshoot was measured to be 18 mV. Figure 11(b) shows the measurement result of the boost converter with the input voltage variation reduction circuit. Undershoot and overshoot were measured as 4 mV and 6 mV. This shows improved resistance to RF noise by outputting a more stable voltage by applying an input voltage variation reduction circuit.

Figure 12 shows the comparison of measured and simulated power efficiency according to the load current for the proposed DC-DC converter with RF noise immunity for OLED displays when the input voltage is 3.7 V and the output voltage is 4.6 V.

Figure 12 (a) shows simulation results for dual mode with dead time control method, dual mode method, and the PWM method. When the dead time control method is applied, the efficiency is improved up to 3.03%, and when the dual mode method is applied, the efficiency is improved up to 8.15%.

The measurement result (Figure 12 (b)) was 30% to 76%, The measurement results were up to 19% lower than the simulation results. It is estimated that the main cause of the difference between the simulation and the measured value is the decrease in efficiency due to the bonding wire in the COB (chip on board) process. We predicted the power loss using the bonding wire actually used. The length of the bonding wire used was about 1.1 cm, 15 um in diameter, and had a resistance of about 2 Ω for input and output, respectively. The simulation results adding conduction loss due to above values are similar to the measured values.

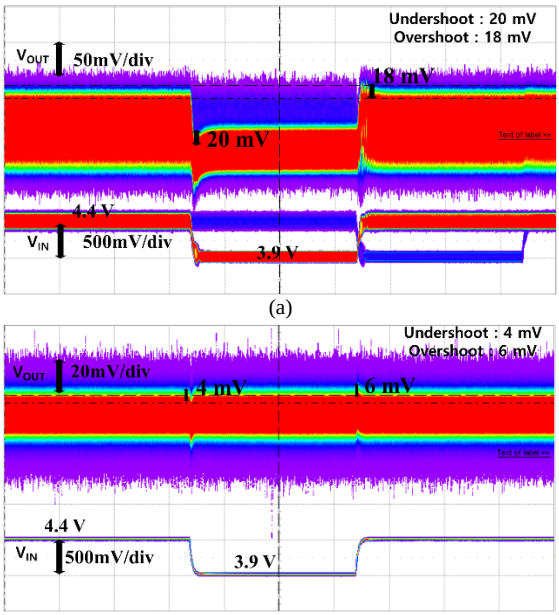


Figure 11. RF noise measurement results: (a) a boost converter of [10] without IVVRC; (b) our boost converter with an IVVRC.

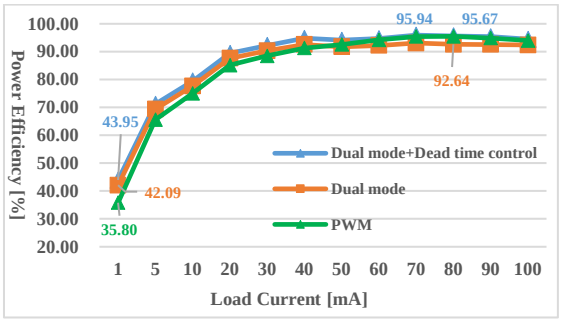


Figure 12. Power efficiency of the proposed DC-DC boost converter: (a) simulation results for methods using the dual-mode or/and the dead-time controller; (b) total power efficiency.

4. CONCLUSION

In this paper, a DC-DC converter for OELD displays with RF noise immunity is designed as a boost converter by using SPWM-PWM dual-mode with a built-in input voltage variation reduction circuit for RF signal immunity and a dead-time controller to increase efficiency. The proposed input voltage variation reduction circuit can be configured in a small area with three current mirrors.

The chip is implemented using a 0.18 μm high-voltage BCD process. As a result of measurement, when an input voltage of 2.9 V to 4.4 V was applied, the output voltage was 4.6 V, and the ripple voltage was measured to be less than 10 mV for the boost converter. As a result of RF noise immunity measurement, the undershoot and overshoot were measured to be 20 mV and 18 mV for the boost converter without the input voltage variation reduction circuit, and decreased to 6 mV to have a more stable voltage. As a result of simulation, the power efficiency of the boost converter was 39% ~ 94%, which is up to 8% higher than that of PWM single mode using SPWM-PWM dual-mode and the dead-time controller. The chip measurements were 30% to 76% for the boost converter.

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