



Volatile Memristor-Based Artificial Spiking Neurons for Bioinspired Computing

Soon Joo Yoon and Yoon Kyeong Lee 

Division of Advanced Materials Engineering, Jeonbuk National University, Jeonju 54896, Korea

(Received May 10, 2022; Revised May 26, 2022; Accepted June 2, 2022)

Abstract: The report reviews recent research efforts in demonstrating a computing system whose operation principle mimics the dynamics of biological neurons. The temporal variation of the membrane potential of neurons is one of the key features that contribute to the information processing in the brain. We first summarize the neuron models that explain the experimentally observed change in the membrane potential. The function of ion channels is briefly introduced to understand such change from the molecular viewpoint. Dedicated circuits that can simulate the neuronal dynamics have been developed to reproduce the charging and discharging dynamics of neurons depending on the input ionic current from presynaptic neurons. Key elements include volatile memristors that can undergo volatile resistance switching depending on the voltage bias. This behavior called the threshold switching has been utilized to reproduce the spikes observed in the biological neurons. Various types of threshold switch have been applied in a different configuration in the hardware demonstration of neurons. Recent studies revealed that the memristor-based circuits could provide energy and space efficient options for the demonstration of neurons using the innate physical properties of materials compared to the options demonstrated with the conventional complementary metal-oxide-semiconductors (CMOS).

Keywords: Memristors, Threshold switch, Artificial neuron, Neuromorphic computing

1. INTRODUCTION

As the amount of data subject to processing has increased rapidly due to ubiquitous electronic devices and sensors for Internet of Things (IOT) and cloud services, the modern computers face the limitations of their computing performance in dealing with such vast amounts of data [1]. The conventional digital computers based on von Neumann architecture have been developed to be specialized in increasing the accuracy and speed of logic operations. The advances in complementary metal oxide semiconductor (CMOS) technology successfully

supported such direction of the development in the past. However, as the speed of data communication between the processing and memory units of the von Neumann architecture becomes the bottleneck in rapidly increasing data-intensive tasks, questions about the efficiency of the computing architecture and the supporting device units have been raised.

The human brain adopts fundamentally different global architecture and composing computing units, and show superior performances to conventional computers in certain areas that require parallel information process or probabilistic or atypical problem solving with low driving energy. The competence of the brain originates from the unique structure of the neural networks in the brain that connect neurons in a large scale through synapses. The structure allows simultaneous storage and processing of the data while minimizing power consumption required for data communication. Another

✉ Yoon Kyeong Lee; yoonklee@jbnu.ac.kr

Copyright ©2022 KIEEME. All rights reserved.
This is an Open-Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (<http://creativecommons.org/licenses/by-nc/3.0>) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

distinct feature of the brain compared to the modern computer is the communication mechanism between neurons, the computing units in the biological neural networks. Neurons receive and send current spikes based on local and temporal inputs from surrounding neighbor neurons. Data processing occurs during the transmission of the spike-coded temporal information whose results depend on the strength of the connectivity, also called synaptic weight.

The continuous effort to build an artificial intelligence established the basis for the novel algorithms that mimic the processing of the biological neural networks. The algorithms represented by artificial neural network (ANN) model the biological neural network by linking the layered nonlinear functional units through trained strength of the connectivity, called synaptic weight. Implementing such algorithm in the conventional computers that adopt fundamentally different architecture than the model structure of the algorithm causes the inefficiency in time and energy consumption. Separate physical device location for storing the large amount of synaptic weights and for processing of such data requires excessive time and power for data transmission through limited communication bandwidth. Crossbar arrays of resistive memory have been utilized to perform the vector-matrix multiplication during the training and inference steps efficiently for the last decade [2-5].

Spiking neural network (SNN) is considered more advanced bioinspired algorithms in that the model encompass the feature of the biological neural network that communicate through temporal spikes. The simulation of SNN in the modern computer is even more challenging due to the complex dynamics and the large population of neurons that cannot be simulated through a simple combination of CMOS devices. Recent announcement of CMOS-based SNN hardware has suggested the energy and time efficiency of SNN in solving certain types of recognition problems, but the development of hardware systems using emerging memory and logic devices remained less explored [6].

Recent advances in various nanoscale electronic devices offer potentially powerful options for hardware implementation of the biological neural network with their inherent complex dynamics that resembles certain characteristics of neurons and synapses [5,7-11]. Memristors, short for memory resistors, are characterized by hysteretic current-voltage behavior whose voltage-induced resistance change can be either volatile or non-volatile. The volatile change from high resistance to low

resistance states can demonstrate the threshold switching of the neurons while the nonvolatile change can be utilized to store different levels of synaptic weights. Compared to the neuron devices based on volatile memristors, synaptic devices based on nonvolatile memristors have been more extensively studied due to their wide application ranges including the implementation of both ANN and SNN. The hardware demonstration of artificial spiking neurons has been less actively pursued partially due to the limited success of SNN compared to ANN. However, the potential of SNN in terms of time and power efficiency, and the continuing effort to develop better algorithms demand corresponding research effort in developing proper electronic devices for artificial spiking neurons that can efficiently simulate SNN.

This paper provides a review of recent research on the hardware implementation of spiking neurons using volatile memristors. The review first introduces the neuron models that have been developed to be consistent with the experimental observations on biological neurons. Next, the principles of different types of volatile memristors are summarized. Various switching mechanisms, materials and current-voltage characteristics provide a wide range of options for the implementation of artificial spiking neurons with different levels of complexity. Other electronic components and their combinations for circuit-level demonstration of spiking neurons will be presented with their output characteristics.

2. NEURON MODELS

2.1 Biological neurons

2.1.1 Spike generation of neurons

The structure of a biological neuron that is actively involved in the information processing consist of three functional parts: dendrite, soma and axon [Fig. 1(a)] [12,13]. The dendrite receives input signals from other neurons and transmits them to the soma. The soma adds the input signals and performs a non-linear processing step. If the total input exceeds a threshold, an output is generated as a form of a voltage spike. The output signal propagates to the axon, which delivers the signal to other neurons.

The neurons communicate through electrical pulses called action potentials or spikes with an amplitude of about 110 mV

with a typical duration of 1~10 ms [Fig. 1(a)]. The post-synaptic membrane potential initially increases linearly to the input spikes. The increase decays without an input, but can reach a critical value called a threshold voltage when consecutive inputs arrive. The threshold is about -55 mV [25 mV above the rest potential (-70 mV)]. In the latter case, the membrane potential exhibits an abrupt rise to about 110 mV, similar to the signal they received from the pre-synaptic neurons.

The spike-generation process is induced by the opening of Na⁺ channels in the cell membrane. The gradual increase occurs in the membrane potential during the time period t_1 in Fig. 1(a) and (b) [13]. Once the membrane potential exceeds the threshold at time t_2 , the fast inward-flow of Na⁺ results in a significant further rise of the membrane potential. This positive feedback raises the potential rapidly until most of the available Na⁺ channels are open. This leads to the observed large upswing of the membrane potential. Once reaching the maximum, the membrane experiences repolarization as described in time period t_3 in Fig. 1(a) due to the inactivation of the Na⁺ channels and the opening of the K⁺ ion channels.

The refractory period where the membrane potential becomes more negative than rest potential (hyperpolarization) after the spike prevents the generation of a second spike immediately after the first one. The overall shape of action potential is described in Fig. 1(c). This short voltage pulse will propagate along the axon of neuron to the synapses with other neurons.

Spike train refers to a chain of action potentials produced by a single neuron in a short time interval. It is believed that the number and the timing of spikes carry the information, not the exact shape of the action potential [13]. This assumption simplifies the physical demonstration of neuron models that simulate the signal transmission function of neurons. In summary, the neurons gather the temporal local information, and produce spike trains at proper times.

2.1.2 Synapses

In biological neural networks where neurons communicate through the spikes, the junction parts between two neurons are called synapses. Specifically, the site where the axon of a pre-synaptic neuron is in contact with the dendrite of a post-synaptic neuron is in contact with the dendrite of a post-

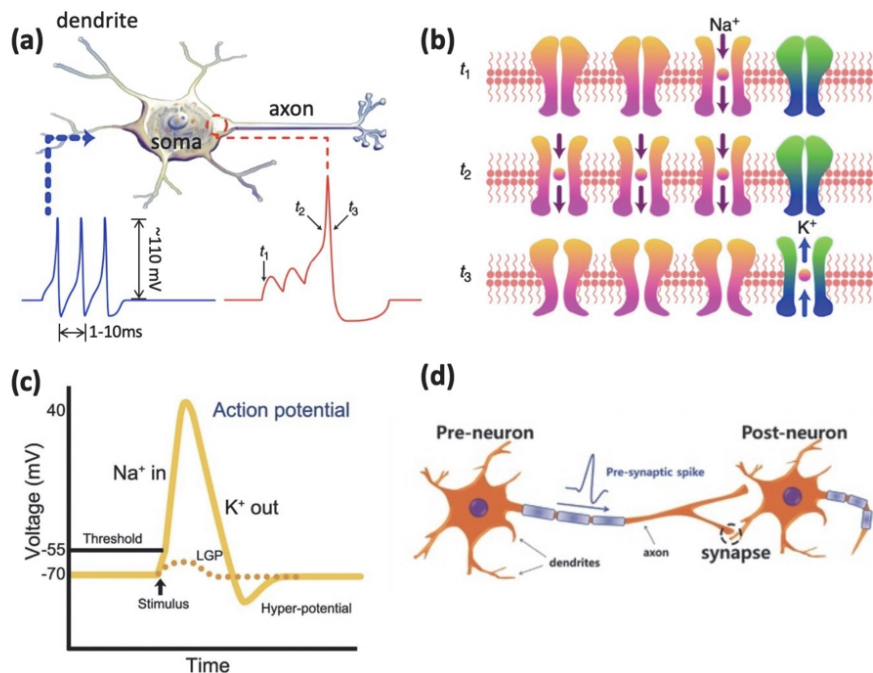


Fig. 1. (a) The structure biological neuron. The neuron generates an action potential after receiving multiple spike inputs from the dendrite (Copyright 2018 Springer Nature [13]). (b) At time t_1 , a small number of Na⁺ channels are open before reaching the threshold. At time t_2 when the threshold voltage reached, most Na⁺ channels are open due to voltage-mediated activation mechanism. After the potential reached its maximum value at t_3 , the opening of K⁺ channels causes the decrease of the potential (Copyright 2018 Springer Nature [13]). (c) The change of membrane potential and the generation of action potential in a biological neuron (Copyright 2019 Wiley-VCH [16]). (d) The magnified view of synapse, presynaptic and postsynaptic neurons (Copyright 2016 Wiley-VCH [38]).

synaptic cell is the synapse [Fig. 1(d)]. Here, the signal sending neuron is called the presynaptic cell and the signal receiving neuron is called the postsynaptic cell. Postsynaptic potential refers to the voltage response of the postsynaptic neuron to a presynaptic spike.

Membrane potential is the potential difference between the interior of the cell and its surroundings. Excitatory synapse refers to the synapse where the change of post-synaptic potential is positive after the arrival of a spike. If the change is negative, the synapse is called inhibitory. The importance of the inhibitory neurons is suggested in many models in neuroscience, but the hardware demonstrations of neurons in electronic devices have more focused on the excitatory neurons yet.

2.2 Integrate-and-fire models

Modeling the dynamics of neural networks unavoidably involves the extraction of key features of neurons that are believed to contribute to the global function of the brain such as perception or decision making. Spike generation mechanism is a particular interest in the modeling while the details in molecular levels are often ignored. Integrate-and-fire models describe action potentials as events based on the experimental observation that neuronal action potentials of a given neuron always have roughly the same form. The observation indicates that the spike shape is not used to transmit information. The precise moment in time of the events does. Two components are necessary to describe the integrate-and-fire models: the variation of the membrane potential and a mechanism to generate spikes. This review focuses on qualitative description of the neuron models to introduce the devices and circuits for their hardware implementation later, but the readers who are interested in the mathematical details of the model should refer to the relevant references [12]. In integrate-and-fire models, the timing of spike generation determine the moment of the events.

Figure 2(a) shows a basic electrical circuit that can demonstrate integrate-and-fire models [14]. The circuit consists of a capacitor and a switch in parallel. Integration occurs as the charge accumulates across the capacitor as a result of the input current [Process (1) in Fig. 2(a)]. Without a leaky electrical path, no relaxation is explicitly considered. When the voltage across the capacitor exceeds a certain threshold,

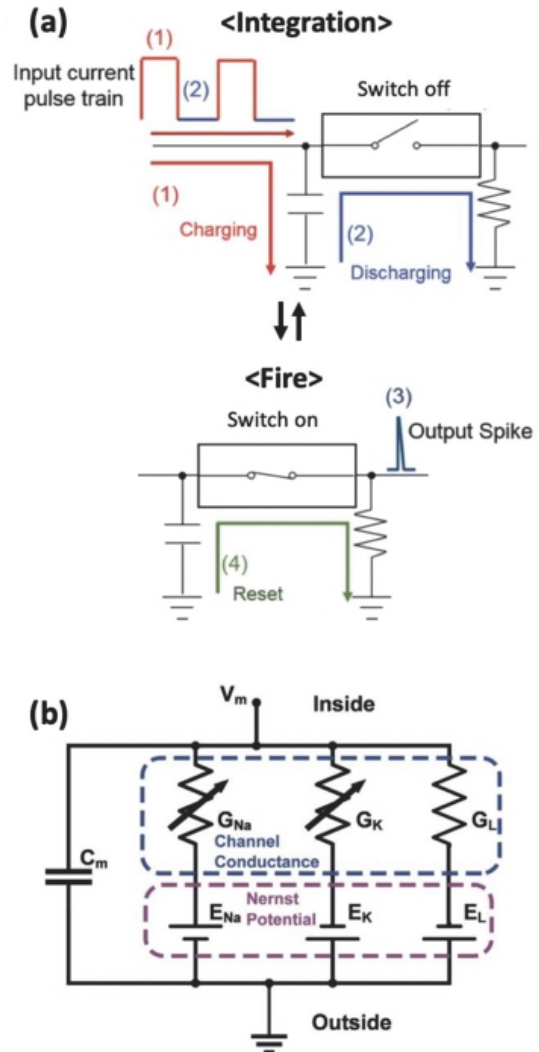


Fig. 2. (a) The basic circuit consisting of one capacitor and one variable resistor for the demonstration of leaky integrate-and-fire neuron (Copyright 2019 Wiley-VCH [14]) and (b) Hodgkin-Huxley model (Copyright 2019 Wiley-VCH [16]).

the switch in the circuit discharges the accumulated charges [Process (2) in Fig. 2(a)], which simulate the firing event [Process (3) and (4) in Fig. 2(a)]. In other types of demonstration, a nonvolatile phase change memory with multilevel analogue resistance states can store the information of the membrane potential instead of the charge storing capacitor [15].

2.3 Leaky-integrate-and-fire model

In biological neurons, the membrane potential returns to the

rest potential in the absence of an input from the pre-synaptic neurons. This relaxation property is considered in a leaky-integrate-and-fire model. The basic electrical circuit representing a leaky integrate-and-fire model is similar to the one for integrate-and-fire model, but with a leaky component that can be innate either in the capacitor or switch in its off-state or an additional resistor in parallel with the capacitor. In the absence of input, the voltage across the capacitor that describes the membrane potential of a neuron decays exponentially to the rest potential. For a typical neuron, the decay time is in the range of 10ms, which is about ten times longer compared to the duration of a spike.

The leaky-integrate-and-fire model is one of the popular models in the hardware demonstration of neurons due to the small number of elements in the circuit and the possibility of parameter tuning using diverse physical properties of emerging switch devices. The limitation of the model includes the absence of components that can simulate the memory effects of neurons observed in experiments such as adaptation and bursting.

2.4 Hodgkin-Huxley model

The Hodgkin-Huxley model is one of the more detailed biophysical neuron models that describe the generation of action potentials based on the level of ion channels and ion current flow [12]. The Hodgkin-Huxley model includes three types of currents that can change the membrane potential: the current through Na^+ and K^+ channels, and a passive leaky channel for the relaxation. The three types of current paths are still a simplified model considering the richness of different ion channels observed experimentally, but successfully describe the change of the membrane potential based on the physical model of variable conductivity of a specific type of ion channels. When Na^+ channels are open, the selective passage of Na^+ through the channels causes a rest or Nernst potential (E_{Na}) of about +67 mV. This means that, at equilibrium with open Na^+ channels, the interior of the cell has a positive potential with respect to the surround because of the selective influx of Na^+ from the external (with high concentration of Na^+) to the internal part (with low concentration of Na^+) of neurons. When K^+ channels are considered, instead, the equilibrium potential E_{K} should become -83 mV. The negative sign is caused by the higher

concentration of K^+ in the interior of the neuron and the resulting outflux of K^+ as previously described in Fig. 1(b). It is found experimentally that the resting potential of the membrane is about -70 mV due to the contributions from both channels, but with stronger effect of K^+ ion channels.

Figure 2(b) describes a model circuit that can be used to analyze the behavior of the Hodgkin-Huxley model [16]. The node voltage assigned as V_m describes the membrane potential which changes with the conductance variations of G_{Na} and G_{K} . The reversed orientation of the two batteries connected to G_{Na} and G_{K} reflect the opposite signs of the Nernst potentials of Na^+ and K^+ ion channels. The variable resistors can be considered as lumped models of a finite number of ion channels. The variations in the conductivity of the resistors are described with several parameters that reflect the activation and relaxation of the channels as a function of the membrane potential, and enable the model to generate action potentials.

The leaky integrate-and-fire model described here has a rather limited scope in describing the complex neuronal dynamics including the memory effect partly due to the fixed value of voltage threshold determined by the model parameters [12]. More generalized models incorporate adaptation variables and stochasticity. The addition can reproduce the adaptive threshold voltage and memory effects often observed in characteristic firing patterns of real biological neurons.

3. MEMRISTOR-BASED THRESHOLD SWITCH

We reviewed representative neuron models in Part 2 and two basic electrical circuits that can simulate the membrane potential of neurons. The electrical elements in the circuits for the simulation of artificial neurons can be built with various types of electronic devices with different physical properties. Artificial neurons built with conventional CMOS have limitations in emulating the rich dynamics of biological counterparts in large scale without sacrificing the power consumption and circuit dimensions. Emerging electronic devices based on memristors, instead, can be used to construct an electronic equivalent of biological neurons in a more energy and space efficient way owing to their innate physical properties and rich dynamics that resemble biological neurons. Memristors can show both volatile and nonvolatile resistive switching depending on the retention time of their low

resistance state. The volatile memristors which becomes locally active within a hysteretic negative differential resistance regime in current-voltage characteristics are of particular interest in the current review since their volatile switching to low resistance state can simulate the spike generation of neurons in various ways. Before introducing the recent progress in hardware demonstration of neurons using volatile memristors, Part 3 summarizes the electrical features of the volatile memristors and their plausible threshold switching mechanism.

3.1 Device structure and characteristics

The basic memristor cell adopts a two-terminal device structure as depicted in Fig. 3(a) [17]. The resistance switching layer is sandwiched between two metal layers whose potential difference determine the resistance state of the active layer. The two-terminal structure allows $4F^2$ (F : minimum feature size) device dimension and three-dimensional vertical stack, which is beneficial for large integration density of neurons. Recent studies also developed three or four-terminal structure of the volatile memristors to separate the terminals for resistance control and for read operation or to better control the resistance states in a gradual manner [18-20].

Various materials can show threshold switching behavior, and be categorized based on their compositions. Oxides and chalcogenides such as SiO_2 , HfO_2 (oxides) and GeTe or GeSe (chalcogenides) are one of the biggest categories [21-25]. Two-dimensional materials such as h-BN , MoS_2 and perovskites have also been actively researched for their threshold switching properties [26-28]. Besides the active layer, electrodes also serve a critical role in threshold switching as they can provide metal ions that can form a conductive filament in the active area or control the composition of the active layer through chemical reactions.

Figure 3(b) shows the unipolar switching behavior of volatile memristors [16]. The sign of voltage polarity does not influence the switching behavior when the state is restored to the initial state after the switching due to the symmetric structure of the two-terminal device. The initial high-resistance state (HRS) is switched to low-resistance state (LRS) when the bias reaches the threshold level (V_{th}). The low-resistance state is maintained even with a reduced bias during the reversed voltage swing until the voltage reaches the minimum that can

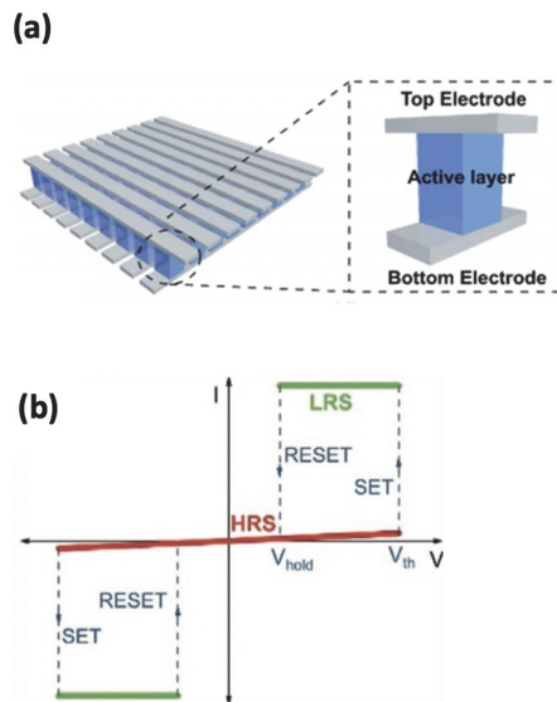


Fig. 3. (a) The two-terminal structure of a unit-cell of typical memristors (Copyright 2020 Wiley-VCH [17]) and (b) I-V characteristics of unipolar threshold switching (Copyright 2019 Wiley-VCH [16]).

maintain the low-resistance state. This voltage is called a hold voltage (V_{hold}). The threshold swing can also be induced by a voltage pulse in which switching and relaxation speed can be measured.

3.2 Threshold switching mechanism

The threshold switching mechanism depends on the material choice for the device. The exact mechanism is still a subject of active debate for certain types of the devices due to the limitations of each model. For the active layers which possess mobile ions under voltage bias, the volatile switching often occurs due to the formation and rupture of local conductive filament. The ions can be provided by electrodes such as Ag and Cu that can be electrochemically oxidized or reduced. Thermal models assume the existence of a positive feedback loop for thermal activation of carriers by Joule heating above V_{th} . Modifications are necessary for amorphous chalcogenides where electronic contribution cannot be neglected.

Threshold switching of Mott memristors such as the ones

based on NbO_2 or VO_2 is a representative example that undergoes temperature-induced volatile resistance change [29,30]. The mechanism partially explains the threshold switching of chalcogenide materials, but the modification that considers the electronic contribution becomes more reasonable to explain the experimental data. The double-injection model first suggested by Mott and Henisch assumes electrons and holes injected from the electrode and the resulting space-charge region at the cathode and anode [31-33]. The two space-charge regions grow under increased bias and eventually overlap when abrupt conductivity changes occur. More advanced model based on the valence-alternation defect pair was suggested by Adler [34]. The generation and recombination of carriers occur in the presence of such defects whose number increases with electric field. Ielmini later proposed the electron current caused by the tunneling between trap sites and continued to modify the original proposal by incorporating a nonequilibrium quasi-Fermi level and carrier temperature [35,36].

4. MEMRISTIVE NEURON

The demonstration of artificial neurons using threshold switch represents a simple and faithful option in terms of the number of devices and energy consumption in contrast to

traditional approaches based on CMOS devices. This section introduces a few selective examples that implement the spiking properties of biological neurons using volatile memristors.

4.1 Artificial neuron based on Mott memristors

One of the first demonstration of spiking neurons was introduced using Mott memristors based on NbO_2 formed from Nb_2O_5 [30]. The proposed neuristor realized the essential features for spike-based computing such as threshold-driven spiking with a refractory period. The threshold switch showed rapid operation speed ($<1\text{ns}$) with low transition energy ($<\sim 100\text{ fJ}$), scalability at least to tens of nanometers with compatibility with conventional CMOS processes. The neuristor circuit contains two Mott memristors. The memristors have a parallel capacitor connected to the DC power source with opposite polarity, similar to the Nernst potentials of Na^+ and K^+ channels in biological neurons. The output voltage is measured across the resistor R_{out} in the neuristor circuit when stimulated by both super-threshold (0.3 V) and sub-threshold (0.2 V) voltage inputs. The pulse with an amplitude over the device threshold produced an action potential with an amplitude of 0.33 V whereas the pulse below its threshold induced a small output voltage change of 0.028 V.

Later, VO_2 -based active memristor neuron was constructed with a similar circuit configuration [29]. Compared to the

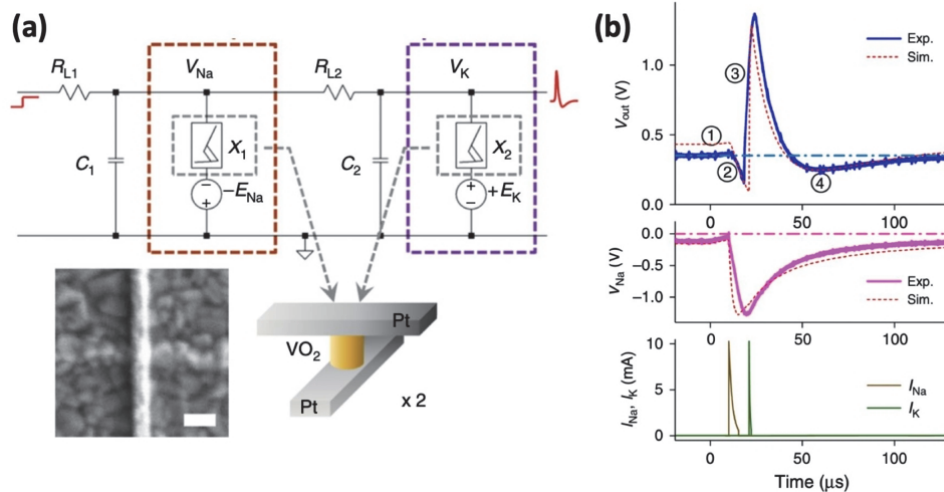


Fig. 4. (a) Basic circuit of a VO_2 -based artificial neuron (Na^+ and K^+ channels are emulated by oppositely DC biased active memristor devices. Scale bar: 100 nm) and (b) basic steps to generate a action spike using a VO_2 neuron [(1) Resting state with closed Na^+ and K^+ channels, (2) hyperpolarization induced by the activation of the Na^+ channel, (3) depolarization caused by the activation of the K^+ channel, and (4) refractory period] (Copyright 2018 Springer Nature [29]).

conventional approach to form VO₂ from amorphous V₂O₅, electroforming-free VO₂ memristors avoided the production of void in the oxide and electrode damage. The prototype circuit described in Fig. 4(a) consists of two DC-biased active memristors (X₁ and X₂) and two parallelly connected capacitors (C₁ and C₂), and load resistors (R_{L1} or R_{L2}). The oppositely-biased memristors X₁ and X₂ emulate the Na⁺ and K⁺ ion channels, respectively, through their variable conductivity depending on the voltage across them. Detailed dynamics to generate a spike can be divided into four steps as described in Fig. 4(b). Step 2 and 3 correspond to the switching to the low resistance state of X₁ and X₂, respectively.

4.2 Artificial neuron based on ion-mediated memristors

Neuro-transistor introduced in 2018 utilized a dynamic pseudo-memcapacitor (DPM) that consists of one memristor and capacitor to demonstrate the integrate-and-fire function of

soma [13]. The upper layer composed of Pt/Ag/SiO_x:Ag/Ag/Pt diffusive memristor was serially connected with a Pt/Ta₂O₅/TaO_x/Pt capacitor [Fig. 5(a)]. The overall capacitance was initially determined by the diffusive memristor (C_p) due to the large dielectric constant of Ta₂O₅, but switched to the series capacitance (C_s) after the diffusive memristor became a low resistance state. Figure 5(b) describes the membrane potential demonstrated as the voltage across C_s in response to the input of voltage pulses. The diffusive memristor of the DPM plays the role of Na⁺ channels in the phase of charge accumulation and the role of K⁺ channels in the phase of discharging. An active neuron can be constructed by applying the DPM as the gate insulator of a transistor that can convert the voltage spike to the current flow [Fig. 5(c)].

Quasi-Hodgkin-Huxley neurons that produce a spike more similar to the biological one was demonstrated using two memristive devices of W/WO₃/PEDOT:PSS/Pt assigned as M₁ and M₂ in Fig. 6(a) [37]. The innate battery effect in conventional oxide-based memristors is originated from the

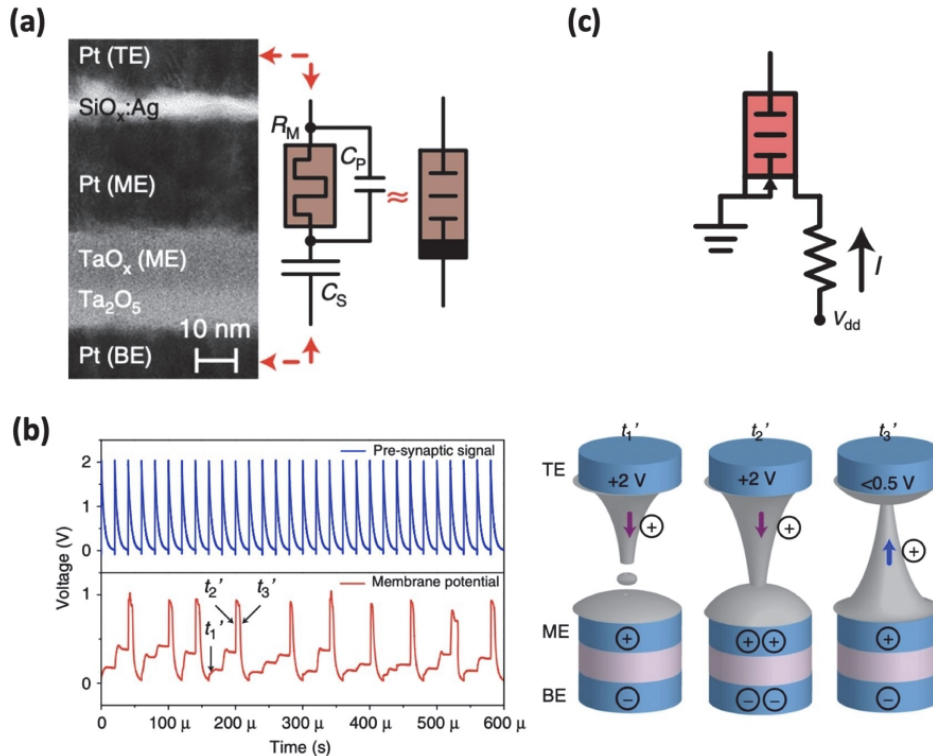


Fig. 5. (a) Cross-sectional transmission electron micrograph (TEM) image of DPM, (b) the integrate-and-fire of a DPM (at time t₁' the potential across the capacitor rose linearly upon the input pulse due to the high resistance of the diffusive memristor and at time t₂' the switching of the diffusive memristor to a low resistance state caused full charge of the capacitor), and (c) the structure of neuro-transistor where a DPM consists of the gate of a MOSFET (Copyright 2018 Springer Nature [13]).

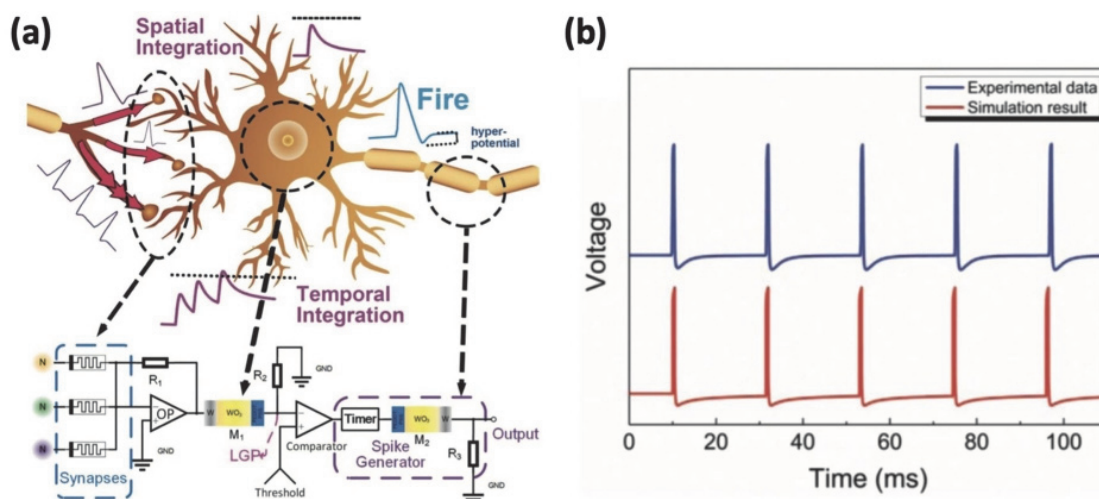


Fig. 6. (a) An artificial neuron constructed by second-order memristors [the voltage over resistor R_2 represents the membrane potential before it reaches the threshold. M_2 contributes the generation of the spikes (purple rectangle)] and (b) the shape of the generated spikes induced by consecutive input pulses (Copyright 2019 Wiley-VCH [37]).

migration of oxygen ions, but the WO_3 /PEDOT:PSS-based memristors rely on the migration of protons supplied by PEDOT:PSS. The complete circuit for the demonstration of Quasi-Hodgkin-Huxley neurons is described in Fig. 6(a). The input signals applied on the memristive device M_1 modulate the membrane potential simulated as the voltage across R_2 . When the membrane potential is below the threshold value, the accumulated current leaks out, which restores the high resistance of M_1 . The output signal, voltage over the resistor R_3 , represents a spike whose shape follows the biological spike as shown in Fig. 6(b).

5. SUMMARY AND OUTLOOK

The report reviewed the hardware demonstration of biological neurons using dedicated circuits containing volatile memristors. Key features of neuronal dynamics are the change of membrane potential according to the input ionic current from presynaptic neurons. The leaky integrate-and-fire models describe the charge accumulation, spike generation, and relaxation processes that occur during the information process in the brain. More detailed molecular picture of the neurons can be included reflecting the variable ion conductance of ion channels with their own Nernst potential depending on the membrane potential. Simplified circuits can be utilized to analyze the behavior of the model using proper elements

including capacitors and resistors. The report reviewed examples of research that applied threshold switch for the capacitors and resistors components to reproduce the spiking generation properties of the neurons. The memristor-based implementation represents the simplest, yet reliable options for the demonstration of such circuits by using the innate physical properties of the device, which reduces the number of the component devices and energy consumption compared to the circuits demonstrated with CMOS.

ORCID

Yoon Kyeong Lee

<https://orcid.org/0000-0001-5160-1015>

ACKNOWLEDGEMENT

This work has supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIT) (No. NRF-2022R1C1C1010071).

REFERENCES

- [1] D. S. Jeong, K. M. Kim, S. Kim, B. J. Choi, and C. S. Hwang, *Adv. Electron. Mater.*, **2**, 1600090 (2016). [DOI: <https://doi.org/10.1002/AELM.201600090>]
- [2] S. Ambrogio, P. Narayanan, H. Tsai, R. M. Shelby, I. Boybat, C. di Nolfo, S. Sidler, M. Giordano, M. Bordini, N.C.P. Farinha,

- B. Killeen, C. Cheng, Y. Jaoudi, and G. W. Burr, *Nature*, **558**, 60 (2018). [DOI: <https://doi.org/10.1038/s41586-018-0180-5>]
- [3] S. Oh, Y. Shi, J. Valle, P. Salev, Y. Lu, Z. Huang, Y. Kalcheim, I. Schuller, D. Kuzum, *Nature Nanotechnology*, **16**, 680 (2021) [DOI: <http://doi.org/10.1038/s41565-021-00874-8>]
- [4] Z. Wang, S. Joshi, S. Savel'ev, W. Song, R. Midya, Y. Li, M. Rao, P. Yan, S. Asapu, Y. Zhuo, H. Jiang, P. Lin, C. Li, J. H. Yoon, N. K. Upadhyay, J. Zhang, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, R. S. Williams, Q. Xia, and J. J. Yang, *Nat. Electron.*, **1**, 137 (2018). [DOI: <https://doi.org/10.1038/s41928-018-0023-2>]
- [5] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H.S.P. Wong, and H. Qian, *Nat. Commun.*, **8**, 15199 (2017). [DOI: <https://doi.org/10.1038/ncomms15199>]
- [6] M. Davies, N. Srinivasa, T. H. Lin, G. Chinya, Y. Cao, S. H. Choday, G. Dimou, P. Joshi, N. Imam, S. Jain, Y. Liao, C. K. Lin, A. Lines, R. Liu, D. Mathaikutty, S. McCoy, A. Paul, J. Tse, G. Venkataramanan, Y. H. Weng, A. Wild, Y. Yang, and H. Wang, *IEEE Micro*, **38**, 82 (2018). [DOI: <https://doi.org/10.1109/MM.2018.112130359>]
- [7] G. Pedretti, V. Milo, S. Ambrogio, R. Carboni, S. Bianchi, A. Calderoni, N. Ramaswamy, A. S. Spinelli, and D. Ielmini, *Sci. Rep.*, **7**, 5288 (2017). [DOI: <https://doi.org/10.1038/s41598-017-05480-0>]
- [8] J. Woo, T. V. Nguyen, J. H. Kim, J. P. Im, S. Im, Y. Kim, K. S. Min, and S. E. Moon, *Sci. Rep.*, **10**, 11703 (2020). [DOI: <https://doi.org/10.1038/s41598-020-68547-5>]
- [9] D. H. Lim, S. Wu, R. Zhao, J. H. Lee, H. Jeong, and L. Shi, *Nat. Commun.*, **12**, 319 (2021). [DOI: <https://doi.org/10.1038/s41467-020-20519-z>]
- [10] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, *Nano Lett.*, **10**, 1297 (2010). [DOI: <https://doi.org/10.1021/nl904092h>]
- [11] D. Mehta, M. Rahman, K. Aono, and S. Chakrabartty, *Nat. Commun.*, **13**, 1670 (2022). [DOI: <https://doi.org/10.1038/s41467-022-29320-6>]
- [12] W. Gerstner, W. M. Kistler, R. Naud, and L. Paninski, *Neuronal Dynamics: From Single Neurons to Networks and Models of Cognition. 1st ed. Chapter 2* (Cambridge University Press, UK, 2014).
- [13] Z. Wang, M. Rao, J. W. Han, J. Zhang, P. Lin, Y. Li, C. Li, W. Song, S. Asapu, R. Midya, Y. Zhuo, H. Jiang, J. H. Yoon, N. K. Upadhyay, S. Joshi, M. Hu, J. P. Strachan, M. Barnell, Q. Wu, H. Wu, Q. Qiu, R. S. Williams, Q. Xia, and J. J. Yang, *Nat. Commun.*, **9**, 3208 (2018). [DOI: <https://doi.org/10.1038/s41467-018-05677-5>]
- [14] D. Lee, M. Kwak, K. Moon, W. Choi, J. Park, J. Yoo, J. Song, S. Lim, C. Sung, W. Banerjee, and H. Hwang, *Adv. Electron. Mater.*, **5**, 1800866 (2019). [DOI: <https://doi.org/10.1002/aelm.201800866>]
- [15] T. Tuma, A. Pantazi, M. L. Gallo, A. Sebastian, and E. Eleftheriou, *Nat. Nanotechnol.*, **11**, 693 (2016). [DOI: <https://doi.org/10.1038/nnano.2016.70>]
- [16] R. Yang, H. M. Huang, and X. Guo, *Adv. Electron. Mater.*, **5**, 1900287 (2019). [DOI: <https://doi.org/10.1002/aelm.201900287>]
- [17] R. Wang, J. Q. Yang, J. Y. Mao, Z. P. Wang, S. Wu, M. Zhou, T. Chen, Y. Zhou, and S. T. Han, *Adv. Intell. Syst.*, **2**, 2000055 (2020). [DOI: <https://doi.org/10.1002/aisy.202000055>]
- [18] H. Lee, S. W. Cho, S. J. Kim, J. Lee, K. S. Kim, I. Kim, J. K. Park, J. Y. Kwak, J. Kim, J. Park, Y. J. Jeong, G. W. Hwang, K. S. Lee, D. Ielmini, and S. Lee, *Nano Lett.*, **22**, 733 (2022). [DOI: <https://doi.org/10.1021/acs.nanolett.1c04125>]
- [19] E. Herrmann, A. Rush, T. Bailey, and R. Jha, *IEEE Electron Device Lett.*, **39**, 500 (2018). [DOI: <https://doi.org/10.1109/LED.2018.2806188>]
- [20] S. Choi, J. W. Choi, J. C. Kim, H. Y. Jeong, J. Shin, S. Jang, S. Ham, N. D. Kim, and G. Wang, *Nano Energy*, **84**, 105947 (2021). [DOI: <https://doi.org/10.1016/J.NANOEN.2021.105947>]
- [21] J. Yoo, J. Park, J. Song, S. Lim, and H. Hwang, *Appl. Phys. Lett.*, **111**, 063109 (2017). [DOI: <https://doi.org/10.1063/1.4985165>]
- [22] Q. Hua, H. Wu, B. Gao, M. Zhao, Y. Li, X. Li, X. Hou, M.F.M. Chang, P. Zhou, H. Qian, *Adv. Sci.*, **6**, 1900024 (2019). [DOI: <https://doi.org/10.1002/ADVS.201900024>]
- [23] H. Jiang, D. Belkin, S. E. Savel'ev, S. Lin, Z. Wang, Y. Li, S. Joshi, R. Midya, C. Li, M. Rao, M. Barnell, Q. Wu, J. J. Yang, and Q. Xia, *Nat. Commun.*, **8**, 882 (2017). [DOI: <https://doi.org/10.1038/s41467-017-00869-x>]
- [24] C. Yoo, W. Kim, J. W. Jeon, E. S. Park, M. Ha, Y. K. Lee, and C. S. Hwang, *ACS Appl. Mater. Interfaces*, **12**, 23110 (2020). [DOI: <https://doi.org/10.1021/acsami.0c03747>]
- [25] W. Kim, S. Yoo, C. Yoo, E. S. Park, J. Jeon, Y. J. Kwon, K. S. Woo, H. J. Kim, Y. K. Lee, and C. S. Hwang, *Nanotechnology*, **29**, 365202 (2018). [DOI: <https://doi.org/10.1088/1361-6528/aacda0>]
- [26] D. Dev, A. Krishnaprasad, M. S. Shawkat, Z. He, S. Das, D. Fan, H. S. Chung, Y. Jung, and T. Roy, *IEEE Electron Device Lett.*, **41**, 936 (2020). [DOI: <https://doi.org/10.1109/LED.2020.2988247>]
- [27] C. C. Chiang, V. Ostwal, P. Wu, C. S. Pang, F. Zhang, Z. Chen, and J. Appenzeller, *Appl. Phys. Rev.*, **8**, 021306 (2021). [DOI: <https://doi.org/10.1063/5.0038013>]
- [28] Y. Shi, X. Liang, B. Yuan, V. Chen, H. Li, F. Hui, Z. Yu, F. Yuan, E. Pop, H.S.P. Wong, and M. Lanza, *Nat. Electron.*, **1**, 458 (2018). [DOI: <https://doi.org/10.1038/s41928-018-0118-9>]
- [29] W. Yi, K. K. Tsang, S. K. Lam, X. Bai, J. A. Crowell, and E. A. Flores, *Nat. Commun.*, **9**, 4661 (2018). [DOI: <https://doi.org/10.1038/s41467-018-07052-w>]
- [30] M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, *Nat. Mater.*, **12**, 114 (2013). [DOI: <https://doi.org/10.1038/nmat3510>]
- [31] M. L. Gallo and A. Sebastian, *J. Phys. D: Appl. Phys.*, **53**, 213002 (2020). [DOI: <https://doi.org/10.1088/1361-6463/ab7794>]
- [32] T. Kaplan and D. Adler, Thermal, *Appl. Phys. Lett.*, **19**, 418 (2003). [DOI: <https://doi.org/10.1063/1.1653754>]
- [33] N. F. Mott, *The Philosophical Magazine: A Journal of*

Theoretical Experimental and Applied Physics, **24**, 911 (2006).

[DOI: <https://doi.org/10.1080/14786437108217058>]

- [34] D. Adler, M. S. Shur, M. Silver, and S. R. Ovshinsky, *J. Appl. Phys.*, **51**, 3289 (2008). [DOI: <https://doi.org/10.1063/1.328036>]
- [35] A. Cappelli, E. Piccinini, F. Xiong, A. Behnam, R. Brunetti, M. Rudan, E. Pop, and C. Jacoboni, *Appl. Phys. Lett.*, **103**, 083503 (2013). [DOI: <https://doi.org/10.1063/1.4819097>]
- [36] D. Ielmini, *Phys. Rev. B*, **78**, 035308 (2008). [DOI: <https://doi.org/10.1103/PHYSREVB.78.035308>]
- [37] H. M. Huang, R. Yang, Z. H. Tan, H. K. He, W. Zhou, J. Xiong, and X. Guo, *Adv. Mater.*, **31**, 1803849 (2019). [DOI: <https://doi.org/10.1002/adma.201803849>]
- [38] W. Xu, H. Cho, Y. H. Kim, Y. T. Kim, C. Wolf, C. G. Park, and T. W. Lee, *Adv. Mater.*, **28**, 5916 (2016). [DOI: <https://doi.org/10.1002/adma.201506363>]