International Journal of Advanced Smart Convergence Vol.11 No.4 96-103 (2022)
http://dx.doi.org/10.7236/IJASC.2022.11.4.96

IJASC 22-4-11

A Study of 0.5-bit Resolution for True-Time Delay of Phased-Array Antenna System

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Abstract

This paper presents the analysis of increasing the resolution of True-Time-Delay (TTD) by 0.5-bit for phased-array antenna system which is one of the Multiple-Input and Multiple Output (MIMO) technologies. For the analysis, a 5.5-bit True-Time Delay (TTD) integrated circuit is designed and analyzed in terms of beam steering performance. In order to increase the number of effective bits, the designed 5.5-bit TTD uses Single Pole Triple Throw (SP3T) and Double Pole Triple Throw (DP3T) switches, and this method can minimize the circuit area by inserting the minimum time delay of 0.5-bit. Furthermore, the circuit mostly maintains the performance of the circuit with the fully added bits. The idea of adding 0.5-bit is verified by analyzing the relation between the number of bits and array elements. The 5.5-bit TTD is designed using 0.18 μm RF CMOS process and the estimated size of the designed circuit excluding the pad is 0.57×1.53 mm^2. In contrast to the conventional phase shifter which has distortion of scanning angle known as beam squint phenomenon, the proposed TTD circuit has constant time delays for all states across a wide frequency range of 4 – 20 GHz with minimized power consumption. The minimum time delay is designed to have 1.1 ps and 2.2 ps for the 0.5-bit option and the normal 1-bit option, respectively. A simulation for beam patterns where the 10 phased-array antenna is assumed at 10 GHz confirms that the 0.5-bit concept suppresses the pointing error and the relative power error by up to 1.5 degrees and 80 mW, respectively, compared to the conventional 5-bit TTD circuit.

Keywords: *MIMO technology, Phased-array antenna, Phase shifter, True time delay, Beam Squint, Single pole triple throw switch, Double pole triple throw switch.*

1. Introduction

Recently, many studies related to the resolution improvement of the phase shifter are being conducted due to the development of the MIMO technology and the increase in demand in various application fields [1]-[3]. In particular, in the case of military phased-array antennas such as the Active Electronically Scanned Array (AESA), efforts are being made in various ways to secure a wide bandwidth related to the resolution of array antenna as Tx/Rx modules with a relatively narrowband characteristic have some limitations [4]. Distortion

Manuscript Received: October. 13, 2022 / Revised: October. 16, 2022 / Accepted: October. 17, 2022
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known as beam squint, one of the limitations of narrowband characteristics, can be effectively reduced through TTD circuit that can provide a relatively constant time delay over a wide frequency [5]. However, this circuit provides a couple of trade-offs: Firstly, the smaller the minimum time delay, the larger the circuit size because the parameters of the components supported in the RF integrated circuit process are quite limited. Secondly, the number of required circuit blocks increases as the steering angle is subdivided.

As a compromise between these trade-offs, this paper presents a concept to increase the resolution while minimizing the increase in the overall size of the circuit by inserting an additional delay option corresponding to 0.5-bit. Section 2 discusses the system architecture of the 5.5-bit TTD circuit with the proposed 0.5-bit option added. It also explains the role of SP3T and DP3T switches (one of the features distinguished from the conventional TTD topologies using only SPDT and DPDT switches) as well as the operation of the 0.5-bit system at each delay state. Section 3 presents the theoretical analysis on the effect of the proposed 0.5-bit TTD concept. In phased-array antenna system, the definition of the half power beam width derived from a beam pattern is given in degrees. Also, a minimum possible scanning angle can be defined by designers. The analysis is performed by using these two definitions. In section 4, the actual design of the 5.5-bit TTD circuit and simulation is performed. The performance of designed circuit is also discussed by applying the simple array antenna examples.

2. System Architecture

The conventional TTD circuit topology mainly uses only Single Pole Double Throw (SPDT) and Double Pole Double Throw (DPDT) switches, and each switch has one reference path and another delay path [6]-[9]. Subsequently, the number of delay cells present in each delay path becomes the number of bits of the TTD circuit, and the time value of the delay cell becomes $2^{(n-1)}$ times each step where n is the number of stages. As shown in Figure 1, the 0.5-bit delay option proposed in this paper is implemented by configuring the first stage of the conventional TTD system with SP3T and DP3T. Each path is connected to a reference path and delay cells corresponding to 0.5-bit and 1-bit. The delay cell used in 0.5-bit has a value of half of the time delay unit (TDU). The 0.5-bit option operates every second of normal 1-bit operations to compensate for nulls between each of the two states.

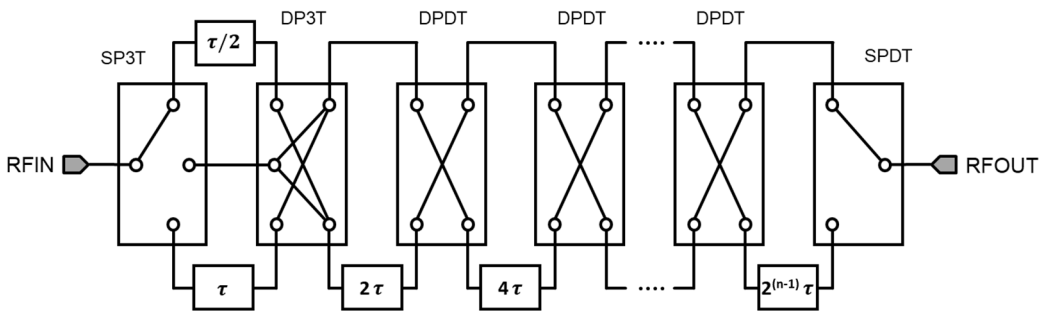


Figure 1. Block diagram of proposed TTD circuit

3. Theoretical Analysis on Effect of 0.5-bit TTD Applied to Array Antenna

The effect of adding 0.5-bit is demystified by analyzing the relation between the number of effective bits and the number of elements of the array antenna. In array antenna system, the minimum possible scanning angle θ_{LSB} in degrees can be defined as

$$\theta_{LSB} = \frac{\theta_{max}}{2^n} \tag{1}$$

where θ_{max} and n are the maximum scanning azimuth and the effective bit of TTD circuit, respectively. Also, the half power beam width (HPBW) of the beam pattern is approximated as

$$HPBW = \frac{50.764\,\lambda}{Nd\cos\theta}(deg) \tag{2}$$

where λ, N, d and θ are wavelength at the frequency being used, the number of array elements, distance between the elements and desired scanning angle, respectively [10]. The HPBW is the point at which the power of the array antenna's beam pattern is halved, and when the power goes below that point, the sensitivity of the transmission and reception systems may decrease. Therefore, the minimum possible scanning angle shall be equal to or smaller than HPBW so that the power of the beam pattern is sufficiently secured at a scanning angle not supported by the array antenna system. This can be expressed by the equations:

$$\theta_{LSB} \leq HPBW \tag{3}$$

$$\frac{\theta_{max}}{2^n} \leq \frac{50.764\,\lambda}{Nd\cos\theta} \tag{4}$$

To derive the relation between n and N, Equation 4 is organized as follows.

$$2^n \geq \frac{Nd\theta_{max}\cos\theta}{50.764\,\lambda} \tag{5}$$

After taking the log of both sides of Equation 5 and rearranging for n, the equation can be:

$$n \geq \frac{\log\left(\frac{Nd\theta_{max}\cos\theta}{50.764\,\lambda}\right)}{\log 2} \tag{6}$$

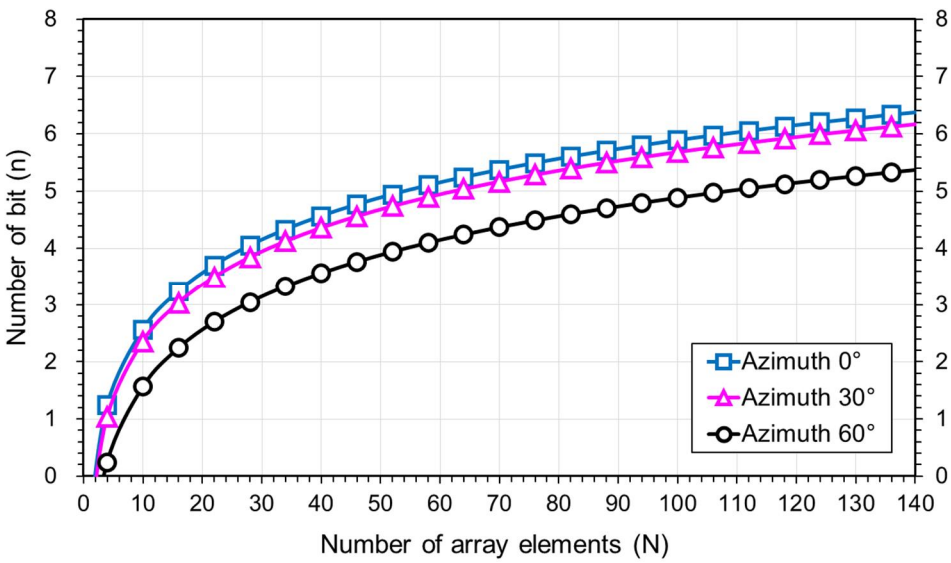


Figure 2. Estimated relation between effective bits and number of array elements

Figure 2 shows the result of plotting Equation 6 for n and N as an example when the maximum scanning angle is 60 degrees, d is $\lambda/2$, and frequency is approximated within the Ku-band. Analyzing the case where N is 70 and the azimuth is 0 degrees, the number of required TTD circuit bits is around 5.37, so using a TTD circuit with 6-bits rather than 5.5-bits can lead to cost increase due to excessive redundancy. Therefore, the proposed 0.5-bit concept can be recognized as a good alternative in terms of chip size reduction and cost reduction when designing an optimized TTD circuit.

4. Design and Analysis of 5.5-bit TTD Circuit

In this study, the design is conducted using the 0.18 μm generic RF CMOS process. The design phase can be divided into delay cells, switch circuits, and matching. For the first phase of the design, the π-network of a low-pass filter structure consisting of a series inductor and two shunt capacitors is used as a topology of a delay cell. The characteristic impedance and time delay are estimated respectively as follows [6].

$$Z_0 = \sqrt{L/C} \tag{7}$$

$$T_d = \sqrt{LC} \tag{8}$$

In equation 7, Z_0 is the characteristic impedance that is designed to have 50 Ω. In equation 8, T_d is the desired time delay and can be multiplied linearly as the desired time delay increases. For the proposed design, circuits are designed with delays of 1.1 ps and 2.2 ps corresponding to the 0.5-bit option and the least significant bit (LSB) respectively.

In the second phase, each switch to be used for the configuration of the TTD circuit is designed. Four types of switch designs are required to implement the circuit proposed in this paper. The base topology of all types of switches uses a series shunt structure consisting of a series MOSFET that operates as a switch and a ground shunt MOSFET that improves isolation characteristics. Inductors for better matching characteristics are added to the input and output terminals of each block.

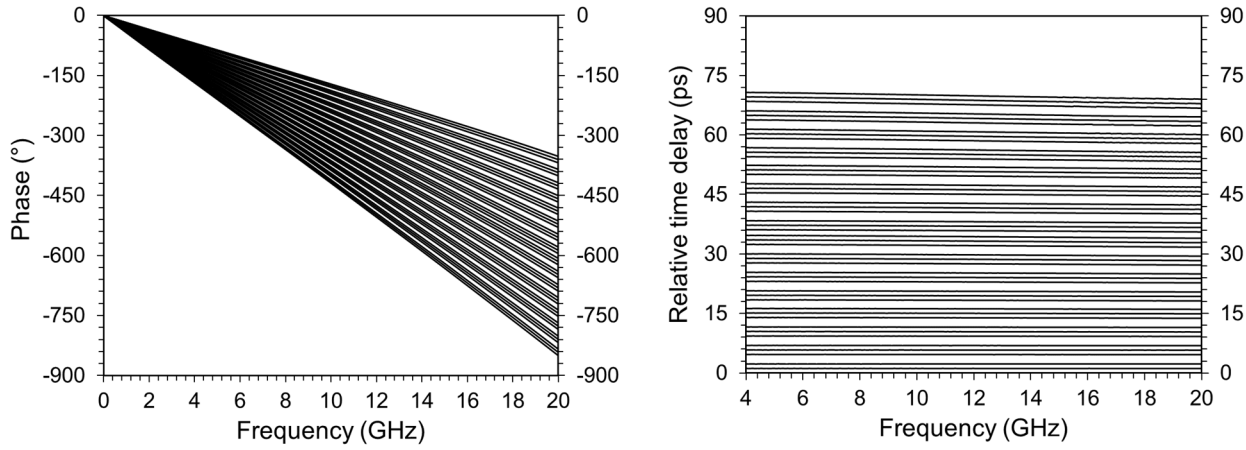
Finally, since the characteristic impedance of the delay circuit is set to 50 Ω, the input and output terminals of all blocks shall be matched accordingly. The matching is achieved through the previously added inductor, switch size, and isolation devices. As a result, the proposed TTD circuit has larger than around 14.7 dB of return losses and less than around 5.3 dB of insertion loss at all delay states in the 4-20 GHz frequency range.

The two delay functions normally used to determine the phase linearity of systems are the group delay and the relative time delay defined as

$$\tau_{GD} = -\frac{d\phi}{d\omega} \tag{9}$$

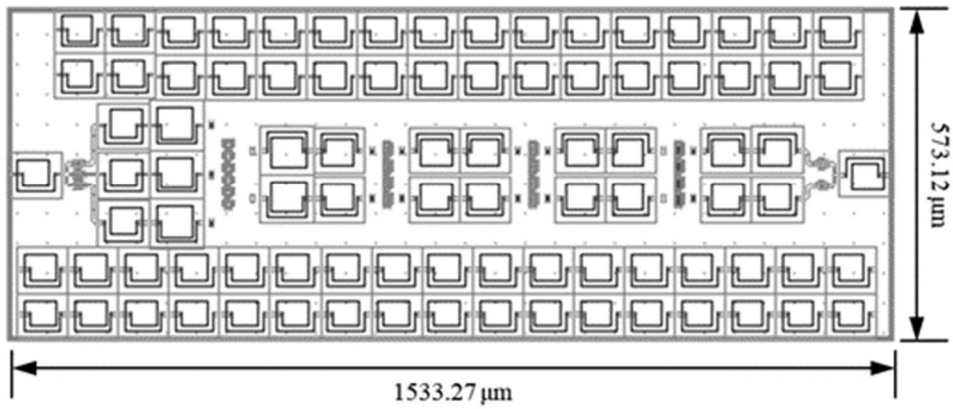
$$\tau_{TD} = -\frac{\phi}{\omega} \tag{10}$$

where ϕ and ω are the shifted phase in radians and the angular frequency in radians per unit time, respectively [9]. Figure 3(a) and 3(b) show the simulation results for the phases of designed 5.5-bit TTD circuit for all delay states and the relative time delays calculated with Equation 10, respectively. It can also be seen in Figure 3(b) that a constant time delay and a maximum relative time delay of almost 70 ps are achieved across the 4-20 GHz frequency range. Furthermore, the 0.5-bit option is identified for every second state of original states corresponding to the 1-bit.

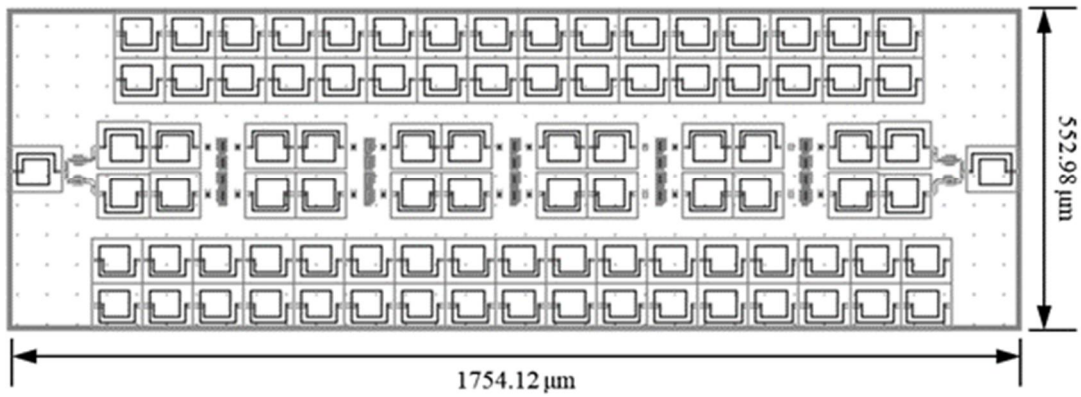


(a) (b)

Figure 3. Simulated (a) phases and (b) relative time delays of designed 5.5-bit TTD circuit for all delay states



(a)



(b)

Figure 4. Layout floor plan for (a) 5.5-bit TTD and (b) 6-bit TTD for size comparison

Table 1. Comparison of Estimated Specification of TTD Circuits according to Effective bits

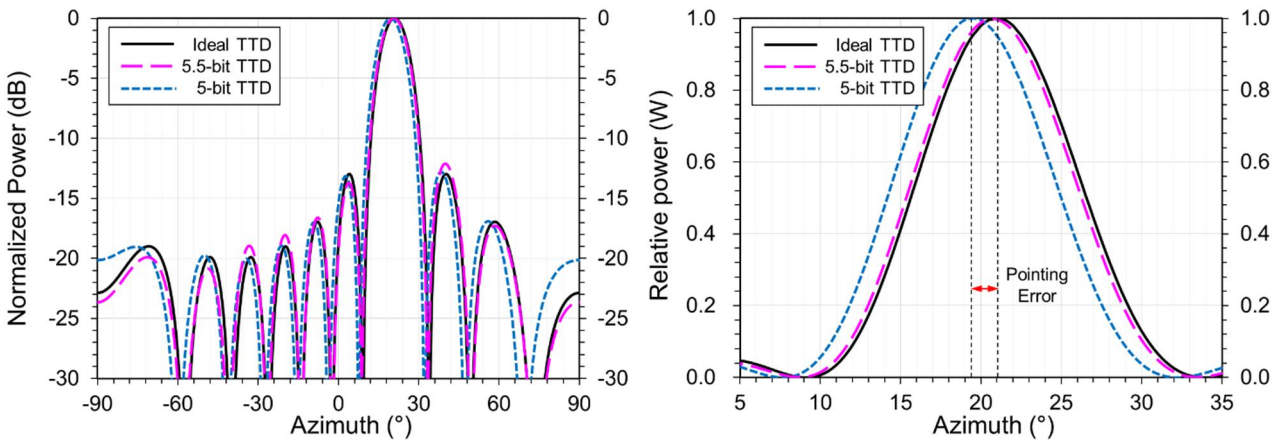
Effective bit	Number of states	Min. time delay unit (ps)	Estimated circuit area (mm^2)
4-bit	16	4.4	0.55×1.32
4.5-bit	24	2.2	0.57×1.41
5-bit	32	2.2	0.55×1.50
5.5-bit	48	1.1	0.57×1.53
6-bit	64	1.1	0.55×1.75

The physical layout floor plan is roughly designed for estimated size comparison as shown in Figure 4. Since inductors for better matching characteristics are placed at the input and output terminals, the size of the switch circuit is dominant to the number of inductors used. Therefore, a TTD circuit using the SP3T and DP3T switches can effectively reduce the total area of the circuit due to an effect similar to merging the two circuits.

Table 1 shows the number of states, the minimum time delay unit, and the expected circuit area according to the effective bit when the maximum time delay is set to 70.4 ps. Since the circuit area increased by adding the 0.5-bit option is smaller than the area increased by adding a full 1-bit, it can be a reasonable alternative in situations where an effective bit increase of TTD is required.

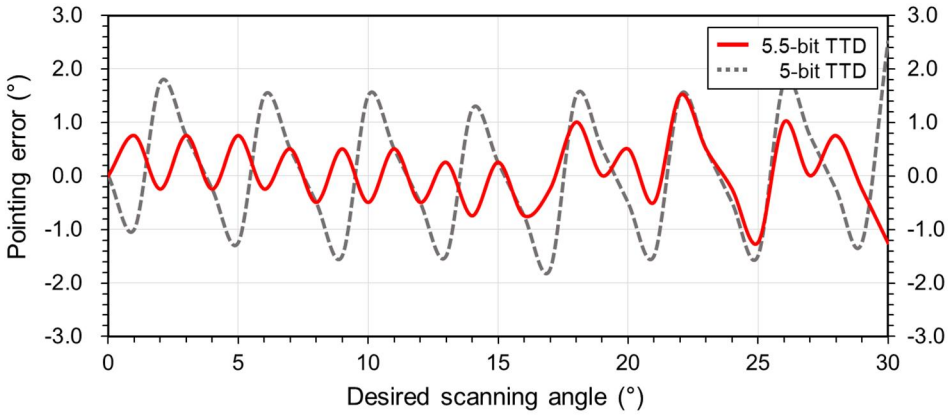
Figure 5(a) is an example of normalized beam patterns of an ideal TTD, 5.5-bit TTD and 5-bit TTD respectively for a 21-degree scanning. Since the array antennas for which 5-bit TTD and 5.5-bit are applied have different minimum steering angles, a pointing error different from the ideal beam pattern occurs during beam steering. In the array antenna beam pattern with a 5-bit TTD, the pointing error has a larger value than in the array antenna with a 5.5-bit TTD. This is represented in detail in Figure 5(b) where the relative power over azimuth is plotted in linear scale at a narrower angle.

The pointing error and relative power error are displayed in 1-degree increments from 0 to 30 degrees as shown in Figure 6. It can be seen that both pointing error and relative power error are improved when 5.5-bit TTD is applied. In particular, the relative power error shows a difference of up to 80 mW at a 2-degree scanning angle. Although these errors can be reduced by increasing the number of bits of the TTD circuit, limitations such as an enlarged circuit area are present due to a limited process.

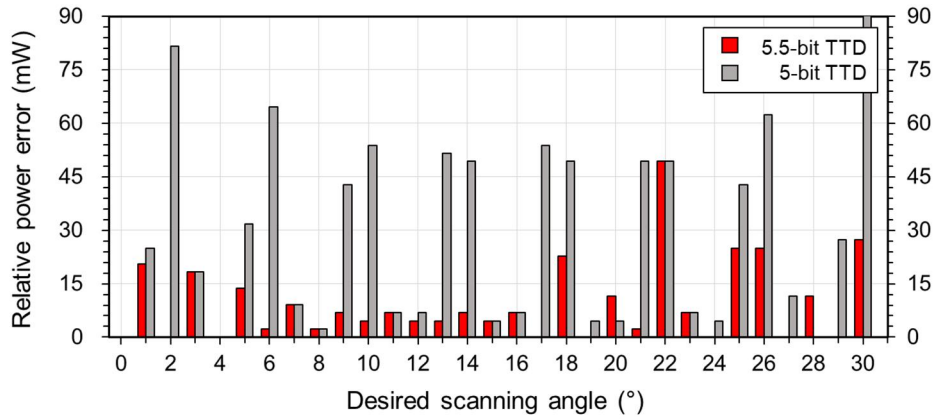


(a) (b)

Figure 5. Comparison of (a) normalized power and (b) related power between ideal, 5-bit, and 5.5-bit TTD circuits simulating at 21° scanning



(a)



(b)

Figure 6. Comparison of (a) pointing error and (b) relative power error for desired scanning angle between 5-bit and 5.5-bit TTD circuits

5. Conclusion

In this paper, a method of improving resolution for true time delay circuit in phased-array system is presented. The effect of adding 0.5-bit delay is analyzed by deriving the relation between the number of bit and the number of array elements. The derived relation shows that the number of bits required for the TTD circuit increases as the number of array elements increases. Therefore, the effect of the 0.5-bit delay option can be analyzed as a way to avoid excessive resolution margin. This concept is proved by designing a circuit having 5.5-bit of delay states using SP3T and DP3T switches for additional bit implementation in contrast to the conventional one using only SPDT switches or only SPDT and DPDT switches. It is confirmed that it has the insertion loss less than 5.3 dB, return losses better than 14.7 dB, and the constant time delay for a wide frequency range of 4-20 GHz. Also, the size of the designed 5.5-bit TTD circuit is estimated to have smaller increase than adding a bit to the 5-bit TTD circuit. Finally, the simulation results for phased array system with the proposed TTD confirmed performance improvement. Pointing errors and the relative power errors are suppressed by up to 1.5 degrees and 80 mW, respectively. Therefore, the proposed '0.5-bit-addition' is verified as a good way to increase the resolution of the TTD circuit with minimized circuit area and power consumption.

Acknowledgement

This work was supported by the Research Fund of Hankuk Univ. of Foreign Studies, and by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIT) (No.2020R1F1A1073315). The EDA tool was supported by the IC Design Education Center(IDEC), Korea.

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