Journal of Convergence for Information Technology
Vol. 11. No. 11, pp. 159-165, 2021
e-ISSN 2586-4440
DOI : https://doi.org/10.22156/CS4SMB.2021.11.11.159

Three-Dimensional Selective Oxidation Fin Channel MOSFET Based on Bulk Silicon Wafer

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벌크 실리콘 기판을 이용한 삼차원 선택적 산화 방식의 핀 채널 MOSFET

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Abstract A fin channel with a fin width of 20 nm and a gradually increased source/drain extension regions are fabricated on a bulk silicon wafer by using a three-dimensional selective oxidation. The detailed process steps to fabricate the proposed fin channel are explained. We are demonstrating their preliminary characteristics and properties compared with those of the conventional fin field effect transistor device (FinFET) and the bulk FinFET device via three-dimensional device simulation. Compared to control devices, the three-dimensional selective oxidation fin channel MOSFET shows a higher linear transconductance, larger drive current, and lower series resistance with nearly the same scaling-down characteristics.

Key Words : SoxFET, FinFET, Bulk FinFET, Raised Source/Drain, Series resistance, Recess channel

요 약 본 삼차원 선택적 산화를 이용하여 20 nm 수준의 핀 폭과 점진적으로 증가된 소스/드레인 확장 영역을 갖는 핀 채널을 벌크 실리콘 기판에 제작하였다. 제안된 기법을 이용하여 삼차원 소자를 제작하기 위한 공정기법 및 단계를 상세히 설명하였다. 삼차원 소자 시뮬레이션을 통해, 제안된 소자의 주요 특징과 특성을 기존 FinFET 및 벌크 FinFET 소자와 비교하였다. 제안된 삼차원 선택적 산화 방식의 핀 채널 MOSFET는 기존의 소자들과 비교하여 더 큰 구동 전류, 더 높은 선형 트랜스컨덕턴스, 더 낮은 직렬 저항을 가지며, 거의 유사한 수준의 소형화 특성을 보이는 것을 확인하였다.

주제어 : SoxFET, FinFET, 벌크 FinFET, 상승 소스/드레인, 직렬저항, Recess 채널

1. Introduction

The multiple gate metal oxide semiconductor field effect transistor (MOSFET) is widely recognized as promising candidates for ultimate scaling of MOSFETs to the shortest channel length[1-3]. Among the multiple gate devices, the fin field effect transistor device (FinFET) is in the spotlight for its simple process, which is compatible with the conventional planar process[4]. FinFETs have been fabricated on silicon on insulator (SOI) substrates to overcome the problems associated with the

*This study was supported by the Research Program funded by the SeoulTech(Seoul National University of Science and Technology).
*This article is extended and excerpted from the conference paper presented at International Microprocesses and Nanotechnology Conference
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Received September 9, 2021 Revised October 20, 2021
Accepted November 20, 2021 Published November 28, 2021

short channel effect. However, FinFETs built on SOI wafers suffer from heat dissipation issues and floating body problems[5,6]. In addition, it is still expensive adapting the SOI wafers.

Recently, the FinFET fabricated on bulk Si substrates is known to solve these problems[7]. The bulk FinFET has advantages over the conventional SOI FinFET, but it still remains issues. One of the major challenges in making Si FinFET is to make small and controllable fin width to suppress of short channel effects. Ashing and trimming technology[8], spacer lithography technology[9] and e-beam lithography technology[10] have been produced, but the plasma damage is occurred on the sidewall of the fin channel during reactive ion etching process. The other problem is enabling high drive current capability by reducing the source/drain (S/D) parasitic series resistance. Selective epitaxial re-growth process[11,12] has been proposed to thicken the fin outside of the gate region, but it needs well-formed sidewall spacers which isolate the fin from the gate.

In this paper, we propose the selective oxidation fin channel MOSFET (SoxFET) based on a bulk Si wafer to yield extremely narrow fin structure and reduced parasitic series resistance using the simple recess-channel technology over a 0.5 μm CMOS process[13,14]. This article is extended and excerpted from the conference paper presented at[15]. The proposed process is more robust and much simpler than other techniques for the same purpose using selective epitaxial re-growth process. The detailed fabrication procedure is explained to form a proposed device. Finally, the electrical characteristics of the SoxFET are compared with those of the bulk FinFET and the conventional FinFET using three- dimensional device simulation.

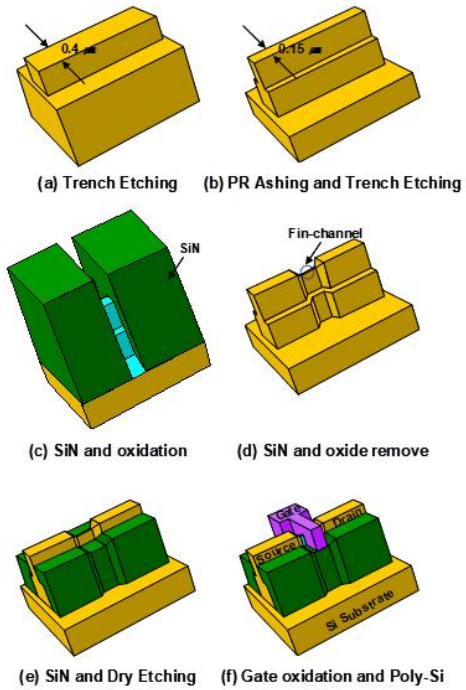

Fig. 1. Three-dimensional process flow of the SoxFET

2. Experimental Implementation

The device structure and the schematic process flow of the proposed SoxFET are shown in Fig. 1. In the implementation of the SoxFET, it is important to achieve controllable dimensions for the fin width because it alleviates short channel effects and governs off-state leakage current. The critical process steps for fin channel formation of the SoxFET are explained as follows. As the starting material, a (100) p-type silicon wafer was used. A photoresist was coated and 0.5 ㎛ design-ruled i-line photolithography steps were taken to define the active region. Trenchs were etched with a width of 400 nm and depth of 250 nm (Fig. 1(a)). The 400 nm silicon film was shrunken to 150 nm by photoresist ashing and dry etching (Fig. 1(b)). The above process steps are not required if the state-of-the-art design rule lithography becomes possible. These processes were performed solely for nanoscale

fin channel fabrication with the conventional micro-meter order lithography technology. The remaining 150 nm width silicon pattern serves as a starting material to oxidation during the subsequent thermal process. A thermal oxide with a thickness 10 nm was grown; a 300 nm SiN layer was deposited. Through sufficient over-etching, the SiN was fully removed from the center of the active pattern. Next, the thermal oxide layer was grown for 35 min at 950 °C in O_2 to make a thinned fin-channel. Unlike the silicon oxide layer, the SiN does not allow oxygen to permeate. Therefore, a thermal oxide layer was created at only a portion where the gap was produced, i.e., the portion of the channel and S/D extension regions (Fig. 1(c)). After the oxidation barriers composed of SiN were removed, the thermal oxide was also removed by wet etching. The shape of the fin channel resembling a bird's beak is shown in Fig. 1 (d). Owing to the three-dimensional selective oxidation, it is possible to fabricate the raised S/D structure without epitaxial growth or layer deposition which has gradually increased connection regions from the channel to S/D regions. These thickened S/D regions help to improve overall parasitic series resistances.

A thermal oxide of 10 nm thickness was grown and a SiN layer of 250 nm thickness was deposited. With dry etching, the removal of SiN layer was stopped in the middle of the silicon sidewall by about 80 nm below the silicon top surface. A 10 nm buffer oxide, which had been underneath the SiN layer, was etched in a diluted HF solution. A 150 nm thick tetraethyl orthosilicate (TEOS) and a 150 nm poly-Si were deposited for scanning electron microscope (SEM) image.

3. Results and Discussions

A top down SEM image of the selective oxidation test pattern taken after the center oxidation layer removing and a cross-sectional SEM image of the silicon fin channel across the gate taken after the SiN layer removing are shown in Fig. 2 (a) and (b), respectively. Because of the three-dimensional selective oxidation, gradually increased extension regions from the channel to S/D regions were fabricated which are advantageous to decrease parasitic resistance and the top corners of the fin channel were rounded which are helpful to suppress possible leakage along the top corners. The width (W_{fin}) and height (H_{fin}) of the fin channel are 20 nm and 80 nm, respectively. An extremely small fin width and height beyond the lithographic limit is obtained with three-dimensional selective oxidation technology.

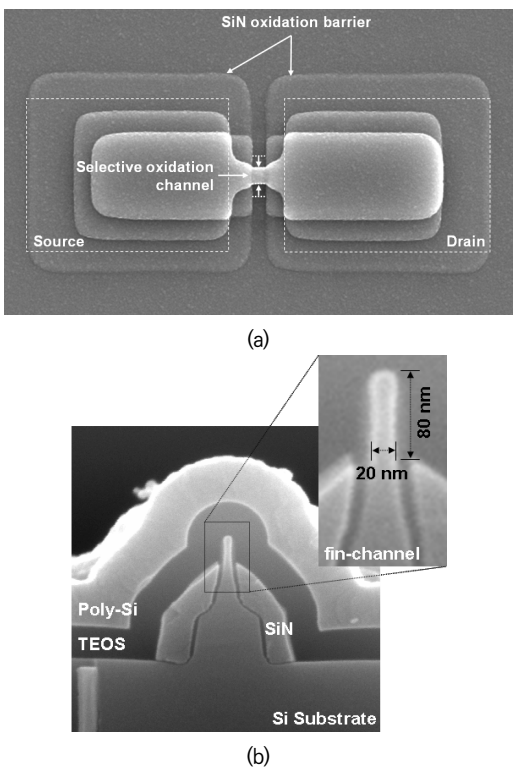

Fig. 2. (a) Top down SEM image of the test pattern taken after the center oxidation layer removing, (b) Cross-sectional SEM image of the SoxFET's fin structure after SiN layer dry etching

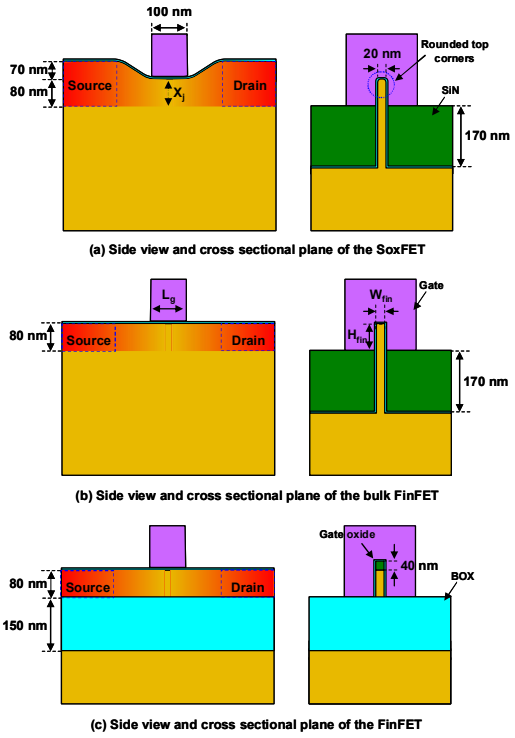

Fig. 3. Schematic diagrams of side view and cross sectional plane of three devices

Electrical characteristics of the SoxFET, the bulk FinFET [7] and the conventional FinFET [3], as illustrated in Fig. 1 (f) are simulated using the Device3D Atlas software package from Silvaco. Schematic diagrams of side view and cross sectional plane of the three devices are described in Fig. 3. W_{fin} and H_{fin} of the fin channel are 20 nm and 80 nm, respectively, while the gate oxide thickness (T_{ox}) is 2 nm. For the conventional FinFET device, the buried-oxide thickness is 150 nm, and the oxide hard mask thickness is 40 nm. To avoid adverse effects associated with heavy doping, the boron concentration in the channel (NA) is uniform and equal to $1x10^{16}/cm^3$. S/D extension region and n+ S/D regions doping (ND) profile is set as Gaussian with peak concentration of $2x10^{19}/cm^3$. The lateral doping abruptness was 1 nm /dec, and the gate direct overlap length was 3 nm. The junction depth (X_j) is defined from the top surface of the fin and here the junction depth is 80 nm. The work function of the n^+ poly-Si gate (Φ_M) is chosen as 4.17 eV. All the device parameters included positions and shapes of S/D contacts of the SoxFET are equivalent to those of the bulk FinFET and the FinFET unless otherwise stated for the purpose of comparative analysis.

The I_d-V_{gs} characteristic and the linear transconductance (G_m) of the SoxFET are compared with those of control devices in Fig. 4. The gate length (L_g) of devices is fixed at 100 nm. The on-state current (I_{on}) of the proposed device is 117 μA at V_{gs}=1.0V and V_{ds}=0.1 V, which is 2.04 and 2.58 times larger than those of the bulk FinFET and the conventional FinFET, respectively. These improvements in the performances are because of the raised S/D structure of the SoxFET, which reduces the parasitic series resistance at S/D extension regions. In other words, the on-state current is mainly affected by the series resistance introduced at extension regions. The maximum linear transconductance ($G_{m,max}$) of the SoxFET shows 1.44 times larger than control devices at V_{ds}=0.1 V. As the gate bias increases, the proposed structure shows a lower degradation in G_m compared to those of control devices which is also due to the lower S/D parasitic series resistance.

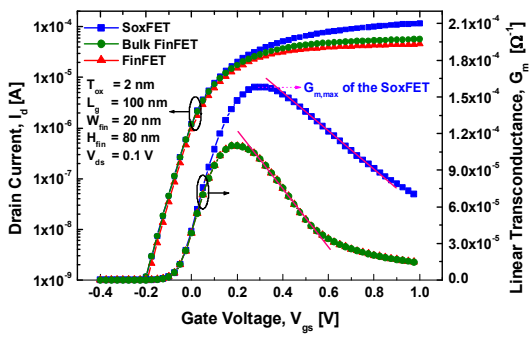

Fig. 4. Comparison of the Id-Vgs characteristic and linear transconductance characteristic of the SoxFET, bulk FinFET and FinFET

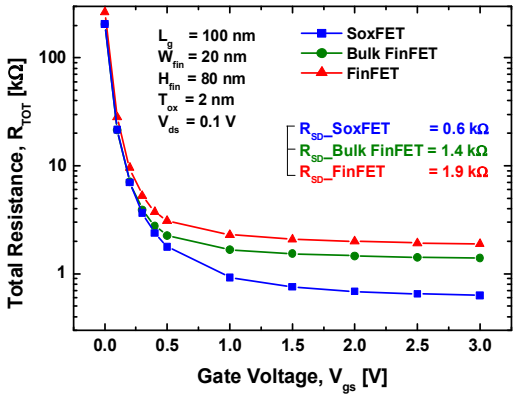

Fig. 5. Total resistance as a function of gate voltage for three devices

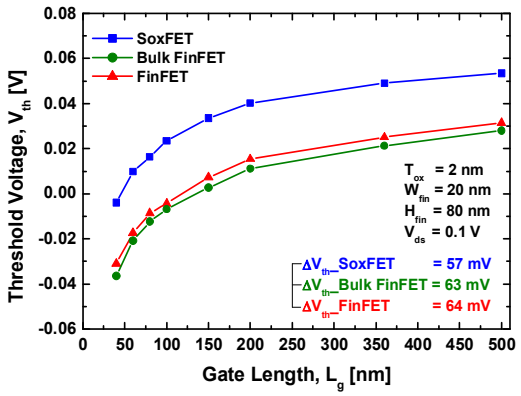

Fig. 6. The threshold voltage roll-off with different structures and different gate length

The on-state current and transconductance improvement should be attributed to the reduction in the S/D resistance. As a result, we extracted the total parasitic resistance at the channel and S/D regions by use of following method. The total resistance of a MOSFET R_{TOT} is calculated by the sum of the channel resistance R_{CH} and parasitic S/D resistance R_{SD}, which is also expressed as V_{ds}/I_S[16]. At low V_{ds} and infinitely large V_{gs}, R_{CH} diminishes and R_{TOT} becomes equal to R_{SD}. The total resistance has been extracted as a function of V_{gs} and is plotted in Fig. 5. It can be seen from Fig. 5 that for high V_{gs} values, R_{TOT} becomes constant, and is taken as R_{SD}. The parasitic S/D resistance is significantly improved for SoxFET (0.6 kΩ), compared to conventional FinFET (1.9 kΩ) and bulk FinFET (1.4 kΩ). The parasitic S/D resistance has been extracted from R_{TOT}-V_{gs} curve at V_{gs}=5 V, and V_{ds}=0.1 V. By self-constructed raised S/D structure of the SoxFET, the parasitic S/D resistance can be reduced, resulting in improved transconductance and drive current. Nevertheless, parasitic capacitances between the S/D and the gate are inherent in the SoxFET. This is expected to adversely impact the device speed and power consumption. There is a tradeoff between series resistance and gate parasitic capacitances.

In Fig. 6, the threshold voltage of SoxFET according to the channel length is compared with those of the bulk FinFET and conventional FinFET. The threshold voltage roll-off is defined as the threshold voltage (V_{th}) which is determined as the intersection between V_{gs} axis and extrapolated linear region of I_d-V_{gs} curve measured at V_{ds}=0.1 V at any gate length while the silicon substrates are kept grounded at all times. Note that threshold voltages are relatively low compared to other fin channel structures because channel doping to adjust the threshold voltage was not performed. It can be seen that V_{th} roll-off is minimized by the use of the proposed structure, but other devices show an excellent behavior as well. The self-constructed raised S/D structure of the SoxFET plays a very important role in suppressing V_{th} roll-off originating from drain potential extension into the source region. For the planar structure, the potential is strongly perturbed by the drain voltage and the potential barrier is removed in the channel region, in contrast to the raised S/D structure for which the potential barrier is only slightly affected in the drain region. Thus, the effects of the raised S/D structure of the SoxFET reduce the charge sharing in the channel, increase V_{th}, and alleviate V_{th} roll- off. Similar results were reported by Waite et al.[17] and Huang et al.[18] on transistor with raised S/D.

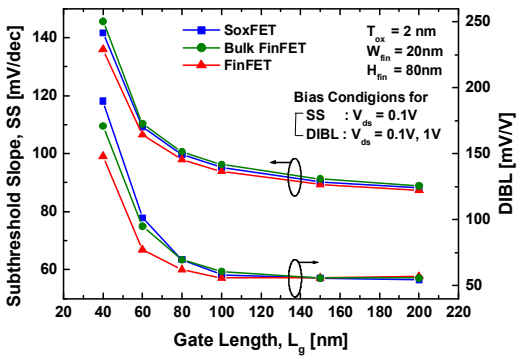

Fig. 7. The subthreshold slope and drain induced barrier lowering characteristic of the SoxFET compared with those of the bulk FinFET and FinFET

Fig. 7 shows the subthreshold slope (SS) and the drain induced barrier lowering (DIBL) comparisons dependence on the gate length. The SS was evaluated from the maximum slope in the I_d-V_{gs} characteristics at V_{ds}=0.1 V and DIBL was evaluated as the gate voltage shift between V_{ds}=0.1 V and V_{ds}=1.0 V curves at I_d=10^{-8} A. It can be observed that the SS and DIBL are minimized by the use of the conventional FinFET, but the SoxFET shows an excellent behavior as well. According to the current industry criterion for high performance applications, SS under 100 mV/dec and DIBL must be kept below 100 mV/V. Under these criteria, we can establish a guideline for minimum gate length to avoid short channel effects. In the case of the SoxFET with H_{fin}=80 nm, W_{fin}=20 nm, N_A=1x10^{16}/cm^3, and N_D= 2x10^{19}/cm^3 the minimum gate length decreased to 80 nm. In Table I, the electrical characteristics of the three devices are summarized.

4. Conclusion

A 20 nm thick fin channel and gradually increased S/D extension region are fabricated on a bulk silicon wafer using a three-dimensional selective oxidation. While verifying the DC characteristics of the SoxFET, the proposed device revealed larger on-current and linear transconductance. We believe that they are responsible for the improved on S/D parasitic resistance, while maintaining the threshold voltage roll-off, SS and DIBL. Therefore, a device geometry of the SoxFET is shown to be a promising solution for minimizing the parasitic S/D resistance of narrow fin devices. Based on simulation and measurement results, if additional device processes are developed along with the formation of the fin structure, it can contribute to the filed of low-cost and high-integration nm-scale CMOS devices in the near future.

Table 1. Summarized electrical characteristics of the SoxFET, bulk FinFET and FinFET.

	SoxFET	Bulk FinFET	FinFET
I_{on}(μA)	117	57.1	45.4
$G_{m,max}$(Ω^{-1})	1.58x10^{-4}	1.1x10^{-4}	1.1x10^{-4}
R_{SD}(kΩ)	0.6	1.4	1.9
V_{th}(V)	0.024	−0.007	−0.004
SS(mV/dec)	95.25	96.28	93.90
DIBL(mV/V)	58.23	60.76	55.70

The device parameters are: H_{fin}=80 nm, W_{fin} =20 nm, T_{ox}=2 nm, L_g=100 nm, X_j=80 nm, N_A=1x10^{16}/cm^3, N_D=2x10^{19} /cm^3, and Φ_M=4.17 eV.

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