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Quadrature VCO as a Subharmonic Mixer

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Abstract

This paper proposes two types of subharmonic RF receiver front-end (called LMV) where, in a single stage, quadrature voltage-controlled oscillator (QVCO) is stacked on top of a low noise amplifier. Since the QVCO itself plays the role of the single-balanced subharmonic mixer with the dc current reuse technique by stacking, the proposed topology can remove the RF mixer component in the RF front-end and thus reduce the chip size and the power consumption. Another advantage of the proposed topologies is that many challenges of the direct conversion receiver can be easily evaded with the subharmonic mixing in the QVCO itself. The intermediate frequency signal can be directly extracted at the center taps of the two inductors of the QVCO.

Using a 65 nm complementary metal oxide semiconductor (CMOS) technology, the proposed subharmonic RF front-ends are designed. Oscillating at around 2.4 GHz band, the proposed subharmonic LMVs are compared in terms of phase noise, voltage conversion gain and double sideband noise figure. The subharmonic LMVs consume about 330 μW dc power from a 1-V supply.

Keywords: *CMOS, LMV Cell, Phase Noise, Quadrature, Subharmonic Mixer, Voltage-controlled Oscillator*

1. Introduction

Highly integrated, low-power, and low-voltage circuits are always the main topics for integrated circuit design and especially important for mobile wireless communication systems due to the battery life. Single stage circuits combining mixer and oscillator have been designed for the purpose of a higher integration and reducing power consumption. For highly integrated low-power receiver front-end, a current reuse technique is typically adopted across different functional blocks. A popular method is cascoding the mixer on top of the input stage of the low-noise amplifier (LNA), while less frequent is stacking mixer and voltage-controlled oscillator (VCO) [1-2].

In [1], a double balanced mixer is stacked on top of the voltage-controlled oscillator (VCO) by using the current reuse topology. The radio frequency (RF) input signal is applied to the input of the mixer, and the oscillator signal is applied to the source nodes of the mixer. Moreover, this topology applies a separate dc bias to the VCO. In [2], the RF front-end merges LNA, mixer, and VCO (called LMV) in a single stage. This topology stacks VCO on top of the mixer. The current source of the mixer is modified as the LNA with inductor

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degeneration. Since the intermediate frequency (IF) outputs are connected to the source nodes of the VCO, the voltage gain is limited due to the low impedance at the source nodes. In [3-4], the VCO itself plays the role of mixer while generating the oscillation frequency. This topology adopts the concept of 'VCO as a fundamental mixer' instead stacking the separate VCO and mixer by exploiting the series LC tank resonator. All of the topologies in [1-4] are based on the fundamental local oscillator (LO) generation which is more susceptible to many challenges of the direct conversion receiver since the frequencies of RF and LO are same.

In this paper, two subharmonic LMVs are proposed based on the quadrature VCO (QVCO) topologies by stacking the QVCO on top of the LNA. Instead of the 'fundamental mixer', the proposed topologies adopt the concept of 'VCO as a subharmonic mixer' by applying the different RF and LO frequencies. The direct advantage of stacking across the RF blocks, the dc power consumption in the RF front-end can be significantly reduced. Another merit of the proposed topologies is that many challenges in the direct conversion receiver can be easily evaded. This paper is organized as follows. In Section 2, several challenges for the direct conversion receiver architecture are described and methodologies are suggested to evade the LO self-mixing by using the subharmonic mixers. Also, a detailed mathematical analysis for the sub-harmonic mixer is described. In Section 3, subharmonic LMV design concepts are described and experimental results are given based on simulation using 65 nm CMOS technology. Finally, a conclusion is given.

2. Direct Conversion RF Front-end Receiver

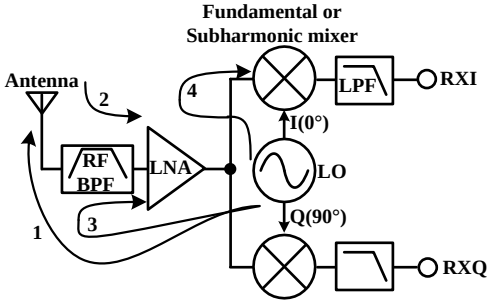


Figure 1. Direct conversion RF front-end receiver and possible paths for self-mixing.

Considering the direct conversion receiver in Figure 1, the frequency of the RF signal (f_{RF}) passes through the antenna, RF band-pass filter (BPF) and LNA, and down-converted directly to the baseband with the mixers by injecting the LO signal (f_{LO}). The down-converted receiver signals are then filtered furthermore with the low-pass filters (LPF) to reject the higher frequencies. Then, the filtered receiver (RX) signals are then fed to the following blocks for signal processing furthermore. While the elimination of the IF filter is a significant advantage to using direct conversion receiver architecture, there are many challenges that must be overcome. One of the most significant is the LO self-mixing, which can seriously degrade the receiver performance with increased intermodulation distortion and noise [5]. Since the RF carrier is directly converted to near dc, any dc offsets created by the mixer itself can interfere with the desired signal (many efficient modulation schemes have significant spectral content at or near dc).

There are several possible paths for LO self-mixing, as shown in Figure 1 [6]. Path 1 represents the LO signal coupling to the antenna where it is radiated and reflections of this signal by nearby objects are received by the antenna as shown in Path 2. Path 2 can also represent a strong nearby interfering signal that is received by the antenna and can couple to the LO port and self-mix, also producing a dc offset. Path 3 represents LO coupling to the input of the LNA, which can be particularly problematic since it will then be amplified along with the RF signal before entering the RF port. Path 4 represents the LO signal that is coupled to the RF port of the mixer, which will then mix with itself and produce a dc offset. Whereas Paths 3 and 4 would generate static dc offsets, the results of Paths 1 and 2 would be dynamic due to the changing operating environment.

To tackle the LO self-mixing problem, several techniques have been suggested such as the use of a subharmonic mixer and the use of a frequency doubler at the output of the LO [7]. While fundamental mixers could be used in Figure 1, subharmonic mixers are very attractive since they can reduce LO self-mixing by

using an LO frequency that is much lower than the RF. This lowered LO frequency enables several benefits such as ease of design and improved LO phase noise. A reduction in LO phase noise can result in a lower receiver noise figure (NF) and improved receiver sensitivity. A reduced dc power consumption of the LO might also be possible since it operates at a much lower frequency when using a subharmonic mixer, which would ultimately result in a longer battery life for mobile devices. In a similar way, for a direct conversion transmitter, the leakage from the power amplifier is so strong and takes severe effect on the LO (called LO pulling). This LO pulling can be effectively evaded by using a subharmonic mixer since the frequency of LO is different from the RF frequency.

As shown in Figure 1, the direct conversion receiver typically requires accurate in-phase (I) and quadrature (Q) LO signals which can be generated by the QVCO. The QVCO is the popular topology to achieve low phase noise using LC-tuned resonator. The most common QVCO is called parallel QVCO (P-QVCO) which couples two VCOs in quadrature with parallel coupling transistors. Another method is called S-QVCO which couples two VCOs in a cascode-like way [8]. While the P-QVCO has low phase and amplitude errors, it has rather poor phase noise performance. On the contrary, the S-QVCO exhibits good phase noise performance with good quadrature accuracy.

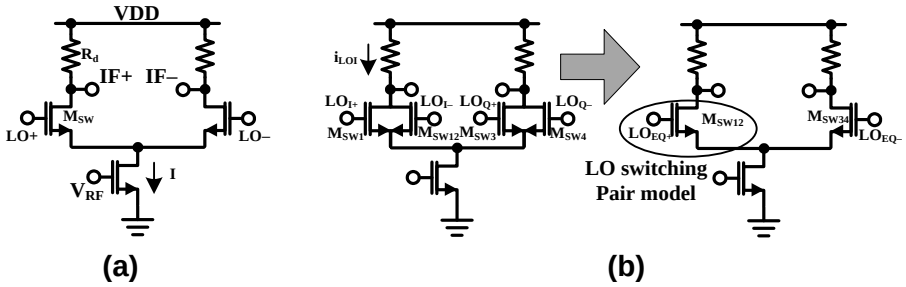


Figure 2. (a) conventional fundamental mixer and (b) SHM.

Figure 2 shows the conventional and subharmonic mixers (SHM). While single switching transistor (M_{SW}) mixes the RF signal with the fundamental LO signal for the conventional mixer, the mixing is achieved with two switching transistors which is connected in parallel for the SHM. The two parallelly connected switching transistors allow the mixing of the RF signal with the doubled frequency of the LO signal.

Following the analytic procedures given in [9], the LO inputs to the subharmonic mixer Figure 2(b) are given by

$$\begin{aligned} v_{LOI+} &= A_{LO}\cos(\omega_{LO}t) \\ v_{LOI-} &= A_{LO}\cos(\omega_{LO}t - \pi/2) \\ v_{LOQ+} &= A_{LO}\cos(\omega_{LO}t - \pi) \\ v_{LOQ-} &= A_{LO}\cos(\omega_{LO}t - 3\pi/2) \end{aligned} \quad (1)$$

and the single-ended RF input to the mixer is

$$v_{RF} = A_{RF}cos(\omega_{RF}t) \quad (2)$$

where A_{LO} and A_{RF} are the amplitudes, and ω_{LO} and ω_{RF} are the angular frequencies of the LO and RF signals, respectively.

To gain more insight into the operation of the SHM, a mathematical expression for the conversion gain of the mixer can be derived. Here, the long-channel transistor models are used for simplicity in order to obtain useful closed-form equations. In the half-SHM circuit shown in Figure 2(b), the LO switching pair transistors M_{SW1} and M_{SW2} are modeled as a single transistor, M_{SW12}. Assuming that the fundamental currents generated by the differential gate voltage signals on M_{SW1} and M_{SW2} perfectly cancel each other, the non-linear component at twice the input frequency is the only signal current that remains. Therefore, M_{SW1} and M_{SW2} are modeled as one transistor with an applied gate voltage signal at a frequency of $2\omega_{LO}$. Transistors M_{SW3} and M_{SW4} in Figure 2(b) can also be replaced by a single equivalent transistor M_{SW34}. The long-channel drain current approximation for a MOSFET in saturation is given by

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2 \quad (3)$$

where μ_n is the electron mobility, C_{ox} is the gate capacitance, v_{GS} is the gate-source voltage, V_t is the threshold voltage, and W/L is width over length of the switching transistors (M_{SW1}~M_{SW4}). If the currents through M_{SW1} and M_{SW2} are i_1 and i_2, respectively, the total current from the switching pair with a differential input is

$$i_{LOI} = i_1 + i_2 = \mu_n C_{ox} \frac{W}{L} \left(V_{GS(LO)} - V_t\right)^2 + \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (v_{LOI+}^2 + v_{LOI-}^2) \quad (4)$$

where $V_{GS(LO)}$ is the dc voltage between the gates and sources of the LO transistors. Since $v_{LOI+}^2 = v_{LOI-}^2$ for a sinusoidal LO signal,

$$i_{LOI} = \mu_n C_{ox} \frac{W}{L} \left(V_{GS(LO)} - V_t\right)^2 + \mu_n C_{ox} \frac{W}{L} v_{LOI+}^2 \quad (5)$$

Ignoring the nonlinear component, the current in (5) can then be set equal to the current generated by the M_{SW12} switching pair model transistor,

$$i_{LOI} = \frac{1}{2} \mu_n C_{ox} \frac{W_{EQ}}{L} \left(V_{GS(LO)} - V_t\right)^2 + \mu_n C_{ox} \frac{W_{EQ}}{L} (V_{GS(LO)} - V_t) v_{LOEQ+} \quad (6)$$

where W_{EQ} is the equivalent width of the M_{SW12} and M_{SW34}.

Clearly, in order to have equal dc currents, the width of transistor M_{sw12} must be twice that of M_{sw1} and M_{sw2}, $W_{EQ} = 2W$. The equivalent applied gate signal voltages to the LO switching pair model transistors, M_{sw12} and M_{sw34}, are

$$v_{LOEQ+} = \frac{A_{LO}^2}{2(V_{GS(LO)} - V_t)} \cos^2(\omega_{LO} t) \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} \cos(2\omega_{LO} t) \quad (7)$$

$$v_{LOEQ-} = \frac{A_{LO}^2}{2(V_{GS(LO)} - V_t)} \cos^2(\omega_{LO} t + \pi) \approx \frac{A_{LO}^2}{4(V_{GS(LO)} - V_t)} \cos(2\omega_{LO} t + \pi) \quad (8)$$

The approximation made in the equations (7) and (8) was to ignore the dc component of the $\cos^2$ term. The output voltage of the mixer is given by

$$v_{out} = \frac{-R_d v_{RF}}{V_{GS(RF)} - V_t} \left(i_{LOI} - i_{LOQ}\right) = \frac{-R_d I}{(V_{GS(RF)} - V_t)(V_{GS(LO)} - V_t)} v_{RF} \left(v_{LOEQ+} - v_{LOEQ-}\right) \quad (9)$$

where v_{RF} is the RF signal voltage, R_d is the load resistor, and $V_{GS(RF)}$ is the dc voltage between the gate and source of the RF transistor. The conversion gain (CG) expression for this subharmonic mixer for the down-converted signal is given by

$$CG_{dB} = 20\log\left(\frac{R_d I A_{LO}^2}{4(V_{GS(RF)} - V_t)(V_{GS(LO)} - V_t)^2}\right) \quad (10)$$

where I is the bias current set by the gate voltage of the RF transistor and all transistors are operating in the saturation region. The values for $V_{GS(RF)}$ and $V_{GS(LO)}$ can be found from a straight-forward dc circuit analysis. From this equation, it is clear that the conversion gain will increase with increasing the bias current, I.

3. Subharmonic LMV Design

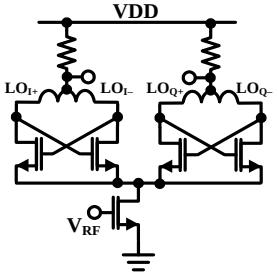


Figure 3. Proto-type subharmonic oscillator-mixer.

A conventional differential LC tank VCO with a current source can be considered as a mixer when an RF signal is applied to the gate of the current source. The down-converted IF signal at the VCO output is negligible

since the inductor in the high-Q LC tank is a short due to the low impedance at the low frequency. Attempting to sense the down-converted signal at the output of the VCO unavoidably degrades the oscillator phase noise [2]. If a series resonator is employed, the impedance is high at the low frequency and the IF signal can be recovered without any signal loss [3-4]. To use the differential VCO itself as a mixer, it could be adopted to the subharmonic mixers without using the series LC resonator.

Figure 3 shows the proto-type subharmonic oscillator-mixer where the two pairs of parallelly connected switching transistors are modified as cross-coupled VCO with two inductors. The remaining task is to run the two VCOs in quadrature. Figure 4 shows the proposed SH LMVs where two VCOs are quadrature coupled using the topologies of P-QVCO and S-QVCO. The IF signal can be sensed directly at the center tap of the two VCO inductors. In the P-QVCO, the switching transistor and coupling transistor are connected in parallel and thus the parasitic capacitances at the tank become larger and the LO swing decreases. In the S-QVCO topology, the switching transistor is cascoded with the coupling transistor. It has been known that the cascode-like connection of two transistors increases the output impedance.

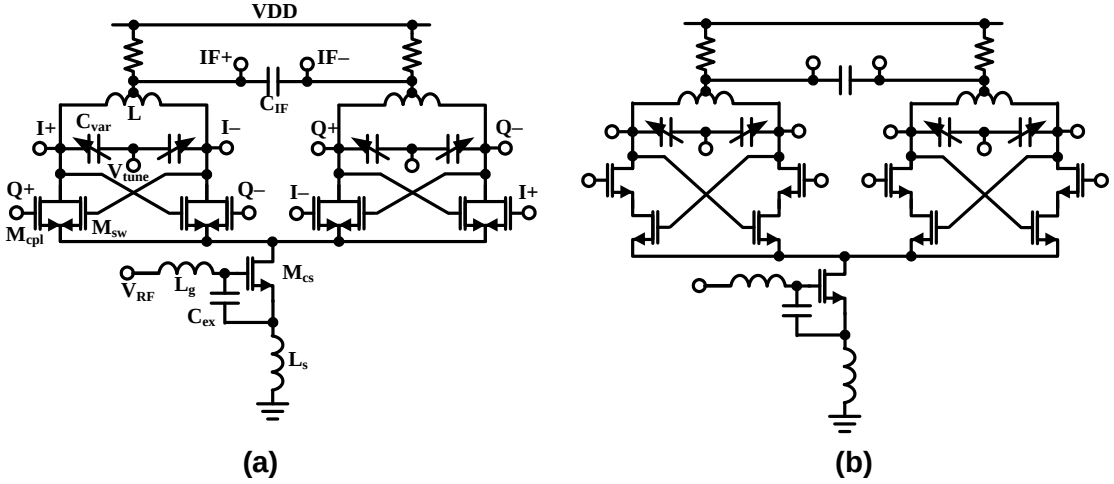


Figure 4. Proposed SH LMVs (a) P-QVCO SH LMV and (b) S-QVCO SH LMV.

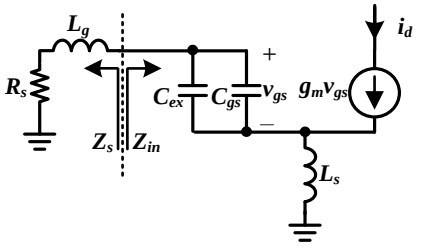


Figure 5. Small-signal equivalent circuit of the RF input transistor.

Figure 5 shows the small-signal equivalent circuit of the LNA where g_m is the transconductance of the transistor M_{cs}, v_{gs} is the small-signal gate-source voltage, and C_{gs} is the internal parasitic capacitance between the gate and source terminals. Z_s and Z_{in} are the impedances looking at the signal source and the LNA input, respectively. The external component sizes of C_{ex}, L_g and L_s are chosen following the power constrained simultaneous noise and input matching (PCSNIM) technique to match the signal source impedance (R_s) of 50 ohm [10-12].

To implement the SH LMVs, a symmetric inductor is used to have a higher quality (Q) factor to have a better phase noise performance. The tuning range is varied with the MOS varactors. The transistors M_{cpl} and M_{sw} in Figure 4 are set to have the same size for fair comparison of the two SH LMVs. The width of the switching and coupling transistors is 16 μm with the minimum channel length of 60 nm. The value of C_{ex} is about 120 fF.

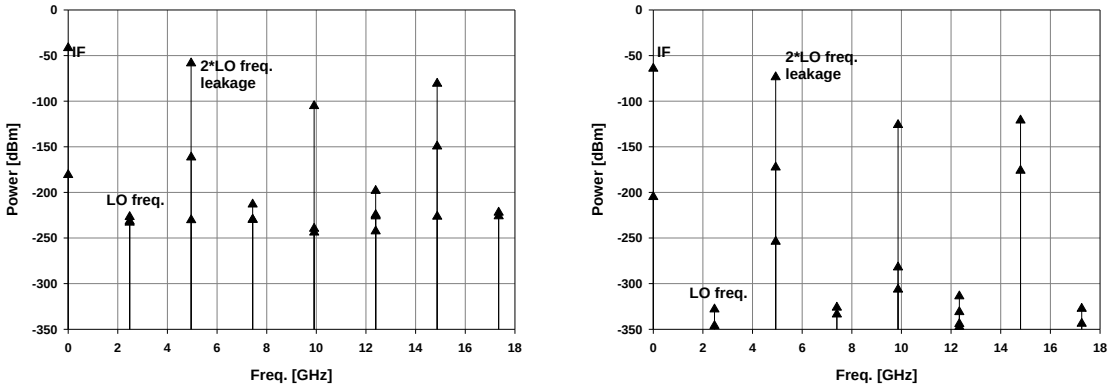


Figure 6. IF output spectrum (a) S-QVCO SH LMV and (b) P-QVCO SH LMV with RF input power of −60 dBm.

Simulations of the proposed LMVs are performed using the harmonic balanced simulation tool, Advanced Design System (ADS). For the simulations, the LO frequency is set to oscillate at around the 2.4 GHz. The applied RF frequency is two times of the f_{LO} which is targeted for 5 GHz WLAN application. All the components used for the simulations are based on the real RF models provided by the foundry process design kit (PDK) to reflect the exact RF characteristics. Figure 6 shows the simulated IF output spectrum for the two SH LMVs with the same dc power consumption. It can be seen that the LO signal is suppressed for the two SH LMVs. However, the two times of f_{LO} is still present at the IF output since the SHMs are single-balanced. This doubled LO frequency can be easily suppressed with small value capacitor at the IF output compared to the fundamental LO mixers. Figure 7 shows the signal swing at the RF input and the IF output when –60 dBm RF input signal is applied. The signal swing of the S-QVCO SH LMV is quite large compared to that of the P-QVCO SH LMV.

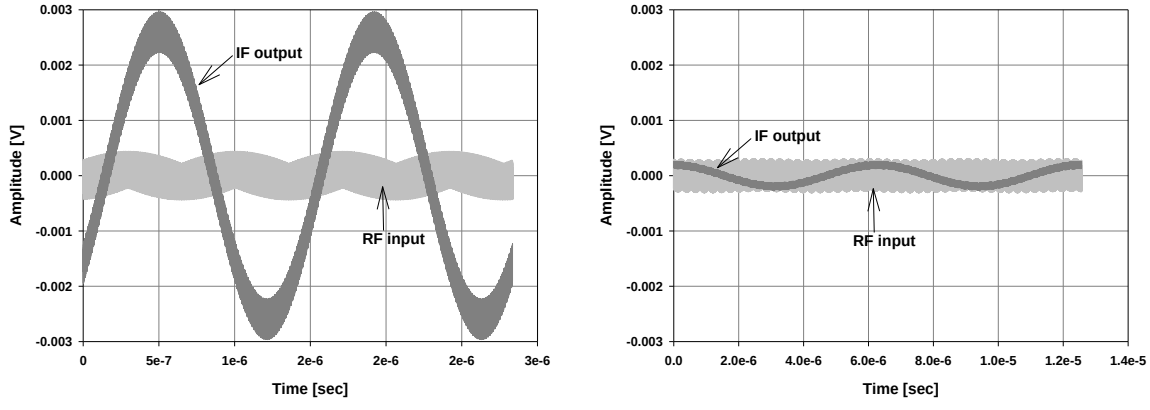
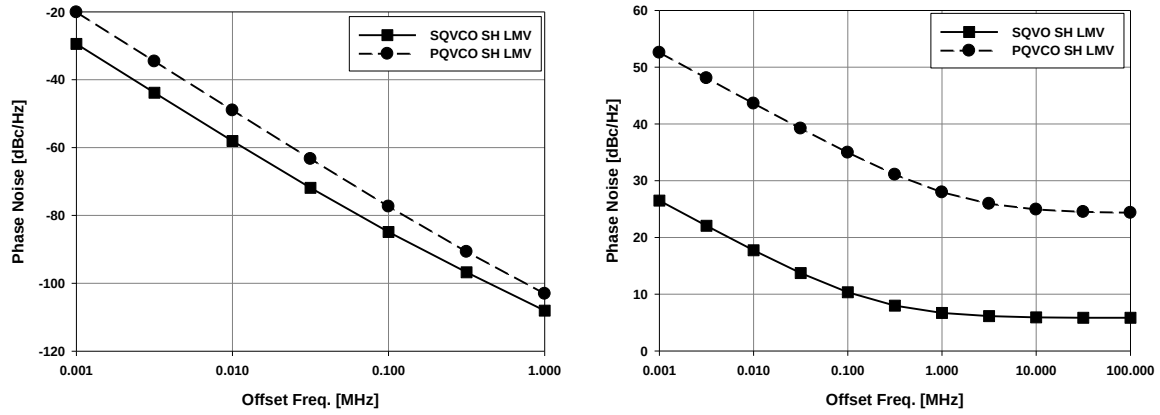


Figure 7. RF input and IF output swing (a) S-QVCO SH LMV and (b) P-QVCO SH LMV with RF input power of −60 dBm.

The reason is that the switching transistors and quadrature coupling transistors for the S-QVCO SH LMV are cascode-like connected and resulted in the higher impedance at the VCO output nodes. For the P-QVCO SH LMV, the switching transistors and quadrature coupling transistors are connected in parallel and more parasitic capacitances contribute significantly to the low output swing. Also, the parallel transistors contribute larger phase noise to the output. The S-QVCO SH LMV displays an excellent phase noise performance. The

voltage conversion gains of S-QVCO SH LMV and P-QVCO SH LMV are about 18 dB and –4dB, respectively.



(a) **(b)**

Figure 8. SH LMV performances (a) phase noise and (b) DSB NF.

Figure 8(a) shows the phase noise performance of the proposed S-QVCO SH LMV and P-QVCO SH LMV. The S-QVCO SH LMV has better phase noise performance compared to P-QVCO SH LMV. The S-QVCO SH LMV has the phase noise of –58 dBc/Hz, –85 dBc/Hz, and –108 dBc/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. The P-QVCO SH LMV has the phase noise of –49 dBc/Hz, –77 dBc/Hz, and –103 dBc/Hz at 10 kHz, 100 kHz, and 1 MHz offset frequency, respectively. As shown in Figure 8(b), the double-sideband (DSB) NF of S-QVCO SH LMV and P-QVCO SH LMV is 6.7 dB and 28 dB, respectively. The dc power consumption of the two SH LMVs is about 330 μW from a 1-V supply voltage.

Table I summarizes the performance of the proposed SHMs. From the simulation results, the proposed SHMs are expected to be successfully integrated for the direct conversion receiver such as smartphone, WLAN, Global Positioning System (GPS), satellite communication receiver, medical body area network, and cable TV (CATV) set-top box while consuming low power with just one integrated block.

Table 1. Performance summary of S-QVCO and P-QVCO SH LMVs

	S-QVCO SH LMV	P-QVCO SH LMV
Oscillation frequency(GHz)	2.48	2.46
DC power consumption(μW)	328	326
Voltage conversion gain(dB)	18	–4
Phase noise@1MHz(dBc/Hz)	–108	–103
DSB NF@1MHz(dB)	6.7	28

4. Conclusion

This paper proposes fully integrated subharmonic radio frequency front-end called LMV by stacking the QVCO on top of the LNA. In the proposed subharmonic LMV, the QVCO itself operates as a subharmonic mixer. Since the QVCO itself plays the role of the single-balanced subharmonic mixer, the proposed topology can remove the RF mixer component in the RF front-end and thus reduce the chip size. Also, the power consumption can be reduced with the dc current reuse technique by stacking. Another advantage of the proposed topologies is that many challenges of the direct conversion receiver can be evaded by exploiting the subharmonic mixing in the QVCO itself instead of the fundamental mixing. The IF signal can be directly extracted from the center taps of the QVCO tank inductors.

The proposed LMVs are designed and simulated using 65 nm CMOS technology. From the simulation results, the proposed LMVs are expected to be successfully integrated for the direct conversion wireless system such as smart phone, WLAN, Global Positioning System (GPS), satellite communication receiver, medical body area network, and cable TV (CATV) set-top box while consuming low power with just one integrated block.

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