Journal of Convergence for Information Technology
Vol. 11. No. 7, pp. 104-110, 2021
e-ISSN 2586-4440
DOI : https://doi.org/10.22156/CS4SMB.2021.11.07.104

Reduction of Source/Drain Series Resistance in Fin Channel MOSFETs Using Selective Oxidation Technique

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선택적 산화 방식을 이용한 핀 채널 MOSFET의 소스/드레인 저항 감소 기법

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Abstract A novel selective oxidation process has been developed for low source/drain (S/D) series resistance of the fin channel metal oxide semiconductor field effect transistor (MOSFET). Using this technique, the selective oxidation fin-channel MOSFET (SoxFET) has the gate-all-around structure and gradually enhanced S/D extension regions. The SoxFET demonstrated over 70% reduction in S/D series resistance compared to the control device. Moreover, it was found that the SoxFET behaved better in performance, not only a higher drive current but also higher transconductances with suppressing subthreshold swing and drain induced barrier lowering (DIBL) characteristics, than the control device. The saturation current, threshold voltage, peak linear transconductance, peak saturation transconductance, subthreshold swing, and DIBL for the fabricated SoxFET are 305 μA/μm, 0.33 V, 13.5 μS, 76.4 μS, 78 mV/dec, and 62 mV/V, respectively.

Key Words : Selective oxidation MOSFET, Fin channel MOSFET, Selective oxidation, Series resistance, Short channel effect

요 약 본 핀 채널 전계 효과 트랜지스터에서 낮은 소스/드레인 직렬 저항을 위한 새로운 선택적 산화 방식을 제안하였다. 이 방법을 이용하면, gate-all-around 구조와 점진적으로 증가되는 형태의 소스/드레인 확장영역을 갖는 핀 채널 MOSFET를 얻을 수 있다. 제안된 트랜지스터는 비교 소자에 비해 70% 이상의 소스/드레인 직렬 저항의 감소를 얻을 수 있다. 또한, 제안된 소자는 단채널 효과를 억제하면서도 높은 구동 전류와 전달컨덕턴스 특징을 보인다. 제작된 소자의 포화전류, 최대 선형 전달컨덕턴스, 최대 포화 전달컨덕턴스, subthreshold swing, 및 DIBL은 각각 305 μA/μm, 0.33 V, 13.5 μS, 76.4 μS, 78 mV/dec, 62 mV/V의 값을 갖는다.

주제어 : 선택적 산화 전계효과 트랜지스터, Fin 채널 전계효과 트랜지스터, 선택적 산화, 직렬저항, 단채널효과

1. Introduction

The multiple gate metal-oxide-semiconductor field effect transistors (MOSFETs) have been recognized as prime candidates for extending MOSFETs to the extreme channel length [1-3]. In these transistors, short channel effects are suppressed very effectively due to the excellent gate control over the body potential. F urthermore, high drive currents per unit area

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Received May 24, 2021
Revised June 18, 2021
Accepted July 20, 2021
Published July 28, 2021

are achieved due to the multiple gate action. From several multiple gate structures, the fin-channel MOSFETs have showed as a promising device structure due to its simple process compatible with the conventional complementary MOSFET process [5], [6]. The fin-channel MOSFET is comprised of a vertical fin-channel surrounded by gate electrodes which provides enhanced gate control. The fin-channel MOSFET has advantages over the conventional planar MOSFET, but several issues must be resolved.

One of the primary challenges in implementing fin-channel MOSFET is achieving controllable and small dimensions for the fin width to suppress adverse effects on device characteristics. Ashing/trimming technology [7], spacer lithography technology [8], and e-beam lithography technology [9] have produced, but the serious plasma damage is introduced on the sidewall of the fin during reactive ion etching process. The other problem is enabling high drive current by reducing the source/drain series resistance (R_{SD}). Because the device operation in fin-channel MOSFETs relies on the use of narrow fins, drive currents can be significantly reduced if there are no special provisions to minimize R_{SD}. Selective epitaxial re-growth process by thickening the fin outside of the gate region was proposed in [10] and [12], but these require well-formed spacers which separate the fin from the gate.

In this paper, we present a fabrication process of the selective oxidation fin-channel MOSFET (SoxFET) to yield a reduced S/D resistances and narrow fin structure using the selective oxidation. This article is extended version from the letter presented at [13]. The proposed process is much simpler and more robust than the conventional selective epitaxial re-growth process [10], [12]. Compared to the control device, the improvement in electrical characteristics with controlled short channel effects of the proposed device is demonstrated.

2. Device Fabrication

In the fabrication of the SoxFET, it is important to achieve controllable and small dimensions for the fin width because it governs off-state leakage currents and alleviates short channel effects. The critical process steps for the SoxFET are explained as follows.

The fabrication process of the SoxFET is schematically illustrated in Fig. 1. The starting material was (100), $1x10^{16}cm^{-3}$ boron doped SOI wafers with 150 nm Si on top of 150 nm buried oxide. A lightly doped substrate was used to minimize the change in threshold voltage due to statistical doping variation and to achieve high carrier mobilities for enahanced transistor drain current. A photoresist was coated and i-line photo lithography steps were performed to define the active region. The active region was etched with a depth and width of 150 and 400 nm, respectively. The width of 400 nm active region was reduced to 150 nm by photoresist ashing and dry etching (Fig. 1(a)). The above photoresist ashing and dry etching steps are not required if nano-scale design rules lithography becomes possible. These processes were performed only for nano-scale fin channel demonstration with the conventional lithography technology. The remaining 150 nm width silicon pattern in Fig. 1 (a) serves as a base material to oxidation during the subsequent thermal oxidation.

The thermal oxide with a thickness of 10 nm was grown and the SiN layer with a thickness of

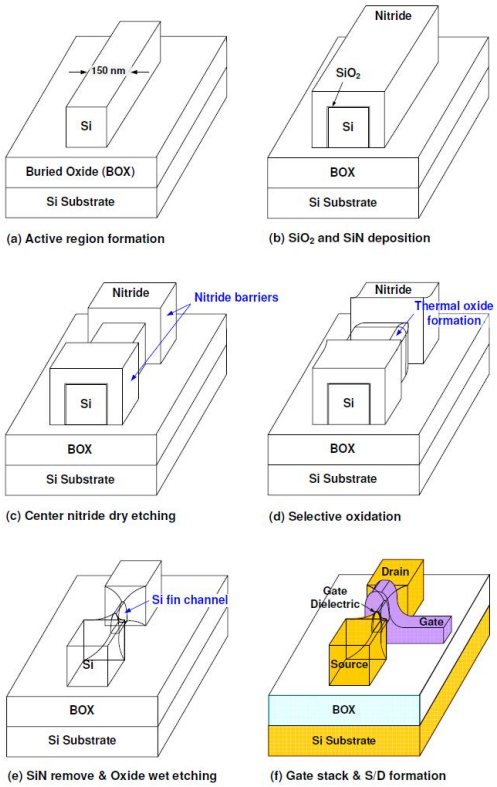


Fig. 1. Process flow for the SoxFET. The channel structure of the SoxFET which has the three-dimensional bird's beak prole shows in (e) after the thermal oxide layer removing by wet etching.

200 nm was deposited. The SiN was completely removed from the center of the active channel region using anisotropic dry etching (Fig. 1(c)). These nitride barriers were not subjected to the control device. Next, the thermal oxide was grown for 40 min at 950 °C to make a thin width fin-channel. Unlike the oxide layer, the SiN layer does not allow oxygen to pass through. Therefore, a thermal oxide layer was grown at only a portion where the gap was formed, i.e., the portion of the channel region and the S/D extension regions (Fig. 1(d)). After SiN oxidation barriers were removed, the oxide layer was also eliminated by wet etching. The three-dimensional bird's beak shape of the fin channel is shown in Fig. 1(e). Due to the

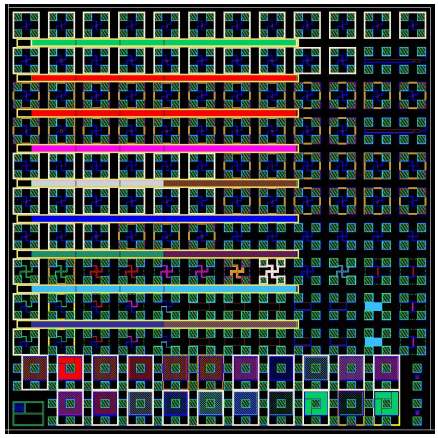
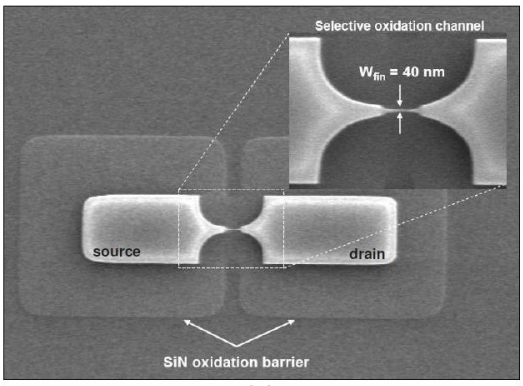
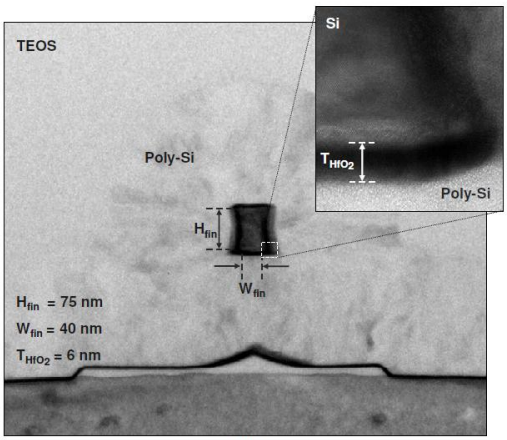


Fig. 2. Mask patterns for device fabrication. It includes proposed SoxFETs, conventional FinFETs, and various capacitances.

selective oxidation, it can implement the raised S/D structure without epitaxial layer growth which has gradually increased extension regions from the active channel toward S/D areas. These thickened S/D regions help to decrease overall parasitic series resistance. In addition, surface treatments of the fin such as the hydrogen annealing [14] and sacrificial oxidation [15] are not needed to remove plasma damage since the fin was formed by thermal oxidation with wet etching. HfO_2 gate dielectrics with a target 60 angstrom were deposited by atomic layer deposition. Then the gate electrode with a thickness of 250 nm was patterned using i-line lithography. The S/D was formed by ion implantation of arsenic with a dose of $60x10^{15}$ cm^{-2} and an energy of 60 keV. Following the implantation, low temperature oxide was deposited and S/D activation was performed by rapid thermal anneal at 950 °C. Finally, contacts and electrodes were formed using conventional semiconductor process techniques. Fig. 2 shows a mask pattern for device fabrication. It includes hundreds of devices and test patterns for proposed and control devices. The samples were measured on-wafer using HP4156A semiconductor parameter analyzer for DC measurement.



(a)



(b)

Fig. 3. Electron micrographs of the fabricated SoxFET. (a) Top down SEM image of the active region in Fig. 1(e), (b) Cross-sectional TEM image of the n structure in Fig. 1(f). The gradullay increased extension regions from the channel toward S/D regions were formed and the channel region was wrapped around the gate oxide and gate electrodes.

3. Results and Discussions

A top down scanning electron microscope (SEM) image of the active region taken after the center oxidation layer removing in Fig. 1(e) and a cross-sectional transmitter electron microscopy (TEM) image of the fin channel across the gate taken after gate stack formation in Fig. 1(f) are shown in Fig. 3(a) and (b), respectively.

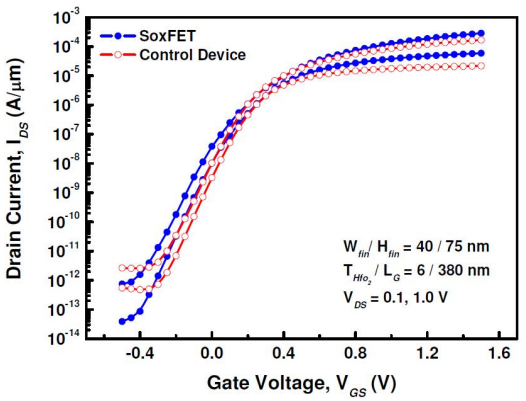


Fig. 4. Subthreshold characteristics of the SoxFET and control device at V_{DS} = 0.1 V and 1.0 V. The SoxFET has the short channel immunity which is similar to the control device and it has more excellent DC performances.

Because of the three-dimensional selective oxidation with wet etching process, gradually increased extension regions from the channel toward S/D regions were implemented which are advantageous to decrease parasitic series resistance and the channel region was wrapped around the gate higk-k oxide and poly-Si gate electrodes which is helpful to suppress short channel effects. It should be noted that the SoxFET shows the gate-all-around structure which providing the best possible electrostatic control. The gate-all-around SoxFET can lead to the increase of the aspect ratio of the gate. The width and height of the fin channel are 40 nm and 75 nm, respectively. An extremely small fin width pass over the lithographic limit was achieved from the selective oxidation technique.

The drain current (I_{DS}) versus gate voltage (V_{GS}) characteristics of the proposed SoxFET and control device with 380 nm gate length (L_G) and 40 nm fin width are shown in Fig. 4. The current was normalized by two times of the fin height (H_{fin}) plus two times of the fin width (W_{fin}) due to the gate-all-around structure of the SoxFET.

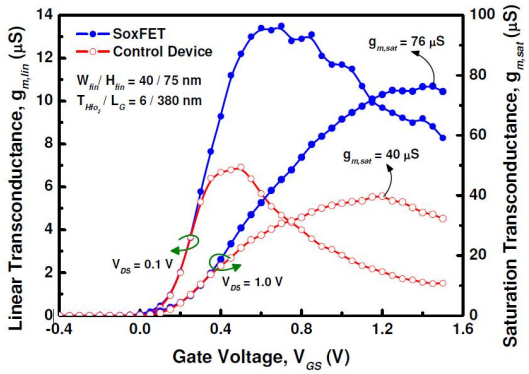


Fig. 5. Transconductance characteristics of the two devices at the linear and saturation regime. The gm peak of the SoxFET is 1.96 and 1.92 times larger than that of control device at the linear and saturation region, respectively.

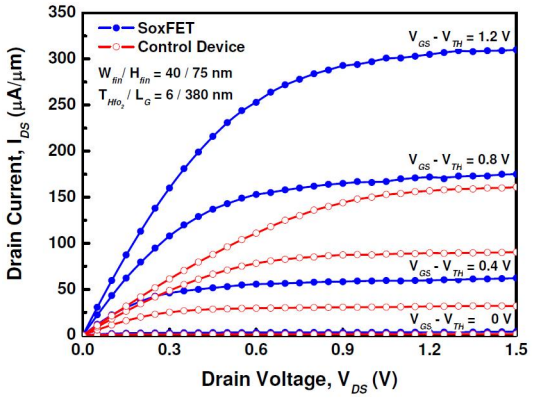


Fig. 6. I_{DS}–V_{DS} characteristics of the SoxFET and control device at various gate overdrives. The series resistance reduction in the SoxFET results in a 94 % improvement in the drain current at V_{DS} = 1.2 V and V_{GS}–V_{TH} = 1.2 V.

The SoxFET shows almost twice higher drive current, indicating a series resistance reduction as a result of the selective oxidation. The subthreshold slope of 78 mV/dec and DIBL of 62 mV/V was obtained with the SoxFET whereas that of the control device shows the subthreshold slope of 77mV/dec and DIBL of 43 mV/V at the same gate length. The subthreshold slope was evaluated from the maximum slope in the I_{DS} versus V_{GS} characteristics at V_{DS} = 1.0 V and DIBL was evaluated as the gate voltage shift between V_{DS} = 0.1 V and V_{DS} = 1.0 V curves at I_{DS} = 1 nA. It is noted that the SoxFET has the short channel immunity which is similar to the control device and it has more excellent DC performances. The threshold voltages (V_{TH}) of the SoxFET and control device which are extracted by the linear extrapolation method showed 0.33 V and 0.24 V, respectively. The SoxFET exhibits about 0.1 V higher V_{TH}. This could be contributed by the reduction of the charge sharing of the channel due to the raised S/D structure of the SoxFET. For the planar structure, the channel potential is strongly disturbed by the drain voltage and the potential barrier is removed in the channel region.

In contrast to the raised S/D structure for which the potential barrier is only slightly influenced by the drain region. Thus, the effects of the raised S/D structure of the proposed SoxFET which diminishes the charge sharing of the channel increase the V_{TH} [16,17].

The linear transconductance ($g_{m,lin}$) and saturation transconductance ($g_{m,sat}$) of the SoxFET are compared in Fig. 6 with that of the control device. The peak $g_{m,lin}$ for the SoxFET is 13.5 μS, while it is 6.9 μS for the control device. In the saturation region, there is a 92 % peak transconductance improvement for the SoxFET compared with the control device. A key to achieved high transconductance values is the low series resistance. The impact of the S/D series resistance is larger for the control device, so the transconductance enhancement could be substantially lower. As the gate bias increases, the control device shows a signicantly degradation in $g_{m,lin}$, which is also due to the higher S/D series resistance of the S/D extension regions.

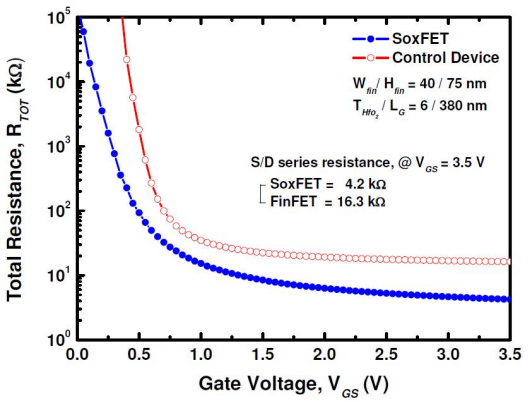


Fig. 7. Extracted total resistances as a function of gate voltage. The SoxFET demonstrated a 74 % reduction in S/D series resistance compared with that of the control device.

In Fig. 6, the drain current (I_{DS}) versus drain voltage (V_{DS}) characteristics of the SoxFET and control device are showed for gate overdrives (V_{GS} -V_{TH}) of 0, 0.4, 0.8, and 1.2 V. The SoxFET has 1.94 times larger drive current of 305 μA/μm at V_{GS} -V_{TH} = 1.2 V and V_{DS} = 1.2 V than the control device, which shows 157 μA/μm. The drain current enhancement in the SoxFET comes primarily from the reduced S/D series resistance. In other words, the current drivability is mainly affected by the parasitic series resistance introduced at S/D extension regions. More significant performance enhancement can be expected by improving further process tuning and device optimization.

The drive current and transconductances improvement should be attributed to the reduction in the parasitic S/D resistance. Therefore, we extracted the total parasitic resistance at the S/D regions and the channel regions by use of following method. The total resistance of a MOSFET is given as [18]

$$R_{TOT} = \frac{V_{ds}}{I_s} = R_{CH} + R_{SD} \quad (1)$$

Table 1. Summarized electrical characteristics of the SoxFET and control device.

	SoxFET	Control Device
$I_{DS,sat}$ (μA)	305	157
peak $g_{m,sat}$(μS)	76.4	39.8
R_{SD}(kΩ)	4.23	16.3
V_{th}(V)	0.33	0.24
SS(mV/dec)	78	77
DIBL(mV/V)	62	43

where R_{TOT} is the total resistance, R_{CH} is the channel resistance and R_{SD} is the S/D series resistance. At low V_{DS} and infinitely large V_{GS}, R_{CH} gradually diminishes and R_{TOT} becomes equal to R_{SD}. The R_{TOT} has been calculated as a function of V_{GS} for the I_{DS} versus V_{GS} curves and is plotted in Fig. 7. It can be seen from Fig. 7 that for high V_{GS} values, R_{TOT} becomes constant, and is taken as R_{SD}. The S/D series resistance is signicantly improved for the SoxFET (4.23 kΩ), compared to the conventional FinFET (16.3 kΩ). By gradually increased S/D extension region structure of the proposed SoxFET, the S/D series resistance can be reduced resulting in improved transconductance and drive current. In Table I, the electrical characteristics of the two devices are summarized.

4. Conclusion

The selective oxidation fin channel MOSFET which has the gate-all-around structure and gradually increased S/D extension regions are fabricated. In our investigation of DC characteristics of the proposed device, the proposed SoxFET revealed larger saturation current and transconductances. The proposed device geometry can responsible for the improved on series resistance while maintaining the short channel behaviors.

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