JKIICE

Short Paper

한국정보통신학회논문지 Vol. 25 No. 6: 853~856, Jun. 2021

다양한 매칭 회로들을 활용한 저잡음 증폭기 설계 연구

Design of Low Noise Amplifier Utilizing Input and Inter Stage Matching Circuits

Sung-Hun Jo*

*Assistant professor, Department of Electronic Engineering, Dongseo University, Busan, 47011 South Korea

ABSTRACT

In this paper, a low noise amplifier having high gain and low noise by using input and inter stage matching circuits has been designed. A current-reused two-stage common-source topology is adopted, which can obtain high gain and low power consumption. Deterioration of noise characteristics according to the source inductive degeneration matching is compensated by adopting additional matching circuits. Moreover trade-offs among noise, gain, linearity, impedance matching, and power dissipation have been considered. In this design, 0.18-mm CMOS process is employed for the simulation. The simulated results show that the designed low noise amplifier can provide high power gain and low noise characteristics.

Keywords : Low noise amplifier, Matching circuit, Maximum gain, Minimum noise figure

Ⅰ. Introduction

Low noise amplifier (LNA) is a key building block in modern electrical system. LNA amplifies a very weak signal at the front end of the wireless receiver. The first stage in wireless receiver has the most significant effect on the noise performance of the entire system because the effect of noise from subsequent stages are reduced by stage gains [1], [2]. Thus, the LNA locating at the first stage in wireless receiver is required to have minimum noise figure and maximum gain. Moreover, in designing the LNA, trade-offs among noise, gain, linearity, impedance matching, and power consumption should be considered [3], [4]. In particular, the main process of LNA design is to simultaneously perform input matching and noise matching under a given amount of power consumption. In this paper, a current-reused two-stage common-source LNA topology utilizing input stage, inter stage, and output stage matching circuits is designed, which can obtain high gain and low noise characteristics.

Ⅱ. Designed System Architecture

A simplified schematic of the cascode LNA topology is shown in Fig. 1 [5]. The miller effect can be eliminated in cascode structure, which improves isolation between input and output matching circuits [6]. That is, inverse leakage signal can be effectively suppressed. In addition, in order to reduce power consumption in the cascode structure, the size of the transistor M1 should be sufficiently small. That is, the gate-source capacitance (C_{gs}) of transistor M1 should be small, which requires a large value of L_S. However, when the value of L_S is increased, minimum achieveble noise figure(NF) increases, which causes deterioration of noise characteristics. By adding C_{ex}, deterioration of noise characteristics can be prevented without increasing the size of the transistor M1. However, since the gain decreases as the value of C_{ex} increases, it is important to select C_{ex} and L_S with adequate values in consideration of performance trade-offs.

Received 27 April 2021, **Revised** 1 May 2021, **Accepted** 10 May 2021

*** Corresponding Author** Sung-Hun Jo(E-mail:sunghun@dongseo.ac.kr, Tel:+82-51-320-4226)
Assistant professor, Department of Electronic Engineering, Dongseo University, Busan, 47011 South Korea

Open Access http://doi.org/10.6109/jkiice.2021.25.6.853 print ISSN: 2234-4772 online ISSN: 2288-4165

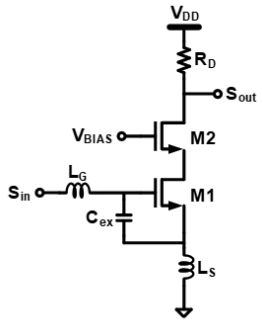

Fig. 1 Simplified schematic of the cascode LNA

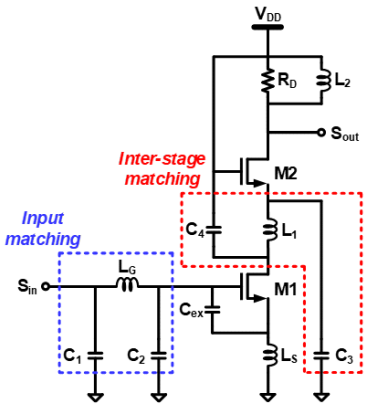

Fig. 2 Schematic of designed LNA

Moreover, adding C_{ex} leads to a decrease in power consumption, which can deteriorate linearity. In order to improve the linearity, the value of transconductance of transistor M1 must be increased, but this means an increase in power consumption. Therefore, it becomes difficult to overcome the trade-off between linearity and current consumption in a design where the amount of usable power is limited. Thus, in a design requiring low power consumption, the current-reused method can be effectively used [3], [7]. By combining cascode and current-reused method, low power consumption and high gain can be obtained.

Designed current-reused two-stage common-source LNA topology is shown in Fig. 2. The designed topology can achieve high gain characteristic through low power consumption, but it has a disadvantage of deteriorating the noise figure. Thus, to prevent deterioration of the noise figure, an input matching circuit is utilized.

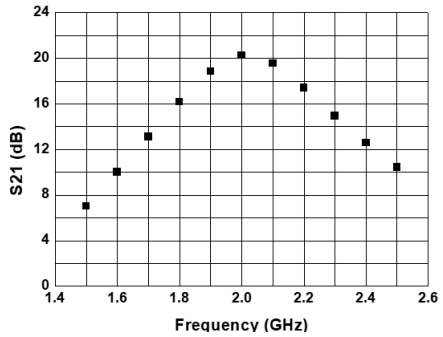

Fig. 3 Power gain of the designed LNA

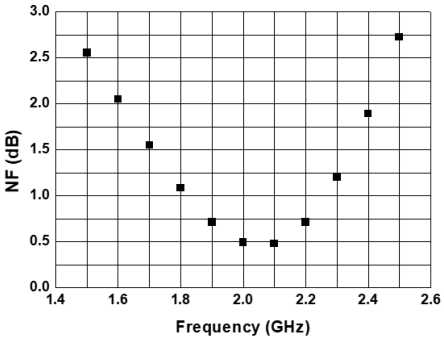

Fig. 4 Noise figure of the designed LNA

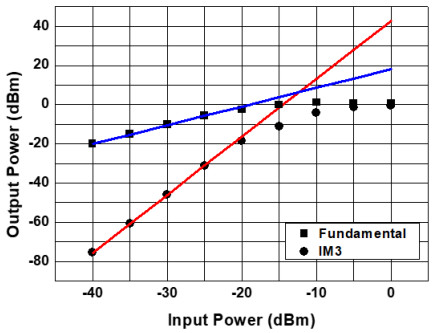

Fig. 5 IIP3 of the designed LNA

Table. 1 Design parameters

Parameter	Value
L_G	24 nH
C_1	320 fF
C_2	50 fF
C_{ex}	145 fF
L_S	0.5 nH
L_1	2 nH

Parameter	Value
L_2	10 nH
R_D	900 Ω
C_3	630 fF
C_4	500 fF
M1(W/L)	60 μm / 0.18 μm
M2(W/L)	60 μm / 0.18 μm

Table. 2 Performance summary

Parameter	Value
Target Frequency	2 GHz
NF	0.5 dB
S21	20.3 dB
S11	-17.4 dB
IIP3	-12.1 dBm
Power dissipation	5.3 mW
Supply voltage	1.8 V
CMOS Technology	0.18 μm

In the source inductive degeneration matching scheme, a relatively high bias current is required to achieve simultaneous power and noise matching. Therefore, if this scheme is used in a design that requires low power consumption, noise figure becomes worse. Thus, to prevent deterioration of the noise figure, an input matching scheme is also used. Previously, input matching was performed only through L_G, C_{ex}, and L_S. By adding C_1 and C_2, input matching can be performed effectively even when low power consumption is required. That is, value of L_S can be reduced to improve gain and noise figure while maintaining input matching through adjustment of L_G, C_1, and C_2 values.

Furthermore, the two transistors M1 and M2 share the same bias current to reduce power consumption. The amplified signal from the transistor M1 is applied to the gate of the transistor M2 through the coupling capacitor C_4, and the capacitor C_3 acts as a by-pass capacitor for the transistor M2. In the designed structure, L_G, C_1, C_2, C_{ex}, and L_S are adopted for simultaneous power and noise matching. In addition, L_2 and R_D were used for output matching, and an LC network (L_1-C_4) between the gain stages was used for inter stage matching.

In order to obtain the minimum noise figure and maximum gain, the value of V_{gs} of transistor M1 must be determined. After that, the size of the transistor M1 is determined in consideration of the available power budget. As the size of the transistor M1 becomes smaller, power consumption decreases, but the cut-off frequency also decreases, thus it is important to determine an appropriate size of transistor M1. In this design, when V_{gs} is equal to about 600 mV, it shows the maximum gain and minimum noise characteristics.

Fig. 3 shows power gain (S21) of about 21.3 dB at 2 GHz. Noise figure (NF) of the designed LNA is shown in Fig. 4. It represents a value of about 0.5 dB at 2 GHz. Third order input intercept point (IIP3) is shown in Fig. 5. The extrapolated lines intersect on about －12.1 dBm. Moreover, design parameters are shown in the Table 1. Various components including capacitors, inductors, and resistors are adopted to implemented the designed structure. Performance of designed LNA is summarized in the Table 2. It has been designed to target of the 2 GHz and implemented using 0.18-μm CMOS process.

Ⅲ. Conclusion

In this paper, LNA utilizing various matching circuits is designed. current-reused two-stage common-source topology is adopted, which can obtain a high gain through low power consumption. Deterioration of noise figure according to current-reused two-stage common-source topology and inductive source degeneration matching is compensated by utilizing additional matching circuits.

ACKNOWLEDGEMENT

This work was supported by the Dongseo University Research Fund of 2020. (DSU-20200028)

REFERENCES

[1] H. Rashtian and S. Mirabbasi, "Applications of Body Biasing in Multistage CMOS Low-Noise Amplifiers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 6, pp. 1638-1647, Jun. 2014.

[2] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A Millimeter-Wave (23-32 GHz) Wideband BiCMOS Low-Noise Amplifier," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 289-299, Feb. 2010.

[3] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An Ultra-Low-Power Wideband Inductorless CMOS LNA With Tunable Active Shunt-Feedback," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 6, pp. 1843-1853, Jun. 2016.

[4] J. Hu, K. Ma, S. Mou, and F. Meng, "A Seven-Octave Broadband LNA MMIC Using Bandwidth Extension Techniques and Improved Active Load," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3150-3161, Oct. 2018.

[5] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifiers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 11, pp. 1388-1396, Nov. 1999.

[6] P. Wei, M. Tsai, S. Hsu, C. Shen, and T. Wu, "An Electromagnetic Bandgap Structure Integrated With RF LNA Using Integrated Fan-Out Wafer-Level Package for Gigahertz Noise Suppression," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 12, pp. 5482-5490, Dec. 2018.

[7] P. Qin and Q. Xue, "Design of Wideband LNA Employing Cascaded Complimentary Common Gate and Common Source Stages," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 6, pp. 587-589, Jun. 2017.