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다양한 증분형 아날로그 디지털 변환기의 설계 방정식 유도

정영호*

Derivation of design equations for various incremental delta sigma analog to digital converters

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요 약

증분형 아날로그 디지털 변환기는 전통적인 델타 시그마 아날로그 디지털 컨버터와 달리 리셋 동작을 통한 입력과 출력의 1:1 매핑이 가능하며 이는 멀티플렉싱에 매우 용이하게 사용될 수 있다. 또한, 증분형 아날로그 디지털 변화기는 전통적인 델타 시그마 변환기에 비해 간단한 디지털 필터 설계가 가능하다. 따라서, 본 논문에서는 아날로그 디지털 컨버터 설계에 기본이 되는 딜레이가 있는 적분기와 딜레이가 없는 적분기의 시간 영역에서의 분석을 시작으로 2차 입력 피드 포워드, 확장된 카운팅, 2+1 매쉬, 2+2 매쉬 구조를 갖는 증분형 아날로그 디지털 변환기의 설계 방정식을 유도한다. 이를 통해 설계 이전에 증분형 아날로그 디지털 변환기의 성능을 예측할 수 있을 뿐만 아니라 각각의 아날로그 디지털 변화기에 적합한 디지털 필터를 설계할 수 있다. 또한, 아날로그 디지털 변환기의 정확도를 향상시키기 위한 확장된 카운팅, MASH의 설계 기술들을 제안하였다.

ABSTRACT

Unlike traditional delta-sigma analog-to-digital converters, incremental analog-to-digital converters enable 1:1 mapping of input and output through a reset operation, which can be used very easily for multiplexing. Incremental analog-to-digital converters also allow for simpler digital filter designs compared to traditional delta-sigma converters. Therefore, starting with analysis in the time domain of the delayed integrator and non-delayed integrator, which are the basic blocks of analog-to-digital converter design, the design equations of a second-order input feed-forward, extended counting, 2+1 MASH (Multi-stAge-noise-SHaping), 2+2 MASH incremental analog-to-digital converter are derived in this paper. This allows not only prediction of the performance of the incremental analog-to-digital converter before design, but also the design of a digital filter suitable for each analog-to-digital converter. In addition, extended counting and MASH design techniques were proposed to improve the accuracy of analog-to-digital converters.

키워드 : 멀티플렉싱, 적분기, 증분형 아날로그 디지털 변환기, 디지털 필터

Keywords : Multiplexing, Integrator, Incremental ADC, Digital filter

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Ⅰ. Introduction

Analog-to-digital converters (ADCs) are crucial components for most electronic systems to connect between analog and digital worlds. Also, an ADC can be a very accurate timing reference in some sensing topologies [1]. Among the various types of ADCs, ΔΣ ADCs have been widely used for high resolution with the aid of oversampling and noise shaping technique. There is growing interest in biosensors and Internet of Things (IoT) systems, which require integrated sensor systems with low power consumption and high accuracy. In some applications, such as ECG/EEG systems and image sensors, a single ADC should be multiplexed among many channels. Therefore, incremental ADCs are one of the best candidates to achieve high power efficiency and more than 16-bit resolution within a narrow band signal (<1 kHz) [2]. Moreover, they can be multiplexed easily and require a very simple digital filter.

Incremental ADCs have most of the advantages of a Δ Σ modulator, such as low power consumption and high resolution [3]. Also, they can easily be reconfigurable to provide operational flexibility [4]. Their operation is also quite similar to that of a ΔΣ modulator except for resetting periodically. In this study, simple design equations in the time domain were derived for various incremental ADCs to predict their resolution and to design the correct digital filter.

Ⅱ. Incremental ΔΣ ADCs

Prior to deriving the design equation, the time-domain characteristics of delayed and non-delayed integrators that are commonly used in incremental ΔΣ ADCs need to be investigated. Fig. 1 shows a delayed integrator and its equivalent model. The input signal (x) passes through the delay block, and the output signal (y) is fed back to the input. Table 1 shows the generalized time domain characteristics of a delayed integrator according to the time index. Based on the characteristics, the integrator output after M clock cycles can easily be obtained.

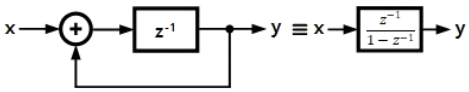

Fig. 1 A delayed integrator and its equivalent model

Table. 1 Time domain characteristics of a delayed integrator

Time index	$x(i)$	$y(i)$
1	$x(1)$	$y(0)$
2	$x(2)$	$y(0)+x(1)$
3	$x(3)$	$y(0)+x(1)+x(2)$
. .	. .	. .
M	$x(M)$	$y(0)+x(1)+x(2)+\cdots+x(M-1)$ $\therefore y[M]=\sum_{i=1}^{M-1}x(i)$

Similarly, Fig. 2 shows a non-delayed integrator and its equivalent model. In the same way, the integrator output after M clock cycles can be calculated as shown in Table 2.

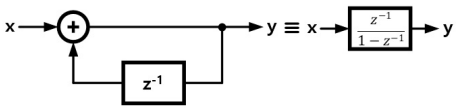

Fig. 2 A non-delayed integrator and its equivalent model

Table. 2 Time domain characteristic of a non-delayed integrator

Time index	$x(i)$	$y(i)$
1	$x(1)$	$x(1)$
2	$x(2)$	$x(1)+x(2)$
3	$x(3)$	$x(1)+x(2)+x(3)$
. .	. .	. .
M	$x(M)$	$x(1)+x(2)+x(3)+\cdots+x(M)$ $\therefore y[M]=\sum_{i=1}^{M}x(i)$

Incremental ΔΣ ADCs have been widely used for multiplexed sensor interfaces because of the periodic reset operation mapping between input and output

samples. Therefore, incremental ΔΣ ADCs can easily be analyzed in the time domain with the reset pulse. Fig. 3 shows the 1st-order incremental ΔΣ ADC and its timing diagram.

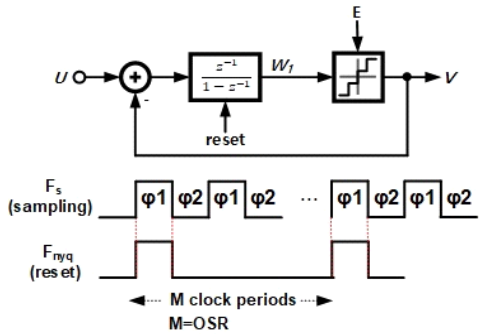

Fig. 3 1st-order incremental $\Delta\Sigma$ ADC and its timing diagram

In Fig.3 E represents the quantization noise of the quantizer and Φ1, Φ1 means sampling and integration phase respectively.

After M clock cycles,

$$W_1[M]=\sum_{i=1}^{M-1}U[i]-\sum_{i=1}^{M-1}V[i] \tag{1}$$

The modulator output V with a linearized quantizer model can be expressed as

$$W_1[M]+E[M]=V[M] \tag{2}$$

The substitution of $W_1[M]$ in Eq. (2) results in

$$\sum_{i=1}^{M-1}U[i]-\sum_{i=1}^{M-1}V[i]+E[M]=V[M] \tag{3}$$

$$\sum_{i=1}^{M-1}U[i]+E[M]=\sum_{i=1}^{M}V[i] \tag{4}$$

Assuming the input signal U is constant, the average of input U($\widetilde{U}$) can be defined as

$$\widetilde{U}=\frac{1}{M-1}\cdot\sum_{i=1}^{M-1}U[i] \tag{5}$$

Therefore, Eq. (4) can be rewritten as

$$\widetilde{U}\cdot(M-1)+E(M)=\sum_{i=1}^{M}V[i] \tag{6}$$

$$\therefore \widetilde{U}+\frac{E[M]}{M-1}=\frac{1}{M-1}\cdot\sum_{i=1}^{M}V[i] \tag{7}$$

With an N-bit internal quantizer, the quantization error E(M) relative to full scale (V_{FS}) is

$$E(M)=\frac{V_{FS}}{2^N} \tag{8}$$

Therefore, the signal to quantization noise ratio (SQNR) and effective number of bits (ENOB) can be calculated as

$$SQNR=20\cdot\log\left(\frac{V_{FS}}{E_{IDC}}\right)= 20\cdot\log\{2^N\cdot(M-1)\} \tag{9}$$

$$ENOB=\log_2\left(\frac{V_{FS}}{E_{IDC}}\right)=\log_2\{2^N\cdot(M-1)\} \tag{10}$$

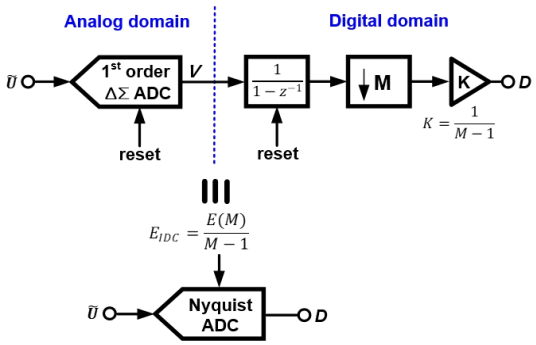

Fig. 4 1st-order incremental $\Delta\Sigma$ ADC with digital filter

Based on Eq. (7), the digital filter of the 1st-order incremental ΔΣ ADC can be implemented as shown in Fig. 4. The incremental ΔΣ ADC can be understood as a Nyquist rate ADC with EIDC, which is the equivalent quantization error of the incremental ΔΣ ADC. According to Eq. (10), 2^M clock cycles are needed to achieve M-bit accuracy in a 1st-order incremental ADC.

Ⅲ. Derivation of design equations for various types of incremental ΔΣ ADCs

1. Input feed-forward 2nd-order incremental ΔΣ ADC

Fig.5 shows the input feed-forward 2nd-order incremental ΔΣ ADC and its timing diagram.

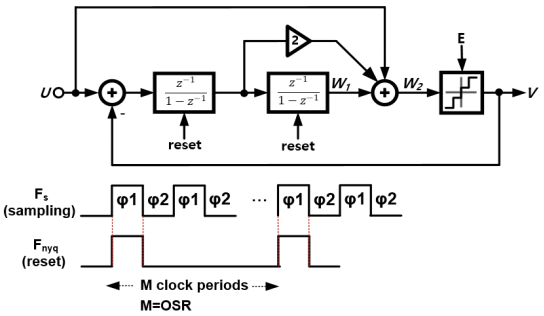

Fig. 5 Input feed-forward 2nd-order incremental $\Delta\Sigma$ ADC and its timing diagram

The design equations of the 2nd-order incremental ΔΣ ADC can be derived in the same way as before. At the end of M(=OSR) clock cycles, W_1 and W_2 are

$$W_1[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i] \tag{11}$$

$$W_2[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i]+ 2\sum_{i=1}^{M-1}U[i]-2\sum_{i=1}^{M-1}V[i]+U[M] \tag{12}$$

With a linearized quantizer model,

$$\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]+2\sum_{i=1}^{M-1}U[i]+U[M]+E[M]= \sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i]+2\sum_{i=1}^{M-1}V[i]+V[M] \tag{13}$$

With mathematical manipulation, Eq. (13) can be simplified as

$$\sum_{L=1}^{M}\sum_{i=1}^{L}U[i]+E[M]=\sum_{L=1}^{M}\sum_{i=1}^{L}V[i] \tag{14}$$

$$\widetilde{U}\cdot\frac{M\cdot(M+1)}{2}+E(M)=\sum_{L=1}^{M}\sum_{i=1}^{L}V[i] \tag{15}$$

Therefore, the design equation of the 2nd-order incremental ΔΣ ADC can be given as

$$\therefore \widetilde{U}+\frac{2}{M\cdot(M+1)}\cdot E[M]= \frac{2}{M\cdot(M+1)}\cdot\sum_{L=1}^{M}\sum_{i=1}^{L}V[i] \tag{16}$$

Based on Eq. (16), the digital filter of the 2nd-order incremental ΔΣ ADC can be implemented by two non-delayed integrators, as shown in Fig. 6.

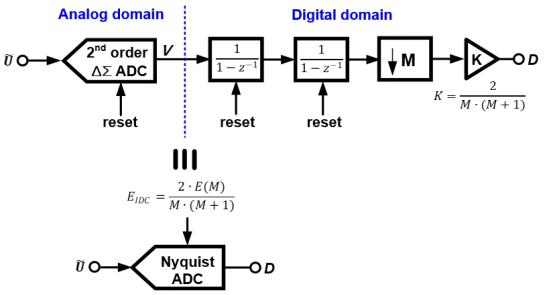

Fig. 6 Input feed-forward 2nd-order incremental $\Delta\Sigma$ ADC with a digital filter

2. Conventional 2nd-order incremental ΔΣ ADC

Fig. 7 shows the conventional 2nd-order incremental ΔΣ ADC and its timing diagram.

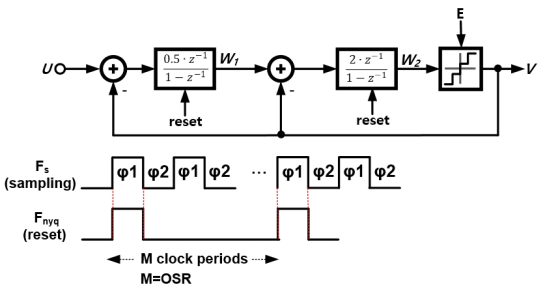

Fig. 7 Conventional 2nd-order incremental $\Delta\Sigma$ ADC and its timing diagram

After M clock cycles, W_1 and W_2 are

$$W_1[M]=\frac{1}{2}\sum_{i=1}^{M-1}(U[i]-V[i]) \tag{17}$$

$$W_2[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i]-2\sum_{i=1}^{M-1}V[M] \tag{18}$$

With a linear quantizer model, Eq. (18) can be rewritten as

$$\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} U[i]+E[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} V[i] \quad (19)$$
$$+2\sum_{i=1}^{M-1} V[M]+V[M]=\sum_{L=1}^{M}\sum_{i=1}^{L} V[i]$$

Consequently, the design equation of the conventional 2nd\-order incremental ΔΣ ADC can be given as

$$\widetilde{U}\cdot\frac{(M-1)\cdot(M-2)}{2}+E(M)=\sum_{L=1}^{M}\sum_{i=1}^{L} V[i] \quad (20)$$

$$\therefore \widetilde{U}+\frac{1}{(M-1)\cdot(M-2)}\cdot E[M]= \quad (21)$$
$$\frac{1}{(M-1)\cdot(M-2)}\cdot\sum_{L=1}^{M}\sum_{i=1}^{L} V[i]$$

According to Eq. (21), two non-delayed integrators consist of a digital filter of the conventional 2nd-order incremental ΔΣ ADC, as shown in Fig. 8.

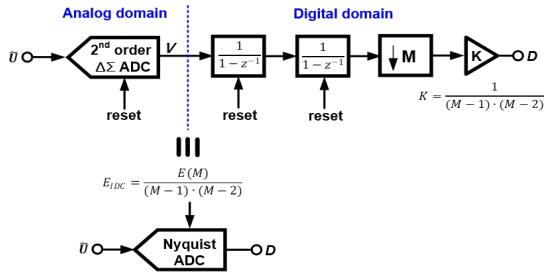

Fig. 8 Conventional 2nd-order incremental ΔΣ ADC with a digital filter

3. Incremental ΔΣ ADC with extended counting

The accuracy of the incremental ΔΣ ADC can be improved by increasing the modulator order or oversampling ratio. Increasing the modulator order can cause stability problems and more power dissipation. Also, a higher oversampling ratio results in higher power consumption to achieve the required settling error. An extended counting scheme was proposed and verified to resolve these issues [5-6]. In this scheme, a residue ADC operates at the conversion rate, not the oversampling rate. In other words, one-to-one mapping between the input and output can be maintained [7]. Fig. 9 shows the incremental ΔΣ ADC with extended counting and its timing diagram. The first stage stores the quantization noise (E_1) at the output of the second integrator (W_2) and then passes into a residue ADC. By combining each digital output, accuracy can be increased.

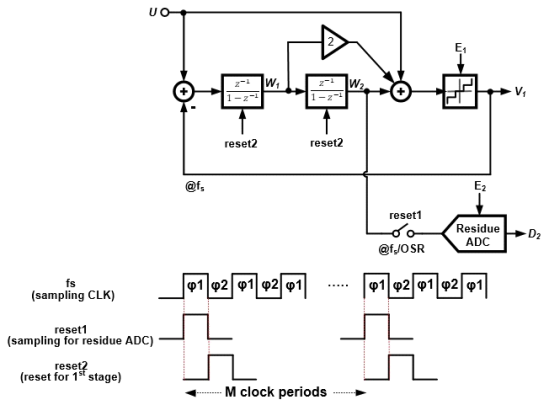

Fig. 9 Incremental ΔΣ ADC with extended counting

After M clock cycles, W_2 is

$$W_2[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} V[i] \quad (22)$$

With a linear quantizer model, D_2 is given as

$$W_2[M]+E_2[M]=D_2 \quad (23)$$

Combining Eq. (22) and (23) results in

$$\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} U[i]+E_2[M]=D_2+\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} V[i] \quad (24)$$

$$\widetilde{U}\cdot\frac{(M-1)\cdot(M-2)}{2}+E_2(M)= \quad (25)$$
$$D_2+\sum_{L=1}^{M}\sum_{i=1}^{L} V[i]$$

$$\therefore \widetilde{U}+\frac{2}{(M-1)\cdot(M-2)}\cdot E[M]= \quad (26)$$
$$\frac{2}{(M-1)\cdot(M-2)}\cdot\left(\sum_{L=1}^{M-1}\sum_{i=1}^{L-1} V[i]+D_2\right)$$

Therefore, the digital filter of the incremental ΔΣ ADC with extended counting can be implemented as shown in Fig. 10.

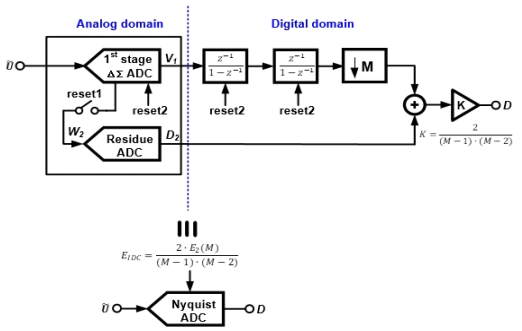

Fig. 10 Incremental $\Delta\Sigma$ ADC with extended counting and digital filter

4. 2+1 MASH incremental ΔΣ ADC

Fig. 11 shows a conventional 2+1 MASH (Multi-stAge-noise-SHaping) incremental ΔΣ ADC with a low-distortion-input feed-forward topology. The design equation can be derived in a similar manner to that shown above.

After M clock periods, W_2 and W_3 are expressed as

$$W_2[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i] \tag{27}$$

$$W_3[M]=\sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}U[i] -\sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]-\sum_{i=1}^{M-1}V_2[i] \tag{28}$$

V_2 is

$$W_3[M]\ +W_2[M]+E_2[M]=V_2[M] \tag{29}$$

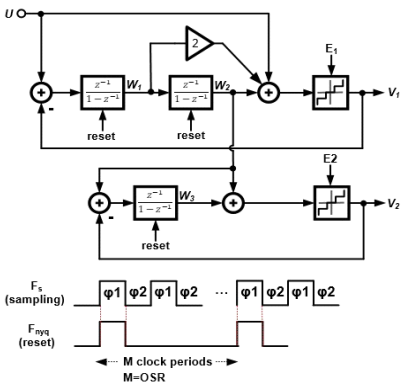

Fig. 11 2+1 MASH Incremental $\Delta\Sigma$ ADC and its timing diagram

Substituting W_2 and W_3 in Eq. (29) results in

$$\sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}U[i]+\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]+E_2[M]= \sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]+\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i]+\sum_{i=1}^{M}V_2[i] \tag{30}$$

$$\sum_{L=1}^{M}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}U[i]+E_2[M]= \sum_{L=1}^{M}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]+\sum_{i=1}^{M}V_2[i] \tag{31}$$

$$\widetilde{U}\cdot\frac{M\cdot(M+1)\cdot(M+2)}{6}+E_2(M)= \sum_{L=1}^{M}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]+\sum_{i=1}^{M}V_2[i] \tag{32}$$

$$\therefore \widetilde{U}+\frac{6}{M\cdot(M+1)\cdot(M+2)}\cdot E_2[M] =\frac{6}{M\cdot(M+1)\cdot(M+2)} \cdot\left(\sum_{L=1}^{M}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]+\sum_{i=1}^{M}V_2[i]\right) \tag{33}$$

Based on Eq. (33), the first stage requires two delayed integrators and one non-delayed integrator. The second stage needs only one non-delayed integrator. By sharing one non-delayed integrator to reduce the area, the digital filter of the 2+1 MASH incremental ΔΣ ADC can be implemented as shown in Fig. 12.

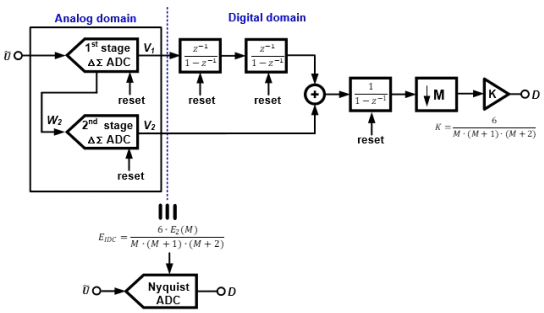

Fig. 12 2+1 MASH incremental $\Delta\Sigma$ ADC with digital filter

5. 2+2 MASH incremental ΔΣ ADC

As an extended version of the 2+1 MASH ADC, the 2nd-stage can be implemented as 2nd-order modulator to improve the ADC resolution, as shown in Fig. 13.

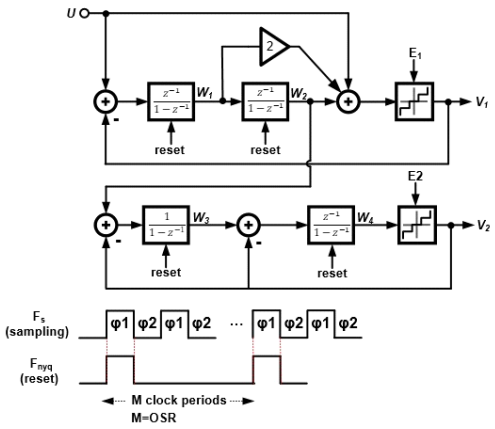

Fig. 13 2+2 MASH Incremental $\Delta\Sigma$ ADC and its timing diagram

After M clock periods, W_2, W_3, and W_4 are expressed as

$$W_2[M]=\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V[i] \tag{34}$$

$$W_3[M]=\sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}U[i] -\sum_{L=1}^{M-1}\sum_{K=1}^{L-1}\sum_{i=1}^{K-1}V_1[i]-\sum_{i=1}^{M-1}V_2[i] \tag{35}$$

$$W_4[M]=\sum_{M=1}^{K-1}\left(W_3[M]-V_2[M]\right) \tag{36}$$

Also,

$$W_4[M]+E_2[M]=V_2[M] \tag{37}$$

Combining Eq. (34)-(37) results in

$$\sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]-\sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i] -\sum_{L=1}^{M-1}\sum_{i=1}^{L}V_2[i]-\sum_{i=1}^{M-1}V_2[i]+E_2[M]=V_2[M] \tag{38}$$

$$\sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]+E_2[M]= \sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i]+\sum_{L=1}^{M-1}\sum_{i=1}^{L}V_2[i]+\sum_{i=1}^{M}V_2[i] \tag{39}$$

$$\sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}U[i]+E_2[M]= \sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i]+\sum_{L=1}^{M}\sum_{i=1}^{L}V_2[i] \tag{40}$$

$$\widetilde{U}\cdot\frac{M^4}{24}+E_2(M)= \sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i]+\sum_{L=1}^{M}\sum_{i=1}^{L}V_2[i] \tag{41}$$

$$\therefore\widetilde{U}+\frac{24}{M^4}\cdot E_2[M]= \frac{24}{M^4}\left(\sum_{N=1}^{O-1}\sum_{M=1}^{N}\sum_{L=1}^{M-1}\sum_{i=1}^{L-1}V_1[i]+\sum_{L=1}^{M}\sum_{i=1}^{L}V_2[i]\right) \tag{42}$$

Based on Eq. (42), the first stage requires two delayed integrators and two non-delayed integrators for the digital filter. The second stage needs only two non-delayed integrators, as shown in Fig. 14.

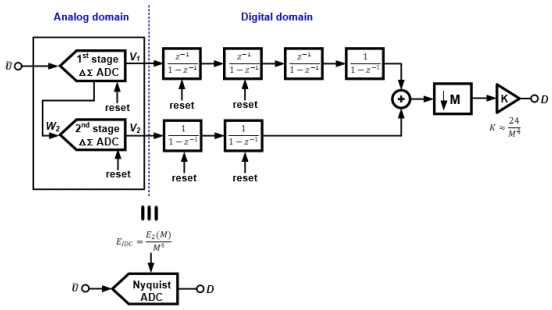

Fig. 14 2+2 MASH incremental $\Delta\Sigma$ ADC with digital filter

Ⅳ. Conclusions

In this study, simple design equations were derived to predict the performance of various incremental ADCs in the time domain. These design equations could help to implement a proper digital filter for many kinds of incremental ADC topologies to prevent performance degradation. Based on the design equations, we were able to easily choose the proper oversampling ratio and number of quantizer levels to meet the given specifications.

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