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Low-ripple coarse-fine digital low-dropout regulator without ringing in the transient state

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Herein, a low-ripple coarse-fine digital low-dropout regulator (D-LDO) without ringing in the transient state is proposed. Conventional D-LDO suffers from a ringing problem when settling the output voltage at a large load transition, which increases the settling time. The proposed D-LDO removes the ringing and reduces the settling time using an auxiliary power stage which adjusts its output current to a load current in the transient state. It also achieves a low output ripple voltage using a comparator with a complete comparison signal. The proposed D-LDO was fabricated using a 65-nm CMOS process with an area of 0.0056 μm^2. The undershoot and overshoot were 47 mV and 23 mV, respectively, when the load current was changed from 10 mA to 100 mA within an edge time of 20 ns. The settling time decreased from 2.1 μs to 130 ns and the ripple voltage was 3 mV with a quiescent current of 75 μA.

KEYWORDS

auxiliary power stage, coarse-fine, digital low dropout regulator (D-LDO), fast transient response, ringing

1 | INTRODUCTION

Digital low-dropout (D-LDO) regulators are used in portable devices, biomedical devices, and internet-of-things applications [1–10] because of their lower supply-voltage, small power-transistors, stability, and compatible processes. However, D-LDO features a long settling time and a ringing problem while settling the output voltage at large load transitions.

Several D-LDOs have been developed to reduce settling time [2–12] and D-LDOs with proportional-integral (PI) control removed the ringing. These devices used a level-crossing ADC with numerous reference voltages [2] and a delay line ADC with an analog voltage-to-current converter [3]. In [4], a steady-state load current (SLC) estimator was used to reduce ringing but required analog voltage-to-time and time-to-digital converters. Moreover, the PI control and SLC estimator were complex because they required an additional mathematical operator. Successive approximation register (SAR)-type D-LDO [5] improved the transient response with a binary PMOS array and removed ringing by using a proportional-derivative (PD) compensator. However, when the load current is significantly changed, the PD compensator increases or decreases the PMOS array current to match the load current. Here V_{OUT} reaches a minimum or maximum voltage, resulting in a long settling time. Coarse-fine D-LDOs [6,7] reduced the settling time using a large PMOS array and a high clock frequency in a coarse control loop, but exhibited large ringing in the transient state. In [6], a coarse-fine D-LDO reduced the ringing by using a current-mirror flash analog-to-digital converter and reference changer, but showed a slow transient response. In [7], the coarse-fine

D-LDO improved the transient response by using the peak detector to trigger coarse mode. The D-LDO turns a large PMOS transistor on or off at a fast clock cycle. However, this process causes a large ringing, which continuously re-triggers coarse mode and degrades stability. To prevent the large ringing, the coarse-fine D-LDO requires a guard time, the maximum possible settling time, to reactivate fine mode and stop the coarse mode, thereby increasing the overall time needed. In [8], the D-LDO reduces the transient response time by using a variable-gain accumulator, but exhibited a large undershoot voltage. Herein, a newly proposed coarse-fine D-LDO removes the ringing and reduces settling time by adding an auxiliary power stage. The novel device achieved a low output ripple voltage by using a comparator with a complete comparison signal. Section 2 describes the architecture of the proposed coarse-fine D-LDO and Section 3 shows the measurement results from the fabricated chip with the conclusions presented in Section 4.

2 | ARCHITECTURE

2.1 | Proposed coarse-fine digital low-dropout regulator

Figure 1 shows a conventional D-LDO consisting of a comparator, bidirectional shift-register, and PMOS array. The comparator compares the output voltage (V_{OUT}) with the reference voltage (V_{REF}). The bidirectional shift-register turns the PMOS transistor on or off in the PMOS array per clock cycle according to the comparator output, resulting in the regulation of V_{OUT} to V_{REF} by the D-LDO. When the load current (I_{LOAD}) is changed from light to heavy, as shown in Figure 1B, a large undershoot voltage is generated and the PMOS array output current (I_{OUT}) is increased. When V_{OUT} is minimized at time T_1, I_{OUT} is equal to I_{LOAD}. However, I_{OUT} increases continuously because V_{OUT} remained lower than V_{REF}. When V_{OUT} is equal to V_{REF} at time T_2, I_{OUT} became almost two times that of I_{LOAD}. Therefore, V_{OUT} increases continuously and an unwanted large overshoot voltage was generated. As a result, unwanted overshoot and undershoot voltages were generated until V_{OUT} settled to V_{REF} at time T_3, generating ringing and increasing the setting time [2–7].

However, the proposed D-LDO specifies that I_{OUT} is nearly equal to I_{LOAD} at time T_2 by turning off half of the turned-on PMOS transistors, as shown in Figure 1C. This process removed the unwanted large overshoot voltage and reduced settling time. The proposed D-LDO also adopted the coarse-fine PMOS arrays to achieve a fast transient response and low quiescent current [6,7].

Figure 2 shows the proposed coarse-fine D-LDO with an auxiliary power stage consisting of an auxiliary PMOS array and auxiliary shift-register (SR) attached to the conventional

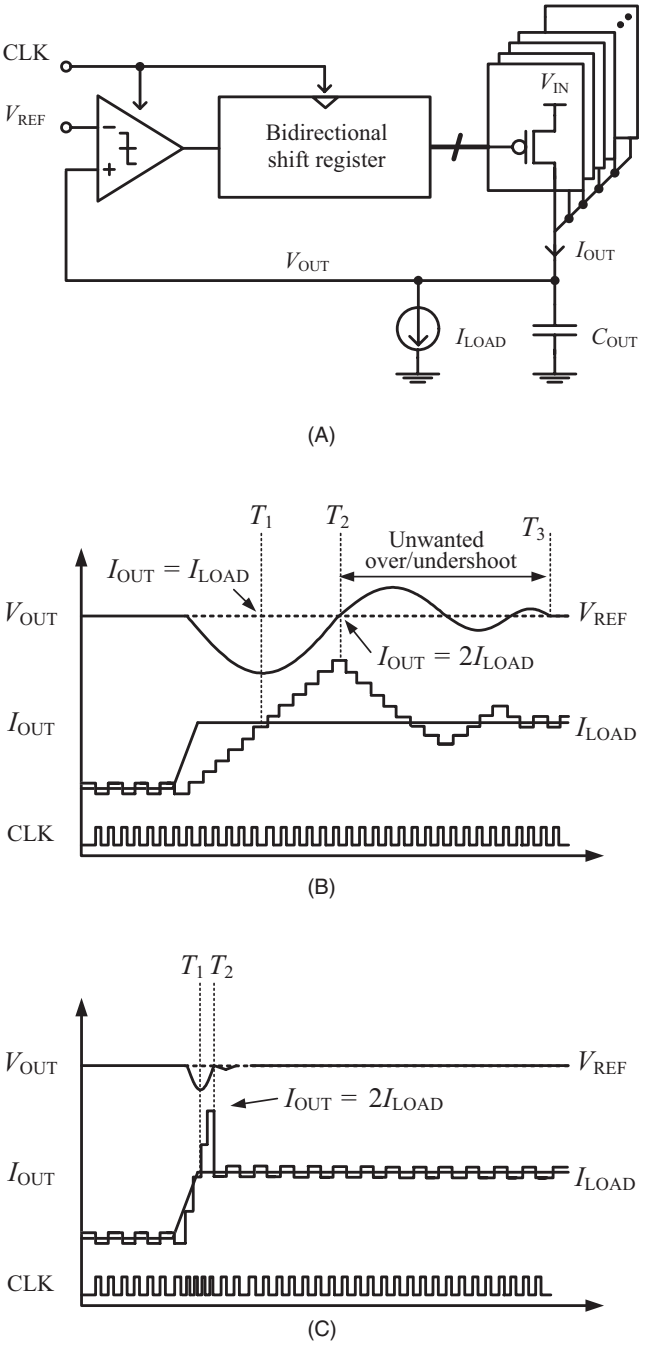


FIGURE 1 (A) Schematic and (B) waveforms of the conventional D-LDO. (C) Waveforms of the newly proposed D-LDO

coarse-fine D-LDO. The proposed D-LDO removed the large unwanted undershoot voltage by using the auxiliary power stage during undershooting. Moreover, the output ripple voltage was reduced and the transient response was enhanced by using a comparator with a complete comparison signal (DONE) (Figure 2B) operating the SR and Bi-SRs immediately after the comparison completes.

The D-LDO supplied a maximum output current when 32 coarse PMOS transistors were turned on. The auxiliary PMOS array increased the output current during the undershoot. When the load current was changed from light to

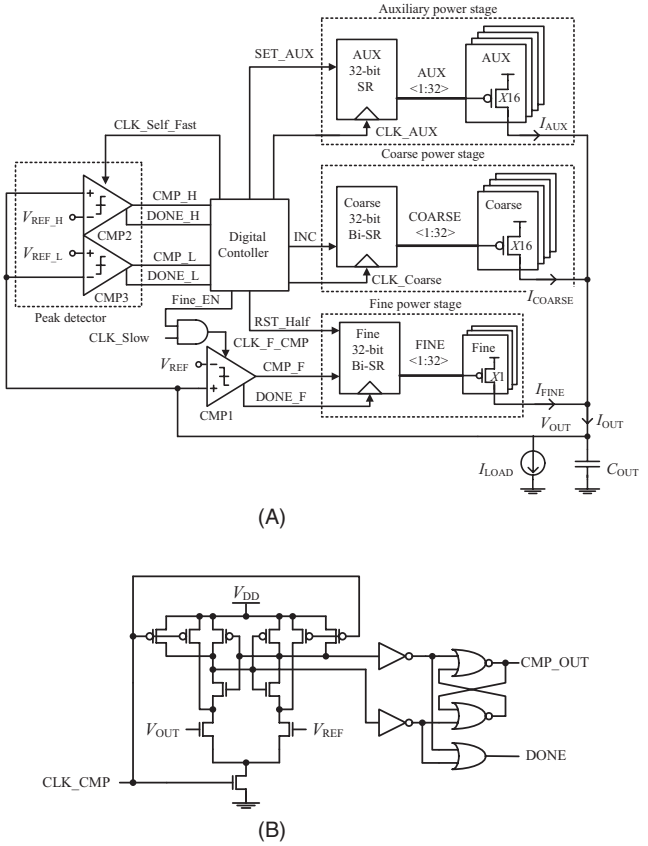


FIGURE 2 (A) Proposed coarse-fine D-LDO and (B) comparator with a comparison complete signal

heavy, the output current increased by as much as two large PMOS transistors per clock cycle by turning on both the auxiliary and coarse PMOS transistors. Therefore, the D-LDO requires 32 auxiliary PMOS transistors to cover the maximum load current changing. The fine PMOS array containing 32 PMOS transistors was designed to cover two coarse PMOS transistors.

In the steady state, the D-LDO finely adjusts the output current (I_{OUT}) using the fine power stage and CMP1 with a slow clock frequency (CLK_F_CMP = CLK_Slow). When the CMP1 compares V_{OUT} and V_{REF}, the fine 32-bit Bi-SR changes the fine PMOS array current (I_{FINE}) to the comparator output signal (CMP_F) by the complete comparison signal (DONE_F).

When the peak detector detects an overshoot or undershoot outside of V_{REF_H} and V_{REF_L}, CMP1 is deactivated (CLK_F_CMP = 0) and the coarse mode is triggered. Then, I_{FINE} becomes halved by the half reset signal (RST_Half). I_{OUT} is controlled coarsely using the coarse and auxiliary power stages via an asynchronous self-clock signal (CLK_Self_Fast) with a fast clock frequency to prevent the use of a high-frequency clock generator. The coarse PMOS array current (I_{COARSE}) decreased or increased from the coarse 32-bit Bi-SR according to the increased signal (INC) and coarse shift-register clock signal (CLK_Coarse). These two signals were changed according to the CMP2 output signals (CMP_H and DONE_H) or CMP3 output signals (CMP_L and DONE_L), when an overshoot (CMP_H = 1) or undershoot (CMP_L = 1) is generated, respectively. Except for the undershoot, the auxiliary PMOS array current remains at zero (I_{AUX} = 0) because the auxiliary 32-bit SR is set by the auxiliary set signal (SET_AUX = 1). When an undershoot is generated (CMP_L = 1), I_{AUX} increases from the auxiliary 32-bit SR as governed by the auxiliary clock signal (CLK_AUX) from CMP3 output signals (CMP_L and DONE_L).

Figure 3 shows the transient waveforms of the proposed D-LDO when undershoots and overshoots are generated. The coarse and auxiliary PMOS currents (I_{COARSE} and I_{AUX}) are 16 times greater than the fine PMOS current (I_{FINE}). The currents (I_{FINE}, I_{COARSE}, and I_{AUX}) increased or decreased as much as a PMOS transistor per clock cycle from the auxiliary and bidirectional shift-registers, as shown in Figure 4. Exceptionally, I_{COARSE} decreased as much as two PMOS transistors per clock cycle from the coarse bidirectional shift-register during the overshoot.

When the load current (I_{LOAD}) is changed from light to heavy, D-LDO detects the undershoot and operates under the coarse mode with a fast clock frequency. It increases both the I_{COARSE} and I_{AUX} until V_{OUT} reaches V_{REF_L}. When $V_{OUT} = V_{REF\_L}$, the output current (I_{OUT}) is nearly two times that of I_{LOAD}. Then, I_{OUT} becomes almost equal to I_{LOAD} by setting I_{AUX} to 0. Therefore, V_{OUT} can be settled within the

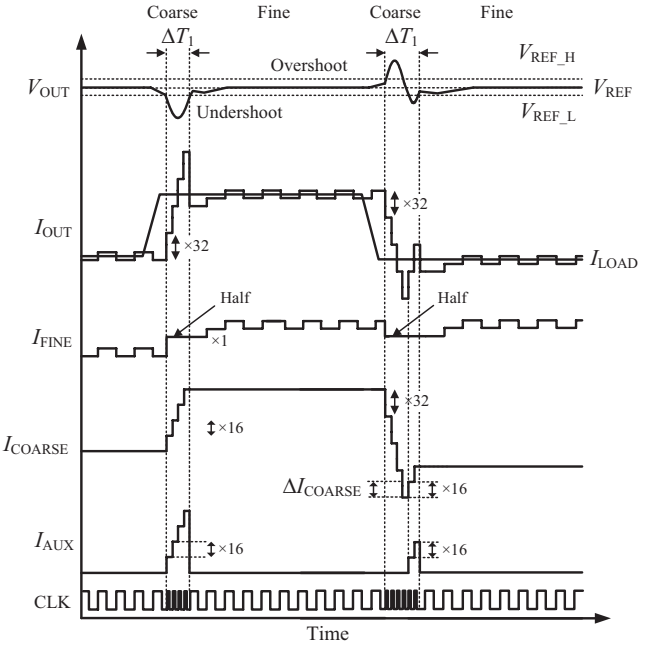


FIGURE 3 Transient waveforms of the proposed D-LDO when an undershoot and overshoot are generated

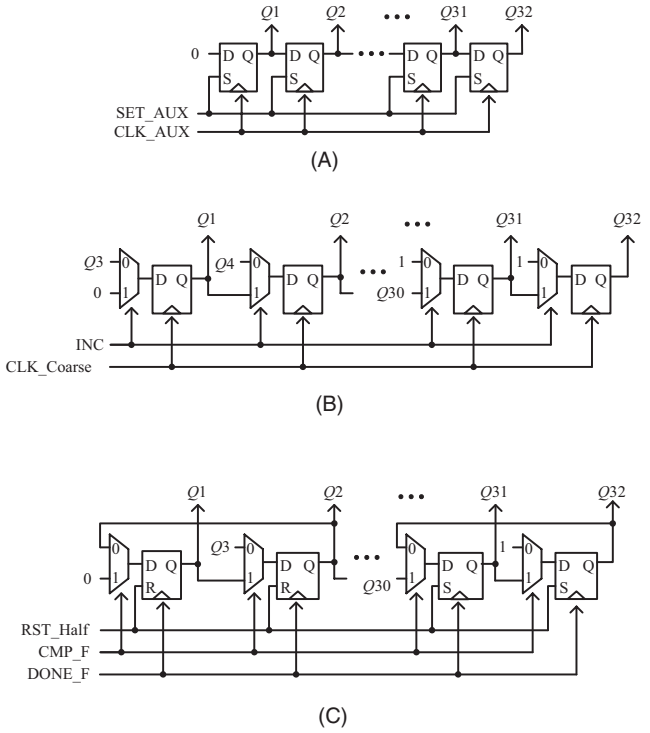


FIGURE 4 (A) Auxiliary shift-register, (B) coarse bidirectional shift-register, and (C) fine bidirectional shift-register

boundary voltages of V_{REF_L} and V_{REF_H}. In addition, fine mode is retriggered and V_{OUT} is finely regulated to V_{REF}.

When I_{LOAD} is changed from heavy to light, overshoot is detected and coarse mode is triggered. However, the auxiliary power stage is not operative, because I_{AUX} was set to 0. To improve the transient response, D-LDO decreases I_{COARSE} as much as two PMOS transistors per clock cycle. After V_{OUT} reaches the value of V_{REF_H}, V_{OUT} continually decreases, because I_{OUT} is smaller than that of I_{LOAD}, causing an undershoot. If the undershoot retriggers coarse mode, D-LDO operates in the same manner as the light-to-heavy load changing. If not, the D-LDO operates under fine mode. As a result, the D-LDO removes ringing, which improves the transient response for both the overshoot and undershoot.

When the coarse-fine D-LDO supplies the maximum or minimum I_{FINE} in fine mode, V_{OUT} is not regulated at V_{REF} because I_{FINE} does not show any further increases or decreases. The D-LDO requires regulation compensation to generate the large glitch voltage [7]. If I_{FINE} is fixed to the maximum or minimum before operating in coarse mode, regulation compensation occurs in the transient state. This generates a large glitch and may retrigger initiation of coarse mode. However, after the newly proposed D-LDO settles V_{OUT} within the boundary voltages of V_{REF_H} and V_{REF_L} during coarse tuning time (ΔT_1), the difference between I_{OUT} and I_{LOAD} falls between $-\Delta I_{COARSE}$ and ΔI_{COARSE}. The fine PMOS array can supply a current of 0-2 ΔI_{COARSE} and initially set to ΔI_{COARSE} by the half reset signal (RST_Half). Therefore, the novel D-LDO can regulate V_{OUT} to V_{REF} using the fine PMOS array in fine mode. This can remove the large glitch voltage of the regulation compensation in the transient state.

Figure 5 shows the digital controller where, in steady state, the fine enable signal (Fine_EN) was high because CMP_H = 0 and CMP_L = 0. CMP1 in Figure 2A operates by the fine comparator clock signal (CLK_F_CMP) with a slow clock frequency (CLK_Slow). The peak detector operates via asynchronous self-clock signal (CLK_Self_Fast) with a fast clock frequency, as shown in Figure 6. When the CLK_Self_Fast changes from low to high, CMP2 and CMP3 compare V_{OUT} with V_{REF_H} and V_{REF_L}, respectively. After both comparisons are performed, the complete comparison signals (DONE_H and DONE_L) become high and CLK_Self_Fast becomes low. This resets CMP2 and CMP3 so DONE_H and DONE_L become low again and CLK_Self_fast becomes high. In this manner, a fast-asynchronous self-clock signal is generated. Therefore, D-LDO can operate the peak detector by the fast-asynchronous self-clock signal without the need for a high-frequency clock generator.

When overshoot or undershoot is generated, as shown in Figure 7, the comparator output signal, CMP_H or CMP_L, respectively increases. Then, Fine_EN becomes lower and the fine PMOS array current (I_{FINE}; described

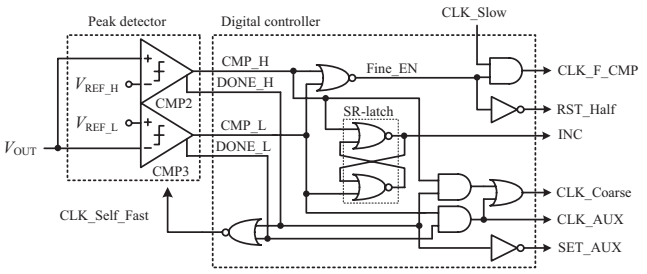


FIGURE 5 Schematics of the digital controller

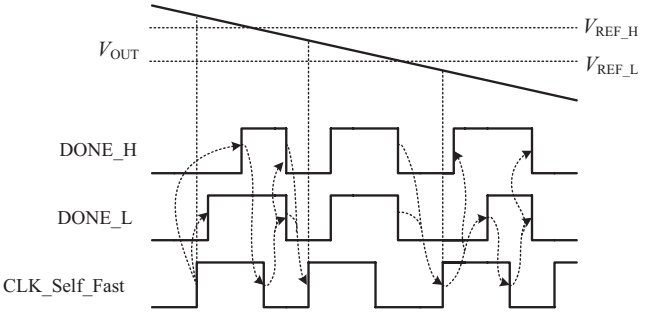


FIGURE 6 Timing diagram of the asynchronous self-clock signal

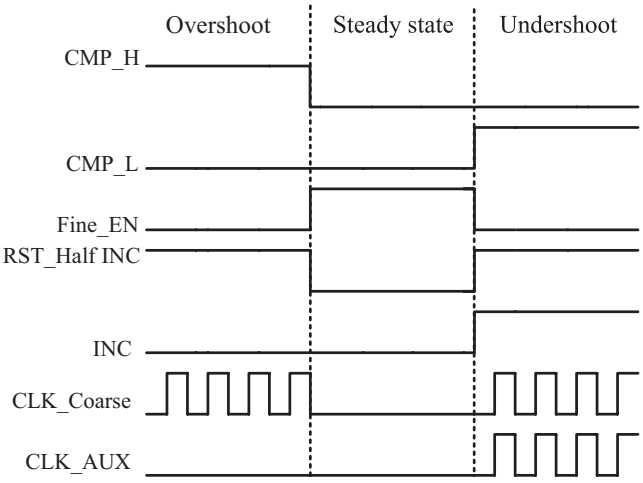


FIGURE 7 Timing diagram of coarse mode

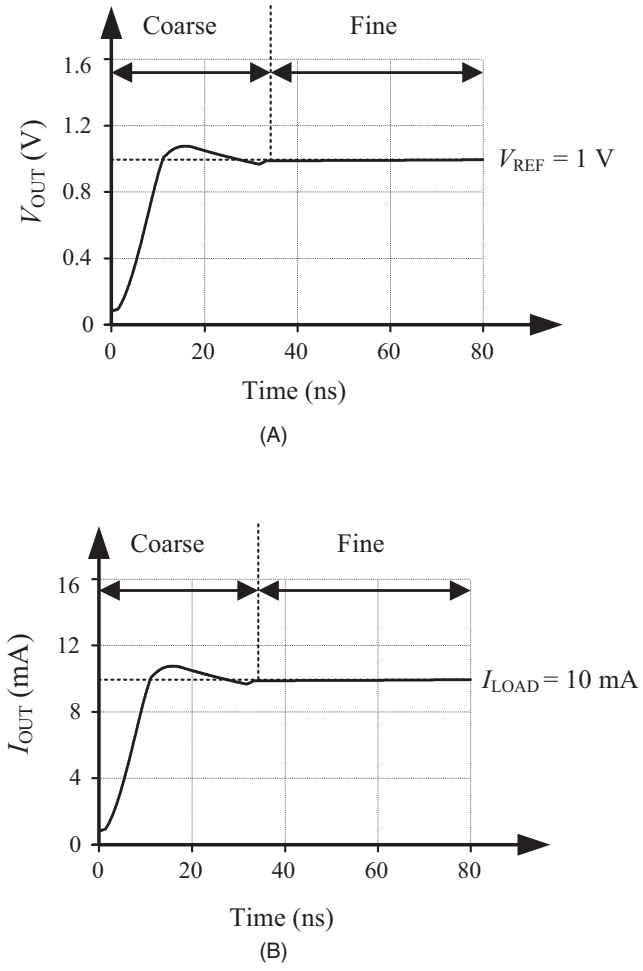


FIGURE 8 Transient waveforms of the newly proposed D-LDO during the start-up state: (A) V_{OUT} and (B) I_{OUT}

in Figure 2A) becomes halved due to the half reset signal (RST_Half). The coarse PMOS array current (I_{COARSE}) decreases or increases according to the increase signal (INC) via the coarse bidirectional shift-register clock

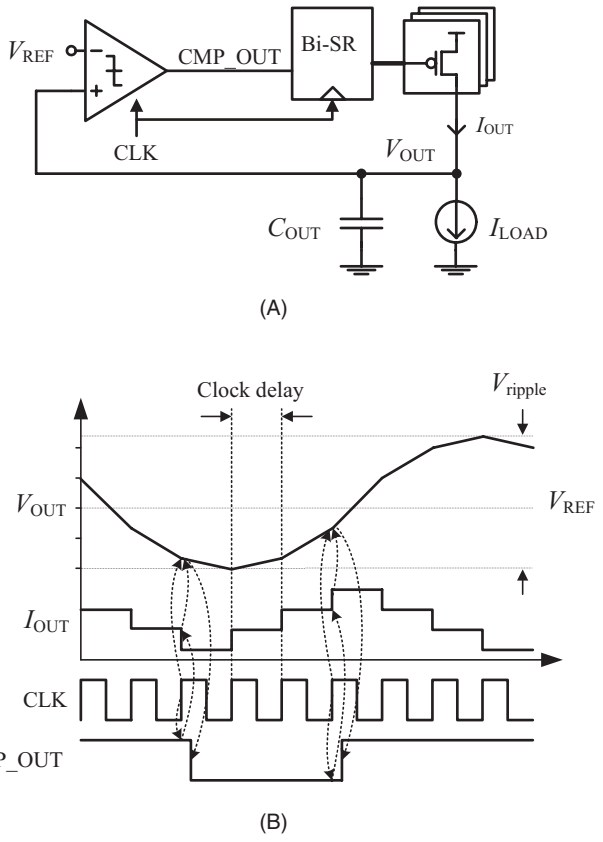
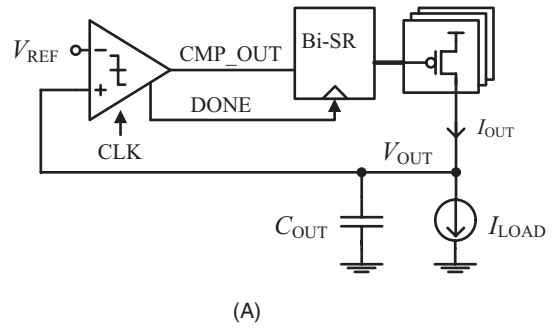


FIGURE 9 (A) Schematic and (B) transient waveforms of a conventional D-LDO when the comparator and bidirectional shift-registers operate using the same clock

signal (CLK_Coarse). The auxiliary PMOS array current (I_{AUX}) increased during the undershoot due to the auxiliary shift-register clock signal (CLK_AUX).

Figure 8 shows the transient waveforms of the newly proposed D-LDO in the start-up state. Initially, the novel D-LDO operates in coarse mode the same manner that caused the undershoot. When V_{OUT} is settled within the V_{REF_H} and V_{REF_L} boundary voltages, the D-LDO operates in fine mode and finely regulates V_{OUT} to V_{REF}.

Figures 9 and 10 show the ripple voltages (V_{ripple}) of the conventional and novel D-LDOs, respectively. The conventional D-LDO operates both the comparator and bidirectional shift-registers (Bi-SR) using the same clock (CLK). Bi-SR changes the output current (I_{OUT}) according to the comparator output signal CMP_OUT generated at the previous rising edge of CLK. This increases the ripple voltage caused by a single clock delay. However, the proposed D-LDO operates the Bi-SR with a complete comparison signal (DONE), as shown in Figure 10 [10]. Therefore, I_{OUT} changes as soon as the comparison is completed, reducing the ripple voltage. Table 1 shows a comparison of the ripple voltages of the two devices. The proposed D-LDO reduces the ripple voltage from 50.5 mV to 11.4 mV at CLK = 50 MHz.



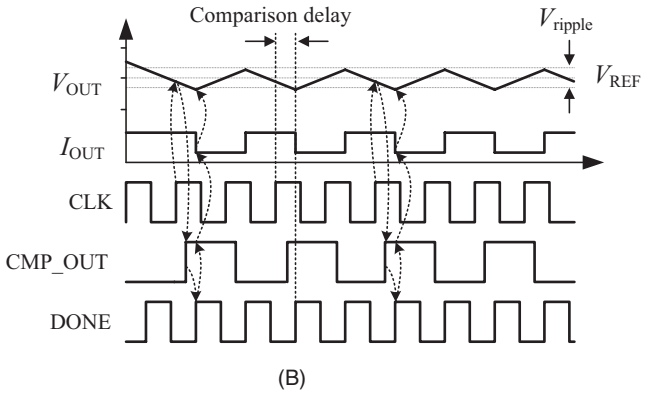


FIGURE 10 (A) Schematic and (B) transient waveforms of the proposed D-LDO using the comparator with a complete comparison signal

TABLE 1 Comparison of the obtained ripple voltages

	Conventional	Proposed
Technology	65 nm CMOS	
Supply voltage	1.2 V	
Clock frequency	50 MHz	
Ripple voltage @ I_{LOAD} = 10 mA	50.5 mV	11.4 mV (22.6%)

3 | EXPERIMENTAL RESULTS

The proposed D-LDO was fabricated using a 65-nm CMOS process with V_{DD} = 1.2 V. Figure 11 shows the chip microphotograph of the prepared D-LDO with an area of 0.0056 mm^2. The 1 nF output capacitor was incorporated on-chip, occupying 0.59 mm^2. The test bench was implemented on-chip to measure the output voltage during the load current changes. Figure 12 shows the measurement setup of the D-LDO at V_{DD} = 1.2 V and CLK_Slow = 50 MHz. V_{REF_H}, and V_{REF_L} are 15 mV above and below the V_{REF} of 1 V. The off-chip resistor, R_1, initially drives the light load current in the D-LDO. The on-chip resistor, R_2, and switch, S_1, in the

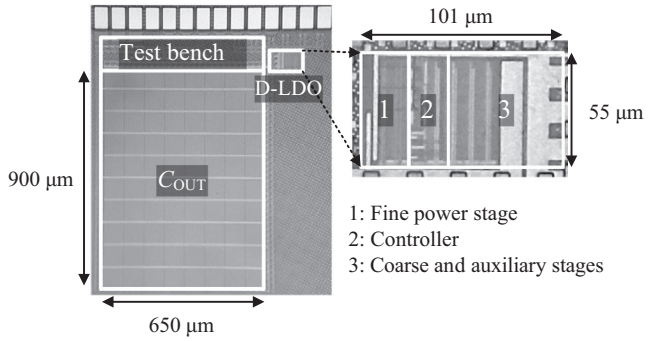


FIGURE 11 Microphotograph of the newly proposed D-LDO chip

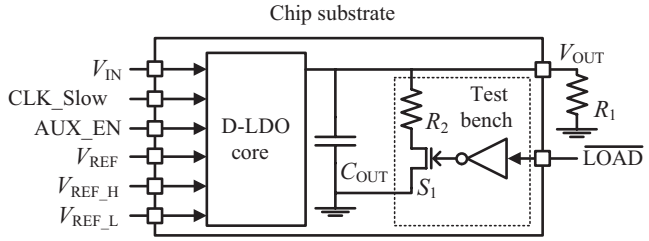


FIGURE 12 Measurement setup of the proposed D-LDO

test bench change the load current from light to heavy. An auxiliary enabled signal (AUX_EN) was then used to activate the auxiliary power stage.

Figure 13 shows the measurement of transient responses with and without the auxiliary power stage when the load current changed from 10 mA to 100 mA with rising and falling edge times of 20 ns at V_{IN} = 1.2 V and V_{OUT} = 1 V. In steady state, the D-LDO regulates V_{OUT} to 1 V from an input voltage of 1.2 V. When the load current was changed from 10 mA to 100 mA, the undershoot and overshoot of the proposed D-LDO decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively. In addition, the settling time decreased from 2.1 μs to 130 ns. The ripple voltage (V_{ripple}) was 4 mV only when using the proposed comparator.

Figure 14 shows the measurement the transient responses of the newly proposed D-LDO, when the load current changes from 10 mA to 100 mA with rising and falling edge times of 20 ns at V_{IN} = 1.2 V and V_{OUT} = 0.5 V. When the load current was changed from 10 mA to 100 mA, the undershoot and overshoot of the proposed D-LDO were 38 mV and 30 mV, respectively, with a settling time of 130 ns. The measured ripple voltage was 4 mV at the steady state at V_{OUT} = 1 V, V_{IN} = 1.2 V, and I_{OUT} = 10 mA, as shown in Figure 15. Table 2 shows the performance comparisons of various D-LDOs. The maximum output current was 100 mA, quiescent current was 75 μA, and peak current

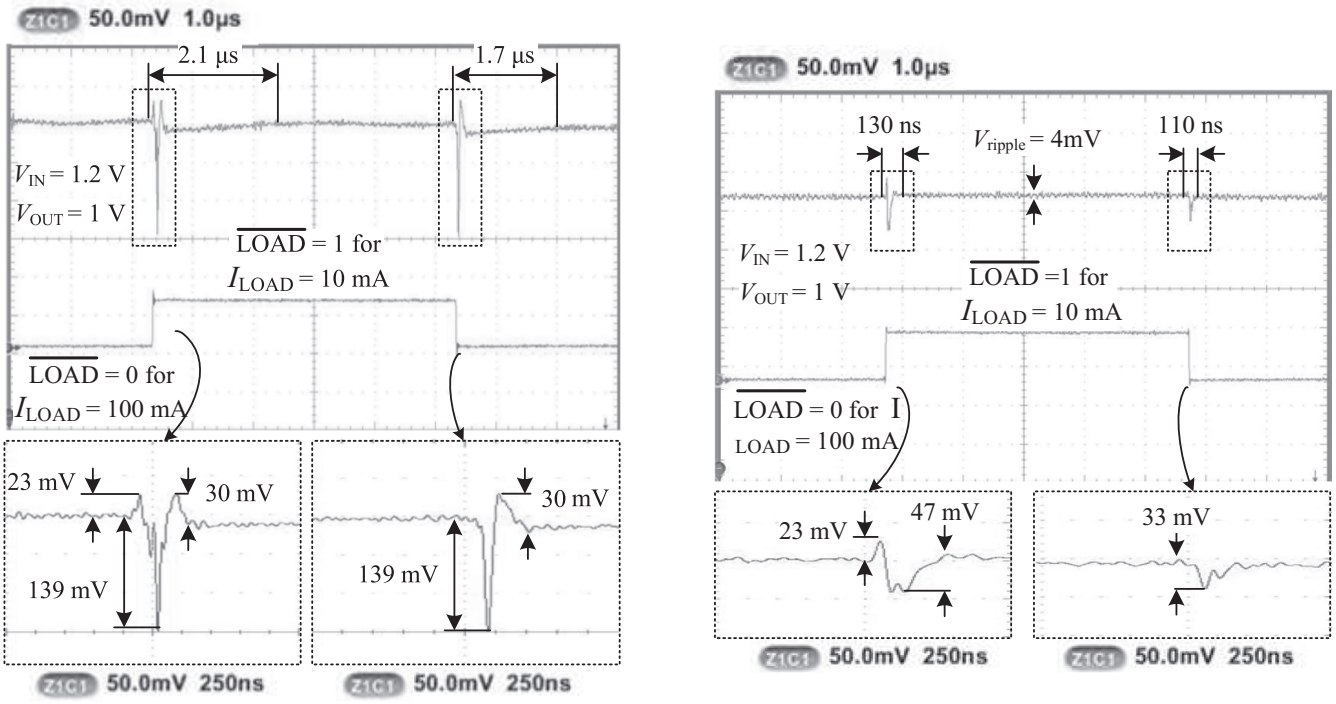


FIGURE 13 Measured transient response (A) without and (B) with the auxiliary power stage when the load current is changed from 10 mA to 100 mA with edge times of 20 ns at V_{IN} = 1.2 V and V_{OUT} = 1 V

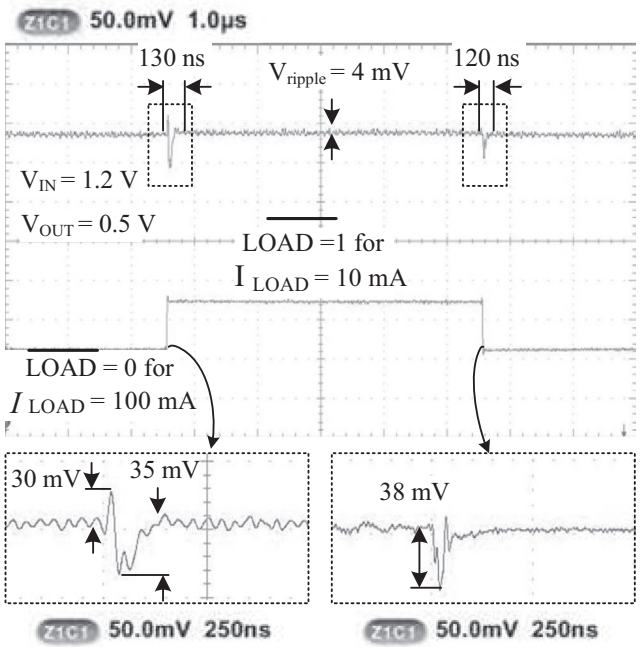


FIGURE 14 The measured transient response of the newly proposed D-LDO when the load current changes from 10 mA to 100 mA with edge times of 20 ns at V_{IN} = 1.2 V and V_{OUT} = 0.5 V

efficiency was 99.93% with a power supply rejection ratio (PSRR) of 53.9 dB at DC.

The widely used figure-of-merit (FoM) for D-LDOs [3,5–7] can be described as follows:

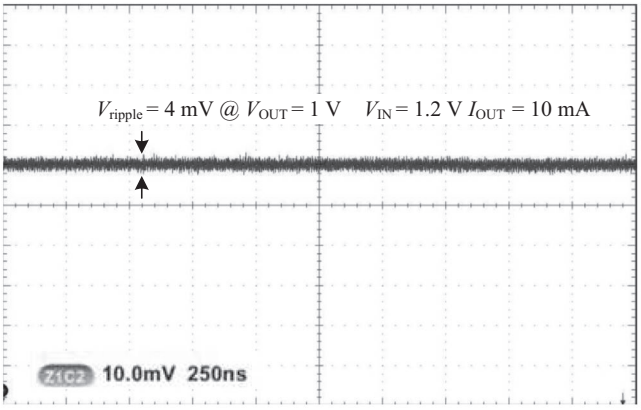


FIGURE 15 The measured ripple voltage at the steady state at V_{OUT} = 1 V, V_{IN} = 1.2 V, and I_{OUT} = 10 mA

$$\text{FoM} = \frac{C_{OUT} \cdot \Delta V_{OUT}}{\Delta I_{LOAD}} \frac{I_Q}{\Delta I_{LOAD}},$$

where C_{OUT} is the output capacitance, ΔV_{OUT} is the maximum undershoot voltage, I_Q is the quiescent current, and ΔI_{LOAD} is the load current change range. Coarse-fine D-LDOs exhibit smaller FoMs than other control-type D-LDOs. The newly proposed D-LDO exhibited the smallest settling time among coarse-fine D-LDOs by removing ringing in the transient state.

TABLE 2 Performance comparisons of previously reported D-LDOs and that developed herein

	ISSCC 2017 [5]	PE 2019 [11]	VLSI 2017 [3]	PE 2018 [8]	JSSC 2017 [6]	TCAS II 2016 [7]	This Work
Technology (nm)	65	130	130	65	28	65	65
Control	SAR/PD/PWM	Adaptive	Delay ADC/PI	S-DLDO	Coarse-fine	Coarse-fine	Coarse-fine
Active area (mm^2)	0.0023	0.18	0.0631	0.014	0.021	0.01	0.0056
Input voltage (V)	0.5–1.0	0.50–1.22	0.84–1.24	0.7–1.2	1.1	0.6–1.1	0.6–1.2
Output voltage (V_{OUT}, V)	0.30–0.45	0.35–1.17	0.6–1.0	0.6–1.1	0.9	0.4–1.0	0.5–1.0
Load current (I_{LOAD}, mA)	2	145	50	25	200	100	100
Quiescent current (I_Q, μA)	14	3,200	400	6	110	82	75
Peak current efficiency (%)	99.8	97.8	99.2	99.9	99.94	99.92	99.93
Load regulation (mV/mA)	5.6	N/A	0.4	0.04	N/A	0.06	0.13
Line regulation (mV/V)	2.3	N/A	N/A	N/A	N/A	3	2
PSRR@DC	N/A	N/A	N/A	N/A	N/A	N/A	53.9 dB
Output capacitance (C_{OUT}, nF)	0.4	1.5	0.5	1.0	23.5	1.0	1.0
Edge time	<1 ns	0.1 ns	10 ns	N/A	4 μs	20 ns	20 ns
ΔV_{OUT}@ΔI_{LOAD}	40 mV @1.06 mA	280 mV @40 mA	250 mV @50 mA	200 mV @23.5 mA	120 mV @180 mA	55 mV @98 mA	47 mV @90 mA
Settling time (μs)	0.1	0.05	0.25	2.08	>10	0.7[a]	0.13
FoM (ps)	199	63.9	20	2.17	7.75	0.43	0.43

[a]Maximum possible settling time ≈1.2 μs.

4 | CONCLUSIONS

A low-ripple coarse-fine D-LDO without ringing in the transient state was proposed herein. It removes the ringing and improves the transient response using an auxiliary power stage, which reduces the output ripple voltage by using a comparator with a complete comparison signal. The undershoot and overshoot decreased from 139 mV to 47 mV and 30 mV to 23 mV, respectively. The settling time decreased from 2.1 μs to 130 ns and the ripple voltage was 4 mV.

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REFERENCES

1. Y. Okuma et al., *0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS*, Proc. IEEE Custom Integr. Circuits Conf., San Jose, CA, USA, Sept. 2010, pp. 1–4.
2. D. Kim and M. Seok, *Fully integrated low-drop-out regulator based on event-driven pi control*, in Proc. IEEE Int. Solid-State Circuits Conf., San Francisco, CA, 2016, pp. 148–149.
3. C. Y. Lim et al., *A 50-mA 99.2% peak current efficiency, 250-ns settling time digital low-dropout regulator with transient enhanced PI controller*, IEEE Trans. Very Large Scale Integr. Syst. **25** (2017), no. 8, 2360–2370.
4. J.-H. Lin et al., *A digital low-dropout-regulator with steady-state load current (SLC) estimator and dynamic gain scaling (DGS) control*, in Proc. IEEE Asia Pacific Conf. Circuits Syst., Jeju, Rep. of Korea, 2016, pp. 25–28.
5. L. G. Salem, J. Warchall, and P. P. Mercier, *A 100 nA-to-2 mA successive-approximation digital LDO with PD compensation and sub-LSB duty control achieving a 15.1 ns response time at 0.5 V*, in Proc. IEEE Int. Solid-State Circuits Conf., San Francisco, CA, 2017, pp. 5–9.
6. Y.-J. Lee et al., *A 200 mA digital low-drop-out regulator with coarse-fine dual loop in mobile application processors*, IEEE J. Solid-State Circuits **52** (2017), no. 1, 64–76.
7. M. Huang et al., *A fully integrated digital LDO with coarse fine tuning and burst-mode operation*, IEEE Trans. Circuits Syst. II: Express Briefs **63** (2016), no. 7, 683–687.
8. M.-A. Akram, W. Hong, and I.-C. Hwang, *Fast transient fully standard cell-based all digital low-dropout regulator with 99.97% current efficiency*, IEEE Trans. Power Electron. **33** (2018), no. 9, 8011–8019.

9. K.-C. Woo et al., *A fast-transient digital LDO using a double edge-triggered comparator with a completion signal*, in Proc. Int. Conf. Electron., Inf., Commun., Honolulu, HI, 2018, pp. 1–4.
10. A. Singh et al., *A digital low-dropout regulator with auto-tuned PID compensator and dynamic gain control for improved transient performance under process variations and aging*, IEEE Trans. Power Electron. **35** (2020), no. 3, 3242–3253.
11. T.-J. Oh and I.-C. Hwang, *A 110-nm CMOS 0.7-V input transient-enhanced digital low-dropout regulator with 99.98% current efficiency at 80-mA Load*, IEEE Trans. Very Large Scale Integr. Syst. **23** (2015), 1281–1286.
12. K.-C. Woo and B.-D Yang, *A digital low-dropout regulator with a voltage differential detector for removing transient oscillation*, J. Semiconductor Technol. Sci. **19** (2019), 492–497.

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