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A dual-path high linear amplifier for carrier aggregation

Dong-Woo Kang | **Jang-Hong Choi**

AI Compact SoC Research Section, Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea

Correspondence
Dong-Woo Kang, AI Compact SoC Research Section, Electronics and Telecommunications Research Institute, Rep. of Daejeon, Korea.
Email: dw77.kang@etri.re.kr

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Abstract

A 40 nm complementary metal oxide semiconductor carrier-aggregated drive amplifier with high linearity is presented for sub-GHz Internet of Things applications. The proposed drive amplifier consists of two high linear amplifiers, which are composed of five differential cascode cells. Carrier aggregation can be achieved by switching on both the driver amplifiers simultaneously and combining the two independent signals in the current mode. The common gate bias of the cascode cells is selected to maximize the output 1 dB compression point (P1dB) to support high-linear wideband applications, and is used for the local supply voltage of digital circuitry for gain control. The proposed circuit achieved an output P1dB of 10.7 dBm with over 22.8 dBm of output 3rd-order intercept point up to 0.9 GHz and demonstrated a 55 dBc adjacent channel leakage ratio (ACLR) for the 802.11af with −5 dBm channel power. To the best of our knowledge, this is the first demonstration of the wideband carrier-aggregated drive amplifier that achieves the highest ACLR performance.

KEYWORDS

adjacent channel leakage ratio, carrier aggregation, complementary metal oxide semiconductor, driver amplifier

1 | INTRODUCTION

Recently, sub-GHz wireless technology has started to gain considerable attention due to longer propagation distance and better penetration characteristic for the Internet of Things (IoT) technologies, which are termed as low-power wide area network [1,2]. Many standards, such as Sigfox [3], LoRa [4], and 802.15. 4g [5], are available for these sub-GHz solutions to realize smart grids for automated metering, security systems, and the Internet of things. The IEEE 802.11 task group also has proposed the new PHY and MAC standards called 802.11ah (Wi-Fi Halow) and 802.11af operating at the sub-GHz band [6,7]. Although long-range and short-burst data transmissions are essential for most mobile sensor networks, some applications, such as a backhaul link or a high-speed internet, must provide large coverage area and high data rates. One of the solutions is to aggregate several contiguous or non-contiguous channels with different communication standards [8]. Figure 1 shows a transmitter architecture capable of carrier aggregation using two separated local oscillators (LO), a wideband drive amplifier, and a power combiner. The two LOs provide independent data transmission for 802.11af as well as 802.11ah. In particular, the transmit spectrum of 802.11af should be satisfied with the requirement of a 55 dBc adjacent channel leakage ratio (ACLR) [9]. Therefore, the main challenge in the transmitter is the design of a wideband high-linear operation [10–12]. The linearity of the transmitter is mostly affected at the final stage, which is the output drive amplifier. Moreover, both

the drive amplifiers have to meet the linearity requirement owing to the carrier aggregation. In this paper, we present a wideband high-linear drive amplifier that is capable of carrier aggregation and programmable gain control. The spectral emission mask of each path achieves the 55 dBc ACLR requirement owing to a high-linear amplification. A two-path carrier aggregation is realized using a wideband gain characteristic and combined output of up to 1 GHz, thereby supporting the sub-GHz standards.

2 | CIRCUIT DESIGN

Figure 2 shows the schematic of the driver amplifier, which has a differential cascode structure. For wideband output matching over sub-GHz, an off-chip transformer with an impedance ratio of 2:1 is employed. The transformer reduces the current of the driver amplifier by half, while doubling the voltage swing. Therefore, a thin-oxide device (40 nm) for the common source stage and a thick-oxide device (270 nm) for the common-gate stage are stacked together to prevent reliability issues due to the dielectric breakdown condition. Moreover, the differential topology reduces the output voltage stress at one of the differential pairs by half. For an output power of 10 dBm, the output voltage swing experienced by the single cascode structure is only 1 Vp-p.

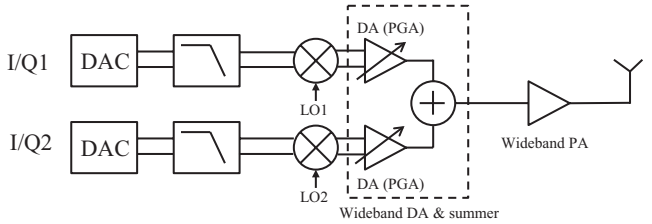
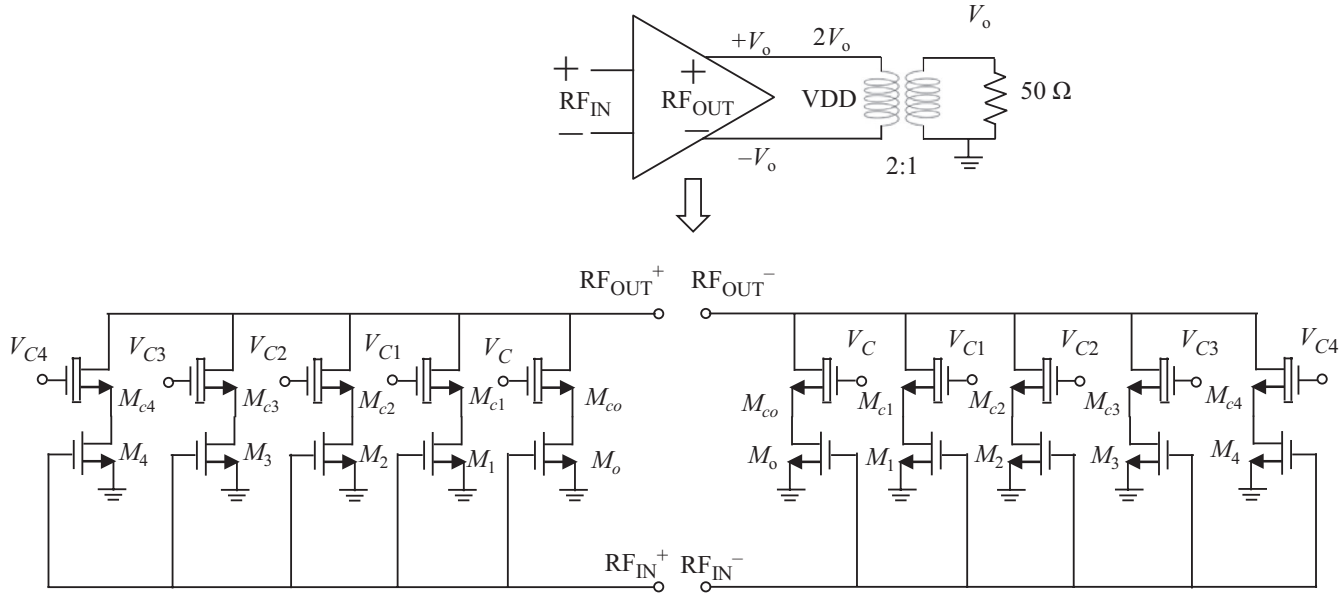


FIGURE 1 Transmitter structure capable of a carrier aggregation

Figure 3 shows simulated voltage waveforms at the drain nodes of the common source transistors and a single-ended output node when the circuit operates at the 1 dB compression point (P1dB) condition with a 900 MHz input signal. According to the time-dependent dielectric breakdown condition, the rms voltage across each transistor should not exceed the maximum supply voltage [12]. The maximum dc supply voltages for the 40 nm and 270 nm devices have been specified as 1.1 V and 2.75 V, respectively, in the design manual of the foundry. Therefore, the cascode topology with a thin-oxide and a thick-oxide device can solve the reliability issue with enough output power level.

The circuit is composed of five differential cascode cells controlled by common-gate transistors (M_{c0}, …, M_{c4}), which provide the function of gain control. The total voltage gain (A_V) is calculated as



	W/L (μm)		W/L (μm)		W/L (μm)		W/L (μm)
M_0, M_1	24/0.04	M_2	53/0.04	M_3	108/0.04	M_4	216/0.04
M_{c0},M_{c1}	24/0.27	M_{c2}	53/0.27	M_{c3}	134/0.27	M_{c4}	288/0.27

FIGURE 2 Schematic of the single-path driver amplifier

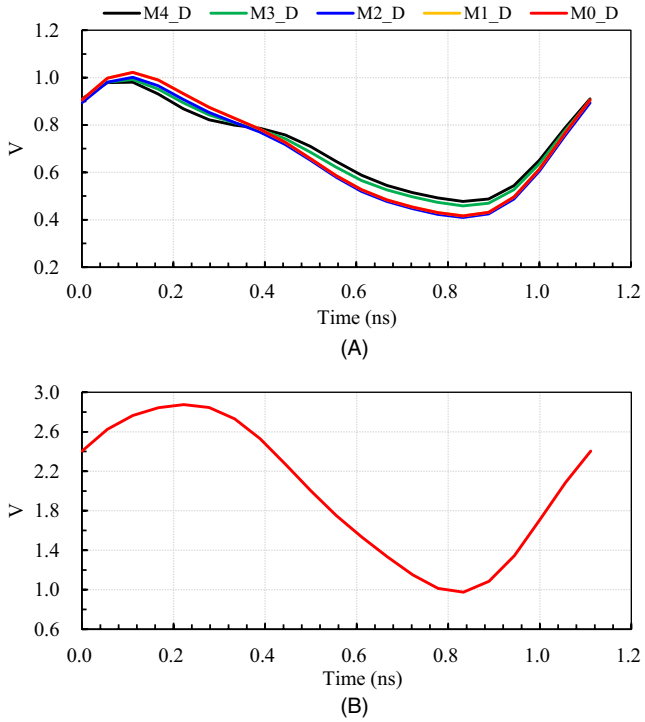


FIGURE 3 Simulated voltage waveforms of (A) drain nodes of 40 nm device (M0–M4) and (B) the output node (RF_{out+}) when the circuit operates at the P1dB condition

$$A_V = \left(g_{m0} + g_{m1} + g_{m2} + g_{m3} + g_{m4}\right) R_L, \tag{1}$$

where g_{mn} (n is 0–4) is the trans-conductance of each cascode cell and R_L is the impedance looking into the transformer. For a total gain range of 24 dB with a 6 dB step, each trans-conductance is expressed as follows:

$$\begin{aligned} g_{m1} &= g_{m0}, \\ g_{m2} &= 2g_{m1} = 2g_{m0}, \\ g_{m3} &= 2g_{m2} = 4g_{m0}, \\ g_{m4} &= 2g_{m3} = 8g_{m0}. \end{aligned} \tag{2}$$

Thus, each gain can be expressed as follows:

$$\begin{aligned} A_{V\_max} &= g_{m0} + g_{m1} + g_{m2} + g_{m3} + g_{m4}\ R_L = 16g_{m0}R_L\ , \\ A_{V\_6dB} &= g_{m0} + g_{m1} + g_{m2} + g_{m3}\ R_L = 8g_{m0}R_L, \\ A_{V\_12dB} &= g_{m0} + g_{m1} + g_{m2}\ R_L = 4g_{m0}R_L, \\ A_{V\_18dB} &= g_{m0} + g_{m1}\ R_L = 2g_{m0}R_L \\ A_{V\_min} &= g_{m0}\ R_L. \end{aligned} \tag{3}$$

As the trans-conductance is proportional to the size of the cascode cell, the gain control can be realized by doubling the size of each cascode cell in order. However, the gain drops slightly (0.1 dB–0.3 dB) with an increase in the size of the transistors due to an increase in the drain capacitances. The gain including each capacitance of the cascode cell is expressed as follows:

$$A_V = j\frac{g_{m_S} g_{m_G}}{\omega C_S C_G} \frac{R_L}{j\omega + g_{m_G}/C_S}, \tag{4}$$

where C_S and C_B are the drain node capacitance of the common source transistor and the common-gate transistor, respectively; and g_{m_S} and g_{m_G} are the trans-conductance of the common source transistor and the common-gate transistor, respectively. Therefore, we increased the size of the transistors slightly to precisely meet the 6 dB gain step.

Only one cascode cell (M_O–M_{CO}), which has the minimum gate width among the other cascode cells, is always switched on by connecting the common-gate bias (V_c) to a fixed bias. Thus, it provides a minimum gain state. The other bias of the cascode cells is controlled by V_{cn} (where n is 1, 2, 3, and 4) through a thermometer code that prevents an undesired glitch issue, instability in gain control loop, and phase discontinuity between the gain states [13]. In particular, the transmit emission mask in the 801.11af system is extremely stringent because the system utilizes an unused channel in the TV white spectrum. It also requires the function of power control to achieve the necessary power level. The signal glitch due to the gain transition can result in spurious emission and affect the other channels; thus, it should be relaxed by a monotonous gain adjustment through the thermometer code rather than a binary code [14].

In the maximum gain setting, the linearity of the driver amplifier should be considered owing to the high ACLR requirement (55 dBc ACLR) for the 802.11af system. The drain current of the cascode amplifier mainly affects the overall distortions, and it can be expanded in a Taylor series [15], which is given by

$$i_{DS}\left(V_{GS} + v_{gs}\right) = i_{DS}\left(V_{GS}\right) + G_1 v_{gs} + G_2 v_{gs}^2 + G_3 v_{gs}^3 + \cdots \tag{5}$$

The drain current is determined by the drain bias of the common source transistor, which is also dependent on the gate bias of the cascode transistor.

$$V_{DS\_CS} \cong V_{g\_CS} + V_{sig\_in} - V_{th\_CG}. \tag{6}$$

For the all transistors to be saturated, the following condition should be satisfied.

$$V_{g\_CS} \le V_{DD} - V_{sig\_out} + V_{th\_CG}, \tag{7}$$

where V_{DS_CS} is the drain bias of the common source transistor; V_{g_CS} and V_{th_CG} are the gate bias and the threshold voltage of the common-gate transistor, respectively. V_{sig_in} is an envelope of the input signal, and V_{sig_out} is an envelope of the output signal.

For a supply voltage of 2 V and a V_{th_CG} of 0.5 V, the gate bias of the common source should be below 1.5 V to generate a linear output power of 10 dBm (V_{sig_out} is 1 V). Therefore, the common-gate bias (V_c) can be optimized for high linearity performance of the driver amplifier. Figure 4 shows a simulated output P1dB for differential outputs according to the variation in the value of V_c at an input frequency of 900 MHz. The maximum output P1dB is in the range of 14.5 dBm to 14.7 dBm for the value of V_c in the range of 1.4 V–1.5 V. For the optimum value of V_c of 1.5 V, the simulated 3rd-order intermodulation distortion (IMD3) for a two-tone signal with 6 MHz tone spacing at a 900 MHz center frequency is shown in Figure 5. The IMD3 is below 55 dBc for a −2 dBm output power.

The core digital supply is 1.1 V, which is the control voltage for the gain bits ($G0$, $G1$, $G2$, and $G3$) and power down (PD) bit. Figure 6 shows the schematic of the gain controller providing the optimum bias V_c. To apply the common-gate bias to the optimum voltage according to the gain change, a digital buffer with a supply voltage of V_c is added to each common gate. The V_c is derived from the resistive divider network from the system supply voltage of 2 V. This toggles the common-gate voltage from 0/1.1 V to 0/1.5 V. Therefore, high linearity and gain control can be achieved simultaneously.

Figure 7 shows a block diagram of the two-path driver amplifier. The core chip (the dashed area) operates in a differential mode, and each input transformer (1:1) converts a single-ended WLAN signal to a differential signal for the purpose of measurement. The output impedance of the chip is matched differentially to 200 Ω, which is transformed to 50 Ω using an external wideband transformer (TCM4-14+, Mini-Circuits).

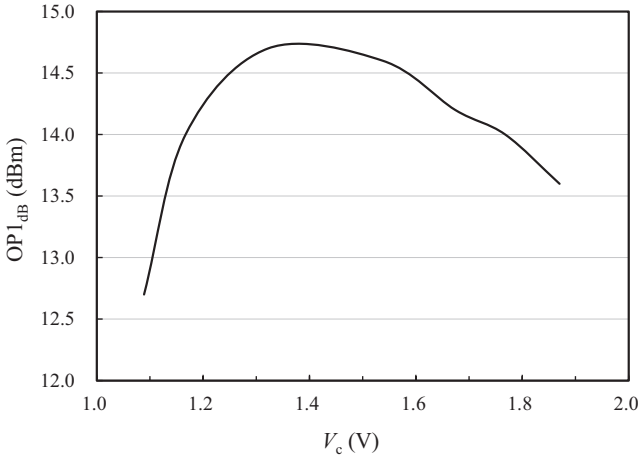


FIGURE 4 Simulated output P1dB according to the V_c

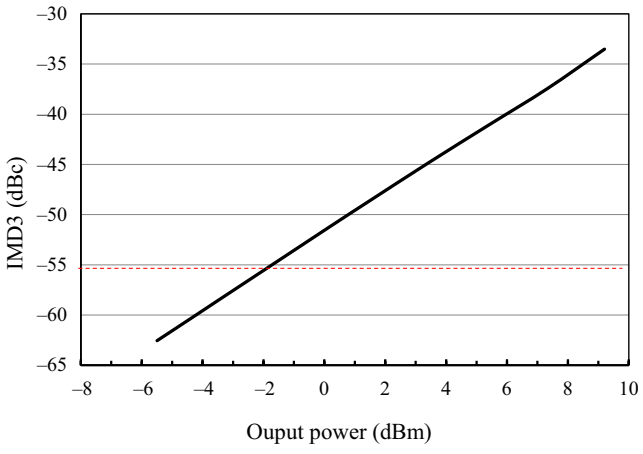


FIGURE 5 Simulated IMD3 according to the output power

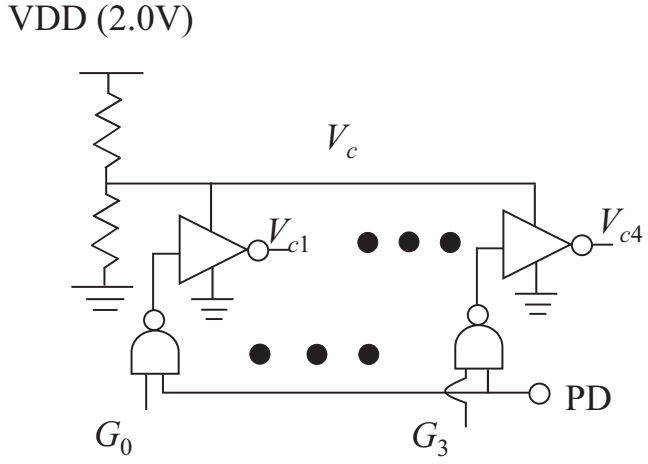


FIGURE 6 Schematic of the optimum voltage generation circuit

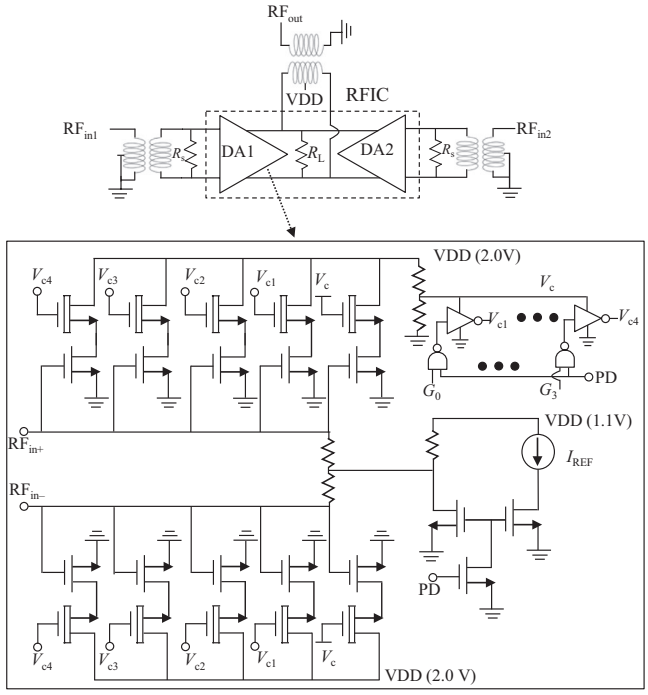
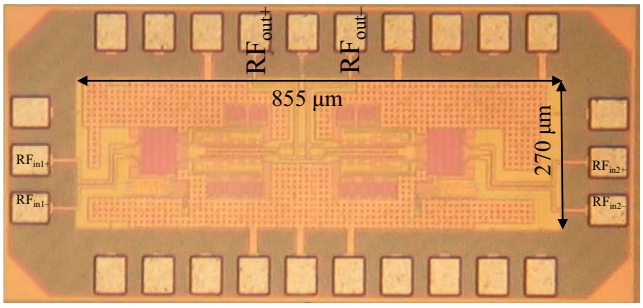
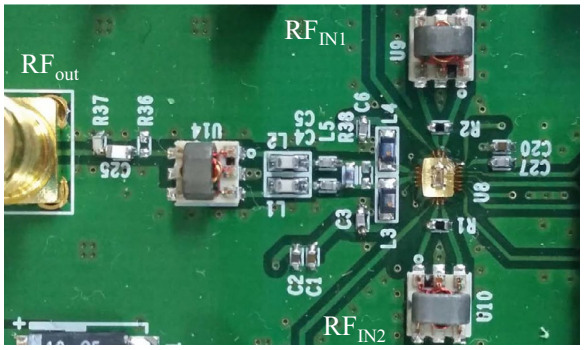


FIGURE 7 Block diagram of the proposed two-path drive amplifier



(A)



(B)

FIGURE 8 Images of (A) fabricated chip and (B) chip on board

The dashed box is a designed chip fabricated using the CMOS technology. The right part (DA2) is a replica of the left part (DA1). A detailed schematic of one of the parts is shown below. By switching on or off one of the parts, the circuit operates in a single or carrier-aggregated mode. The PD signal of the bias circuitry enables all the common source transistors to be turned off. It is also applied to control the common-gate transistors to minimize the leakage current. When the PD signal of each part is disabled simultaneously, the output currents of each path are combined through the load resistor (R_L), which provides the carrier aggregation of RF_{in1} and RF_{in2} as well as the conversion of voltage from current.

3 | MEASUREMENTS

The proposed carrier-aggregated driver amplifier is implemented in a 40 nm complementary metal oxide semiconductor (CMOS) process, occupying a core area of 855 μm × 270 μm, as shown in Figure 8A. The fabricated chip is attached to an FR4 board with off-chip transformers and matching elements as shown in Figure 8B. All radio frequency (RF) signals, bias, and control lines are wire bonded to the printed circuit board (PCB). The cascode stage was

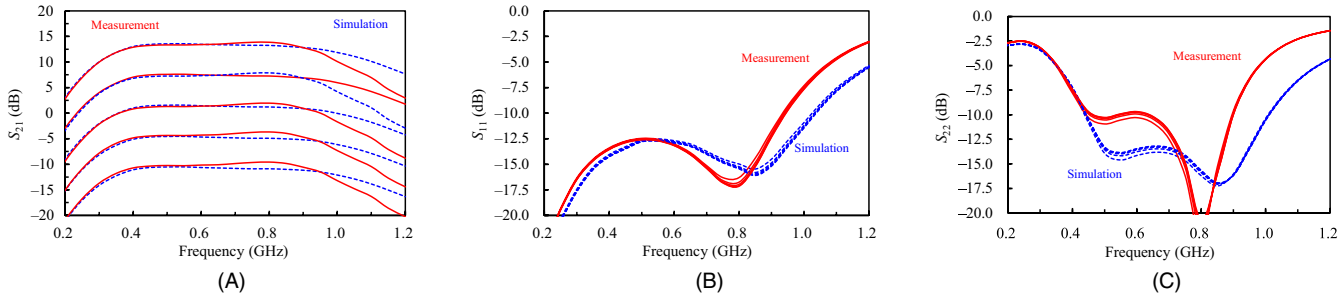


FIGURE 9 Measured and simulated *S*-parameters according to gain change (A) S_{21}, (B) S_{11}, and (C) S_{22}

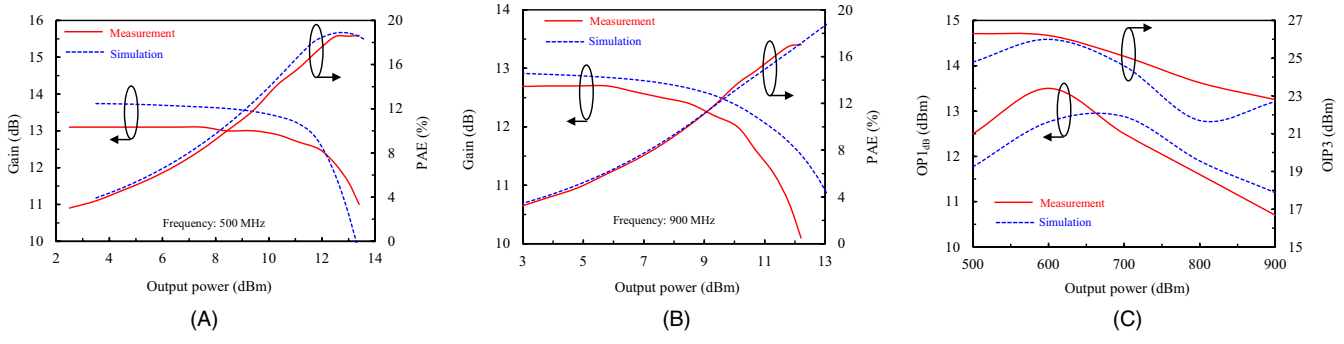


FIGURE 10 Measured and simulated linearity performances: gain and PAE versus output power at an operating frequency of (A) 500 MHz and (B) 900 MHz; (C) OP1dB and OIP3 versus frequency

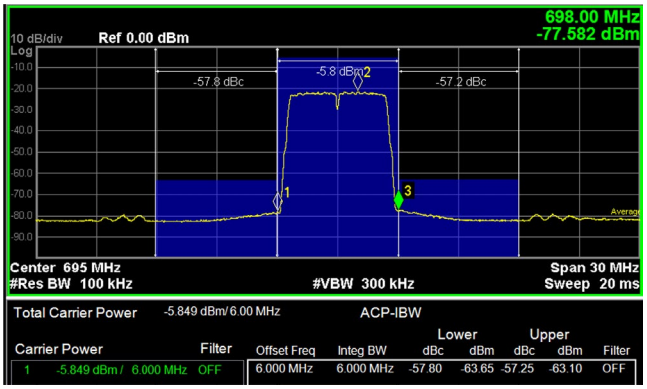


FIGURE 11 Measured channel power and ACLR

powered by a 2 V supply, while other blocks including the bias and digital circuitry were powered by a 1.1 V supply. Each driver amplifier with no input signal drew 24 mA from a 2 V power supply. In all the measurements, the loss of the off-chip networks, such as the transformer and matching networks of the driver amplifier, has been included.

Figure 9 shows the measured and simulated *S*-parameters versus frequency, according to the gain change in a single path. The measured results are in good agreement with the simulation results. We expect that an unwanted parasitic or modeling of external components above 1 Ghz results in an increase in the discrepancy between measurement and simulation. The S_{11} and S_{22} are mostly determined by the off-chip transformers and matching components, which are below −8 dB over 0.4 GHz–0.9 GHz. The maximum value for S_{21} is 14 dB at 0.8 GHz; for the 3 dB bandwidth, ranging from 0.32 GHz to 0.98 GHz, the maximum value is 0.66 GHz. Figure 9A presents the measured gain change versus frequency according to the gain control and exhibits a gain range from −9.4 dB to 14 dB in increments of 6 dB at 0.8 GHz. Figure 10A and 10B show the gain and power-added efficiency (PAE) versus the output power. The measured output P1dB are 12.5 dBm and 10.7 dBm at a frequency of 500 MHz and 900 MHz, respectively. Figure 10C shows the measured output P1dB and 3rd-order intercept point (OIP3) versus frequency. The OIP3 was measured with a 6 MHz frequency offset. The measured output P1dB and OIP3 were over 10.7 dBm and 22.8 dBm, respectively, in the range of 0.5 GHz–0.9 GHz. This indicates an excellent agreement with the simulation results.

The orthogonal frequency-division multiplexing (OFDM)-signal with a 6 MHz bandwidth was applied to the proposed circuit, and the average channel power and ACLR were measured with a spectrum analyzer as shown in Figure 11. The ACLR requirement can be achieved for the channel power of −5 dBm at a frequency of 695 MHz. Furthermore, two modulation signals with a 6 MHz bandwidth were tested to verify the carrier aggregation performance. The driver amplifier can be configured in the carrier aggregation mode

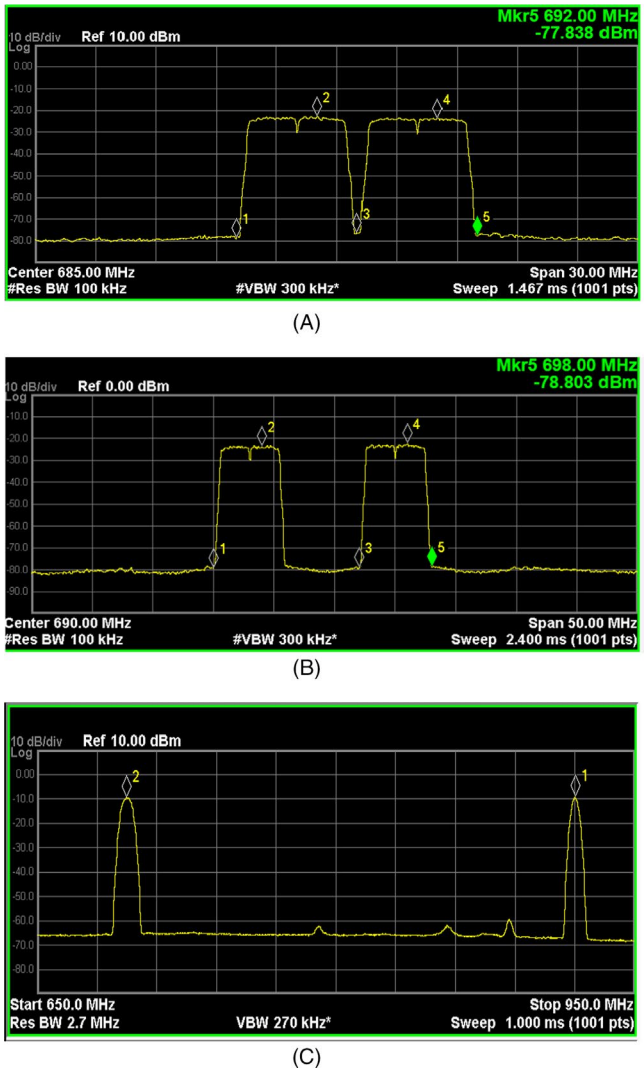


FIGURE 12 Measured (A) contiguous and (B) inter-band (C) intra-band carrier aggregation

by switching on the two paths simultaneously. As shown in Figure 12, the proposed driver amplifier supports (A) contiguous, (B) inter-band, and (C) intra-band carrier aggregations, while maintaining the ACLR performance.

Table 1 compares its performance with that of sub-GHz transmitters. The other references do not satisfy the ACLR requirement of the TV white space spectrum mask. The authors in [11] mentioned that the ACLR can be improved by adding digital predistortion, harmonic cancelation, g_m linearization to attain the required ACLR. Reference [12] describes another design case including a power amplifier and shows a flat error vector magnitude (EVM) response greater than 9 dB to 10 dB back-off owing to the memory effect of the power amplifier. The authors also applied digital predistortion and improved the EVM and ACLR. Without any additional predistortion method, the proposed drive amplifier achieved the highest ACLR performance at both a relatively high output power and low output power.

TABLE 1 Comparison with sub-GHz transmitters

	This work	[10]	[11]	[12]	[16]
Technology (nm)	40	160	65	65	180
Frequency (GHz)	0.5 to 0.9	0.1 to 0.8	0.054 to 0.864	0.054 to 0.864	0.47 to 0.806
OP1dB (dBm)	13.5 to 10.7	9 to 10.8	−8.7 to −1.3	4.3 to 7.8	2.4 to 4.7
OIP3 (dBm)	26.3 to 22.8	18 to 21	5.5 to 8.3	10.6 to 17	14.1 to 21.3
ACLR @MHz offset (dBc)	−55@6 (P_{out} = −5 dBm)	−35@9.14 (P_{out} = 4.6 dBm)	−46@6 (P_{out} = −14 dBm)	−47@6 (P_{out} = −5 dBm)	N/A

4 | CONCLUSIONS

In this paper, we presented a wideband programmable gain driver amplifier for long-range wireless communication, which utilized sub-GHz frequencies supporting the 802.11ah/af standard. The proposed drive amplifier exhibited high linearity by achieving the 55 dBc ACLR requirement. We analyzed the linearity of the amplifier in terms of the bias of the common-gate transistor and provided a design method. By controlling the optimum bias point using the proposed optimum voltage generation circuit, the amplifier provided a 24 dB gain change with a 6 dB step, while maintaining the highest linearity performance. The dual-path amplifier was proposed and designed by combining each output in a current mode. This was tested under an OFDM-modulated signal and the ACLR performance was demonstrated. Moreover, a carrier aggregation to achieve high data-rate transmission was successfully verified by the two independent modulation signals.

FUNDING INFORMATION

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ORCID

Dong-Woo Kang https://orcid.org/0000-0003-4091-3253

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AUTHOR BIOGRAPHIES

Dong-Woo Kang received his BS, MS, and PhD degrees in electrical engineering from Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 2001, 2003, and 2007, respectively. From September 2007 to September 2010, he was a postdoctoral research fellow at the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla. From 2010 to 2013, he worked for Samsung Electronics, Suwon, Rep. of Korea. He is currently working for Electronics and Telecommunications Research Institute. His research interests include CMOS/SiGe ICs for millimeter-wave and terahertz circuit and systems.

Jang-Hong Choi received his BS and MS degrees in electronic engineering from Chonbuk National University, Jeonju, Rep. of Korea, in 1999 and 2001, respectively. Since 2001, he has been with the Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea. His current research interests include radar on chip design, high-speed and low-power analog IC design, and RFIC design for wireless communication.