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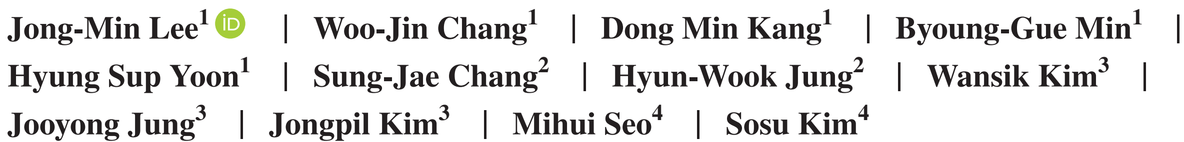
W-Band MMIC chipset in 0.1-μm mHEMT technology



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We developed a 0.1-μm metamorphic high electron mobility transistor and fabricated a W-band monolithic microwave integrated circuit chipset with our in-house technology to verify the performance and usability of the developed technology. The DC characteristics were a drain current density of 747 mA/mm and a maximum transconductance of 1.354 S/mm; the RF characteristics were a cutoff frequency of 210 GHz and a maximum oscillation frequency of 252 GHz. A frequency multiplier was developed to increase the frequency of the input signal. The fabricated multiplier showed high output values (more than 0 dBm) in the 94 GHz–108 GHz band and achieved excellent spurious suppression. A low-noise amplifier (LNA) with a four-stage single-ended architecture using a common-source stage was also developed. This LNA achieved a gain of 20 dB in a band between 83 GHz and 110 GHz and a noise figure lower than 3.8 dB with a frequency of 94 GHz. A W-band image-rejection mixer (IRM) with an external off-chip coupler was also designed. The IRM provided a conversion gain of 13 dB–17 dB for RF frequencies of 80 GHz–110 GHz and image-rejection ratios of 17 dB–19 dB for RF frequencies of 93 GHz–100 GHz.

KEYWORDS
frequency multiplier, image-rejection mixer, LNA, mHEMT, MMIC

1 | INTRODUCTION

Recently, interest in chips and systems operating in the millimeter-wave or sub-millimeter-wave bands, such as radars, seekers, spectrometers, and future giga-class mobile communication technologies, has increased [1,2]. In particular, high-frequency bands are required to supply the demand for ultra-high-speed and broadband communication services due to the explosive increase in information. Therefore, various semiconductor technologies that implement future information and communication and high-tech sensors will be the most important growth engines in the future, thus attracting increasing interest from research institutes worldwide. This interest has increased the importance of national technology development and technology protection, especially technologies that can reliably produce stable electronic devices that operate at higher frequencies. ETRI has been making efforts to develop its own semiconductor processing technology for this purpose. In concert with these efforts, we have been researching metamorphic high electron mobility transistor (mHEMT) technology for many years and have achieved the development of mHEMT technology with 0.15-μm length, and published the performance verification of a 77 GHz monolithic microwave integrated circuit (MMIC) using the developed technology [3,4]. This paper is intended to report on the results of the subsequent research, the development of mHEMT technology

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with 0.1-μm gate length, and the performance verification of a 94 GHz MMIC using the developed technology. In this paper, we summarized the characteristics of ETRI's own mHEMT device with a 0.1-μm gate length and the design and results of the MMIC using it. Based on the verification results, we will proceed to the next phase, the mHEMT processing technology with a gate length of 50 nm for millimeter-wave and terahertz applications. To implement a W-band system, it is necessary to develop a transceiver operating in W-band. First, it is necessary to develop an MMIC with excellent characteristics, making the system compact, lightweight, highly reliable, and enabling its mass production at low cost. Among the many electronic devices, the high electron mobility transistor (HEMT) device is attracting attention as a key alternative component in the development of W-band MMIC devices, due to its low noise and excellent ultra-high-frequency characteristics. Recently, the frequency characteristics of complementary metal-oxide semiconductor (CMOS) devices have continuously improved, and several MMIC results using CMOS technology operating in W-band have been published [5–9]. MMIC using CMOS has the advantages of low price and high integration, as compared to competitive semiconductor technologies. Although there are advantages of the CMOS technology, HEMT also has the advantages of high mobility, large breakdown voltage, and the implementation of high quality-factor passives. Thus, it is considered that the two technologies will continue to compete in the future. Having a metamorphic buffer layer and an indium phosphide (InP) epitaxial layer on a gallium arsenide (GaAs) substrate, mHEMT imparts additional advantages to each device such as excellent device characteristics, due to InP, and ease of processing due to GaAs. Recently, many reports on MMIC using mHMET have been reported, and foundry services, in which the mHEMT technology is used, have been conducted [10–13]. In this paper, we show the characteristics of a 0.1-μm mHEMT device manufactured by ETRI in-house mHEMT process with a 4-inch wafer. In addition, we verified the developed process by the successful development of an MMIC chipset, which is composed of a frequency multiplier, low-noise amplifier (LNA), and image-rejection mixer (IRM).

1.1 | 0.1-μm mHEMT technology

The epitaxial structure of the wafer used in the GaAs-based mHEMT for the W-band MMIC fabrication was established with a molecular beam epitaxy (MBE) method and a semi-insulating GaAs substrate. A cross section of the mHEMT epitaxial structure is shown in Figure 1. Graded and epitaxial-InAlA buffer layers were established on the substrate to form a matched state with the high-concentration-InGaA channel layer, preventing potential defects from propagating to the channel layer of the device. Considering the lattice matching with the buffer layers, an indium composition ratio of 0.53 is suitable; however, as the concentration of InAs and, therefore, the mobility of the channel layer increases, the suitable composition of indium is changed to 0.6. The structure of the wafer is composed of InAlA spacer, planar doping, InAlA Schottky, and InGaA cap layers over the channel layer. The fabrication of the mHEMT device was first performed using a phosphoric acid-based etching solution to electrically separate the mHEMT devices. Afterward, source and drain ohmic electrodes, composed of Au/Ge/Ni/Ti/Au with thicknesses of 340/170/115/115/1200 Å, respectively, were simultaneously deposited. The electrode deposition conditions were optimized by considering the surface roughness and contact resistance of the electrode after heat treatment. In order to improve the speed of the device, the gate must be shortened; therefore, a gate pattern with length 100 nm for forming its electrode is designed using an electron beam exposure method. A recess process was performed to control the threshold voltage of the device

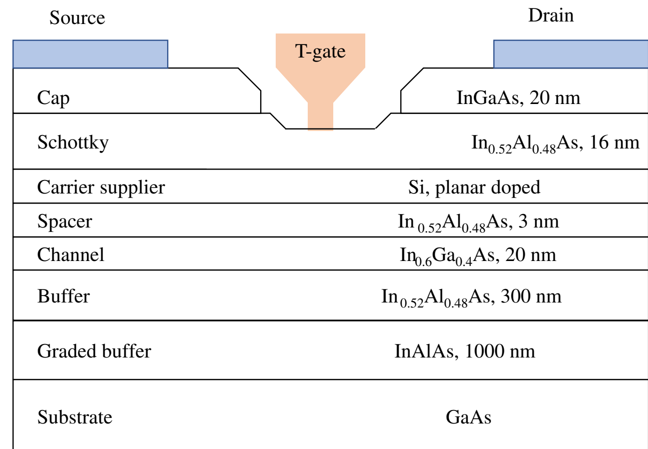


FIGURE 1 Schematic of the cross section of an mHEMT epitaxial structure

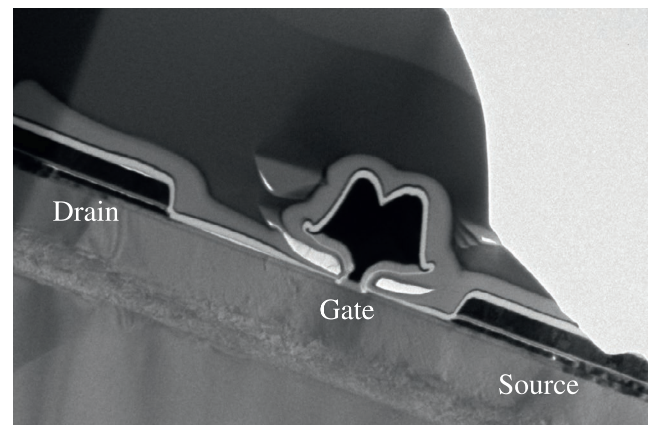


FIGURE 2 Cross-sectional photograph of a 0.1-μm mHEMT with a T-shaped gate structure

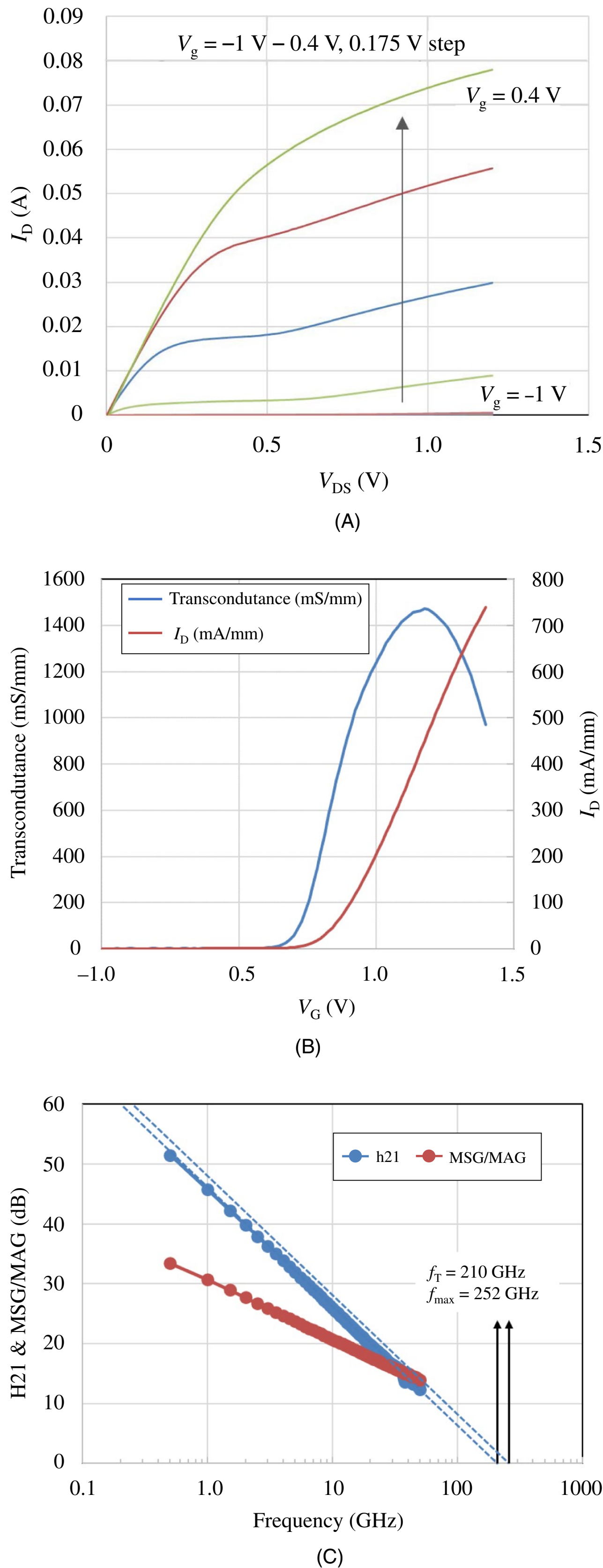


FIGURE 3 (A) Current-voltage curve, (B) transconductance curve, and (C) RF performance of 0.1-μm mHEMT

TABLE 1 Electrical DC & RF parameters of the 0.1-μm mHEMT

Parameter	Value
I_D, max (mA/mm)	740
G_m, max (S/mm)	1.471
V_{BD} (V)	3
f_T (GHz)	210
f_{max} (GHz)	252

and to improve its transconductance. After patterning the gate region to be etched first, a GaA cap layer and an InAlA Schottky layer were etched using succinic acid and citric acid-based etchants. In the recess process, it is necessary to prevent an increase in the gate length during the etching and depth adjustment procedures of the recess. In this study, the concentration and etching time of the etchant were optimized through several experiments to achieve a reproducible recess process. From the cross-sectional photograph of the device (Figure 2), the gate pattern was extended, and the length at which the gate electrode was deposited was approximately 130 nm. A three-layer photosensitive film structure with different photosensitivity was used to generate a reproducible T-type gate structure. Afterward, Ti/Au materials were deposited at a thickness of 500/4000 Å, respectively, using a vacuum deposition equipment and lifted off to form a gate electrode. To protect the device, a SiN_x insulating film of 50 nm in thickness was also deposited. Figure 2 shows a cross-sectional photograph of a device composed of a T-shaped gate structure. Among the device parameters, which were different for each device, the parameters of the standard device were: gate size of 2 μm × 50 μm (2f100), distance between the source and drain electrodes of 2 μm, and distance between the source and gate electrodes of 0.5 μm. The resistor for the fabrication of the MMIC was made of NiCr metal using a vacuum evaporator. The metal for wiring was connected to both sides of the NiCr resistor, enabling the connection of other devices in the MMIC. The width of the resistor metal was 10 μm and the deposited thickness was 60 nm. A metal-insulator-metal structure, in which a SiN_x passivation layer is disposed between the lower electrode and the upper electrode, was used to manufacture the capacitor. SiN_x with a thickness of 50 nm was deposited to protect the mHEMT device. After the front process was completed, the wafer thickness was reduced to 100 μm, and a backside for grounding the device was formed. Direct current (DC) and radio frequency (RF) characteristics were measured using a Cascade on-wafer probe station in the wafer state, to evaluate the characteristics of the manufactured mHEMT device. The output characteristics of a typical mHEMT are presented in Figure 3. The DC characteristics were measured while the voltage of a Keysight HP4142

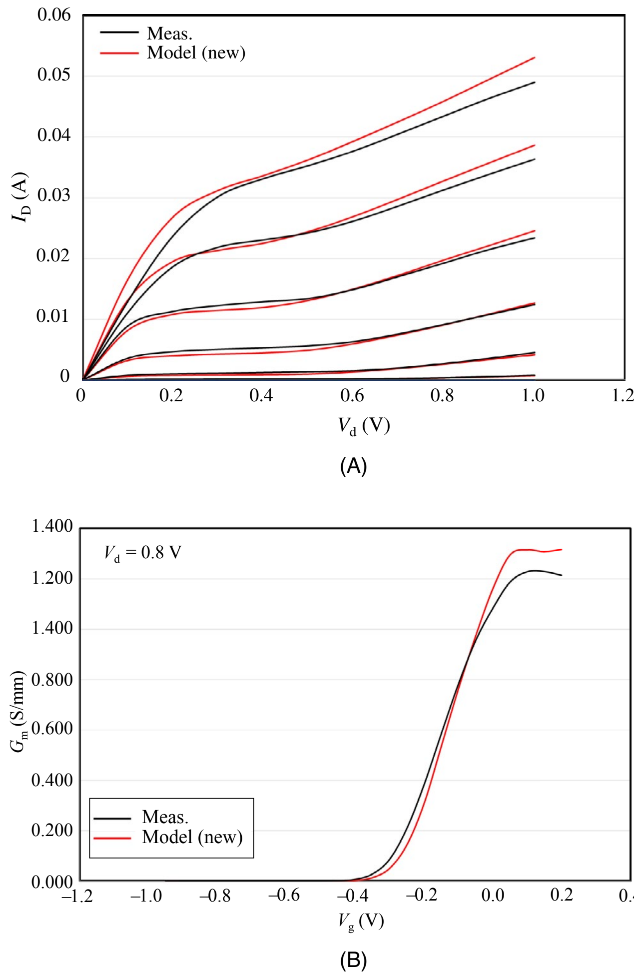


FIGURE 4 Comparison of the measured (black line) and calculated (red line) DC characteristics for mHEMT: (A) current-voltage curve and (B) transconductance curve

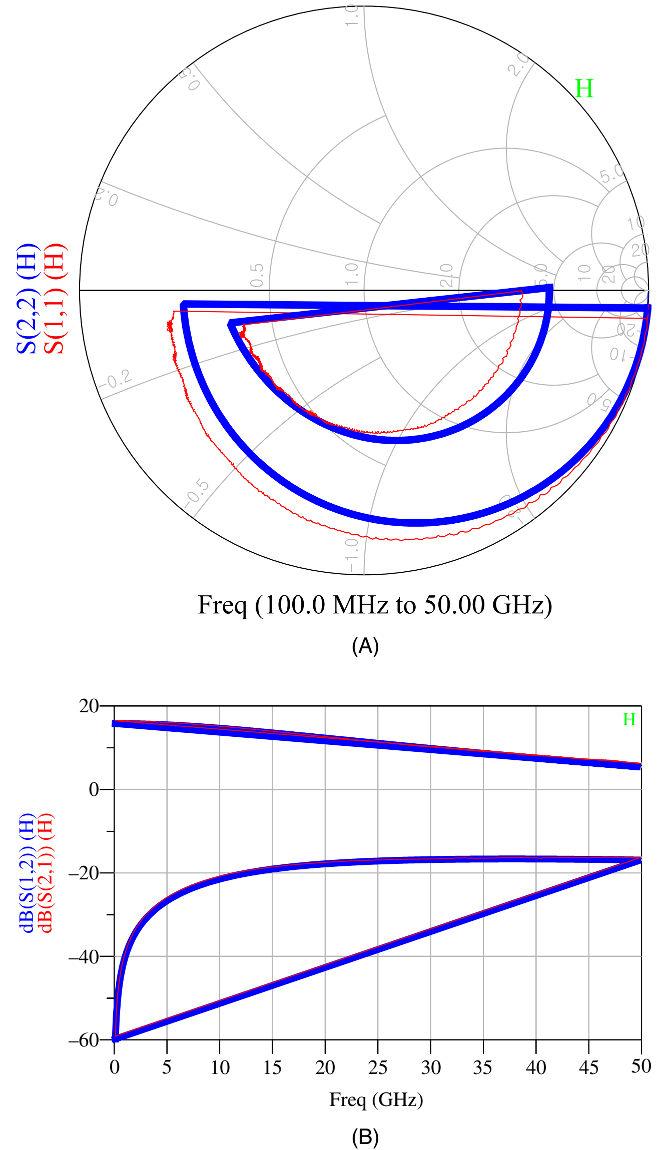


FIGURE 5 Comparison of the measured (red line) and calculated (blue line) RF characteristics for mHEMT: (A) reflection and (B) transmission

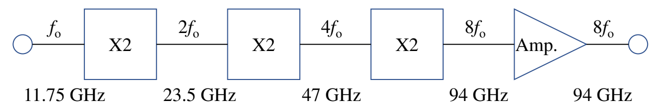


FIGURE 6 Block diagram of the MMIC multiplier

power supply varied. The drain current (I_D) was obtained when the drain voltage (V_D) changed from 0 V to 1.2 V and the gate voltage (V_G) changed from –1 V to 0.4 V in steps of 0.175 V. From this procedure, the mHEMT device showed good pinch-off performance, and exhibited a leakage current of 34 μA and a maximum drain saturation current value of 74 mA when the V_G values were –1 V and 0.4 V, respectively. To measure the transconductance of the device, V_D was fixed at 1 V while V_G changed from –1 V to 0.4 V. As a result, an excellent maximum transconductance of 1.471 S/mm was obtained when V_G = 0.176 V. The manufactured mHEMT S-parameter was measured using a Keysight N5245A microwave network analyzer. The measurement frequency range was 0.5 GHz–50 GHz, and the bias conditions were V_D = 1.0 V and V_G = 0.1 V. Figure 3 also shows the RF characteristics of mHEMT with a 2 μm × 50 μm gate, the current gain (h21), and the MSG/MAG curve determined from the measured S-parameter values. The current gain cutoff frequency (f_T) and the maximum resonant frequency (f_{max}) obtained by extrapolating the curves with a linear relation (slope of –20 dB/decade) were 210 GHz and 252 GHz, respectively. The electrical DC and RF device parameters are listed in Table. 1. We used the results of active and passive devices manufactured by a 0.1-μm mHEMT processing technology developed to design MMIC. For the MMIC design, mHEMT device modeling was performed with measured values while changing the bias and frequency, and a passive device model was produced by comparing the measured value with electromagnetic simulations. Figures 4

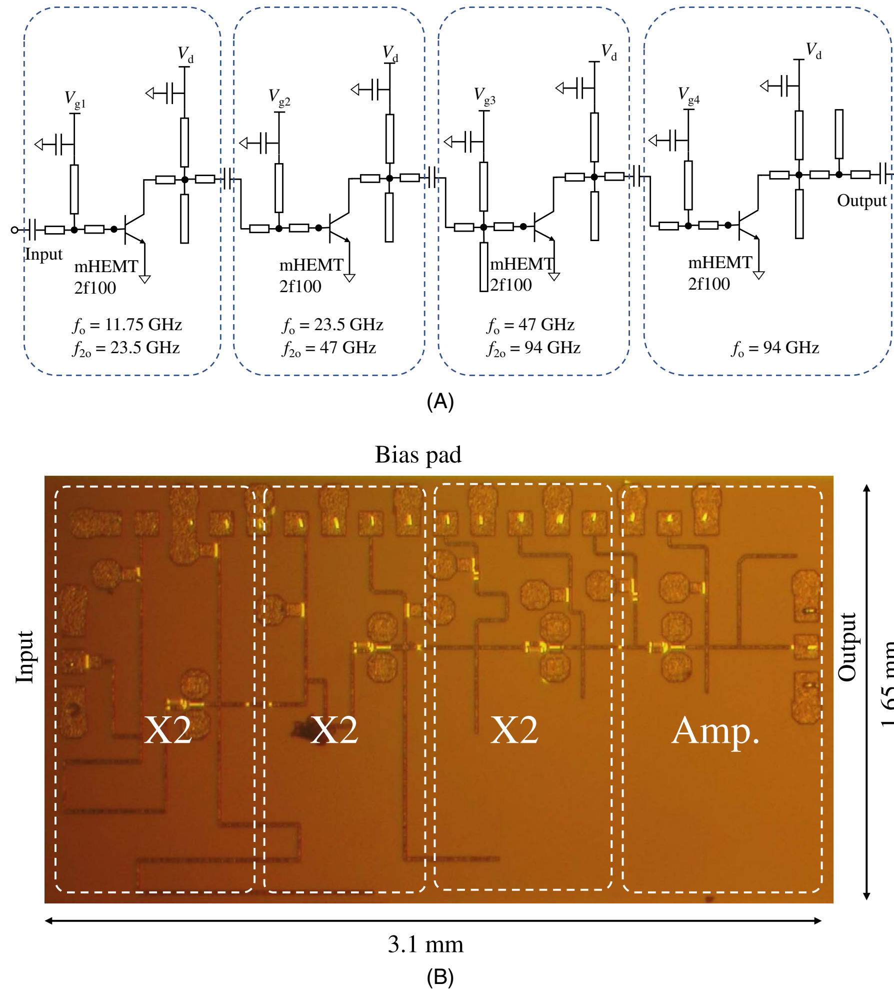


FIGURE 7 Circuit schematic and photograph of MMIC: (A) circuit of the frequency multiplier MMIC and (B) Photograph of the frequency multiplier MMIC

and 5 show the results of comparing the measured values of DC and RF characteristics with those calculated from the extracted model, respectively.

2 | MMIC CHIPSET

2.1 | Frequency multiplier

In the transceiver, the signal generating circuit is used as a local oscillator and a signal source. As the operating frequency of the circuit increases, the design of the frequency generator becomes complex and difficult to implement. In the millimeter-wave and sub-millimeter-wave frequency regime, signal generation is usually implemented using the frequency multiplication technique [7,8], in which an additional low frequency signal source is required. One advantage is the possibility of using a signal source that precisely operates at low frequencies; therefore, it is used when a precise signal source frequency setting is required in a high-frequency band. Figure 6 shows a four-block diagram of the designed active frequency multiplier. The first three blocks are responsible for doubling the frequency, converting an 11.75 GHz frequency input into a 94 GHz signal, which is amplified by the successive amplifier. Figure 7 shows a scheme of the designed frequency multipliers. The active device has a gate size of 2 μm × 50 μm, and a parallel configuration of a resistor and capacitor is adopted to stabilize the stages of the multiplier. The input and output matching networks of each stages were both set to 50 Ω at the input and output frequencies, respectively. Furthermore, the output matching network is also designed to block unwanted harmonics. For the suppression of fundamental signals at each block stage, a shunt open stub was added. The 94 GHz amplifier with common source topology was designed to achieve sufficient output power and gain. Three doubler stages were designed to operate in the region near the pinch-off, and the last stage was designed to operate in the class A region to increase the gain. The performance of the MMIC multiplier was measured while it was on the wafer and when it was connected to a 50-Ω environment. The measurement was performed using an Anritsu MS4647A 110GHz network analyzer. Figure 8 shows the comparison of

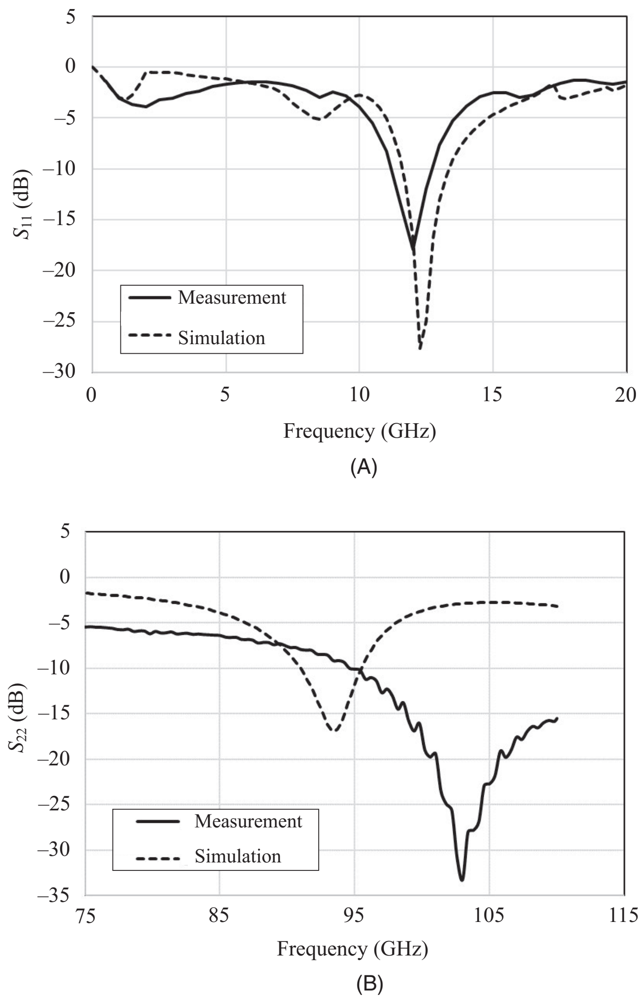


FIGURE 8 Small-signal return loss: (A) input return loss (S_{11}) and (B) output return loss (S_{22})

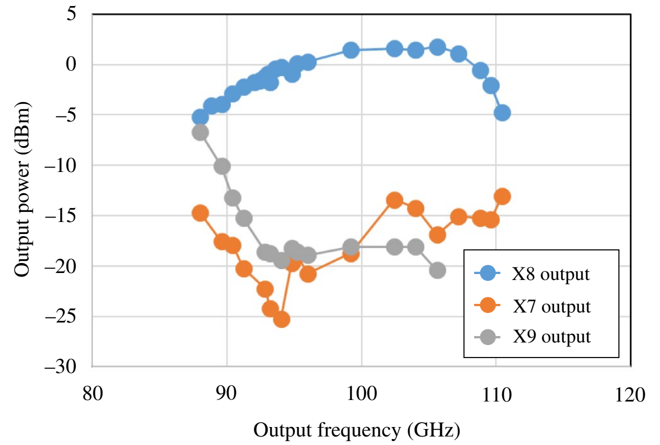


FIGURE 9 Output power versus output frequency of the frequency multiplier with input power of 0 dBm

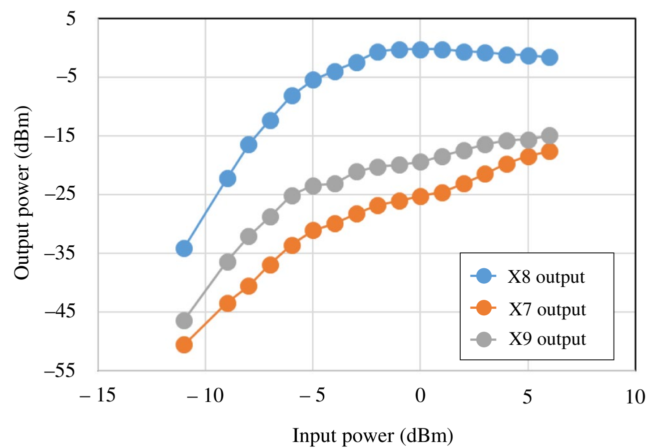


FIGURE 10 Measured output power versus the input power at the input frequency of 11.75 GHz

the multiplier for the simulated and measured port matching performance. The measured input matching showed sufficient matching characteristics of input return loss (S_{11}) lower than −10 dB at the input frequency, which was consistent with the simulation results. The output matching achieved a performance of approximately –10 dB at 94 GHz; however, the frequency when output return loss (S_{22}) is minimum upward shifted from the actual target (94 GHz) to 103 GHz and broad matching frequency ranges were obtained. The discrepancy between the simulation and measurement occurred due to the inaccuracy of the transistor model and EM simulation. An Agilent 83650B signal generator was used to drive the MMIC. Unwanted signal output frequencies occurred between 75 GHz and 110 GHz and their power levels were measured with an Agilent 8565E spectrum analyzer and a HP11970W sub-harmonic W-band mixer. To calibrate the equipment, a HP83558A mm-wave signal source module was connected to the mixer using different configurations (waveguide and on-wafer) and the loss in the RF probe tip was determined. The measured output power was obtained as a function of the frequencies (from 88 GHz to 111 GHz). The spurious suppression, for a constant input power level of 0 dBm, is shown in Figure 9. When the frequency ranged from 94 GHz to 108 GHz, the output power was flat and above 0 dBm. The peak output power (2 dBm) occurred at 105 GHz. The spurious suppression is lower than –15 dBc from 92 GHz to 108 GHz. Figure 10 shows the measured output power and conversion gain at 94 GHz as the input power increases from –11 dBm to 6 dBm. The maximum output power of 1.8 dBm was obtained. Table 2 presents the results of this work compared with other multipliers.

2.2 | Low-noise amplifier

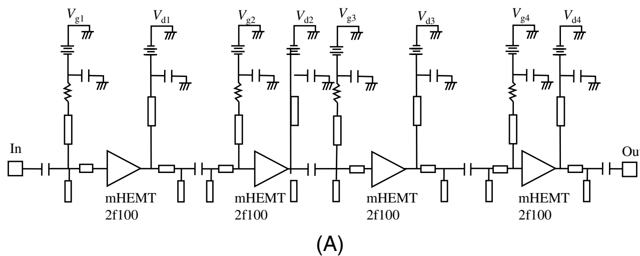
The MMIC low-noise amplifier (LNA) was a four-stage single-ended type of LNA. This architecture was combined with a common-source stage and was chosen due to its low-noise figure and moderate gain. At millimeter wavelength,

TABLE 2 Comparison of the W-band multiplier

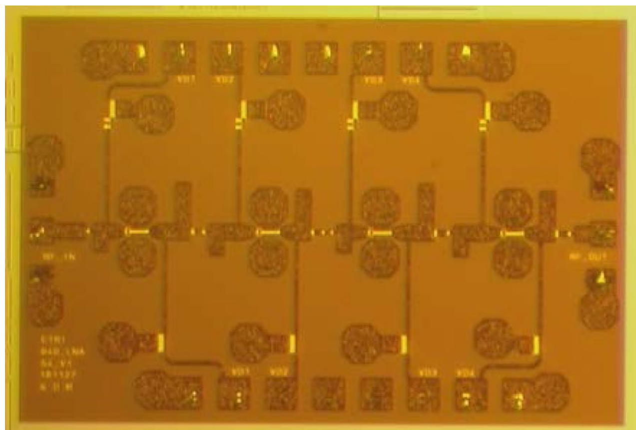
Technology	Freq. (GHz)	Type	Pout (dBm)	HS* (dBc)	P_DC (mW)	Ref.
0.1-μm mHEMT	85–100	×12	1	30	286	[12]
0.15-μm mHEMT	72–114	×6	N/A	40	120	[13]
0.1-μm HEMT	82–102	×9	–6.4	23	99	[14]
0.1-μm mHEMT	92–108	×8	1.8	15	50	This work

*HS, harmonic suppression.

mHEMTs composed of more than four fingers and unit finger width larger than 50 μm, are very difficult to match to 50 Ω since input and output optimum terminations are featured by very low impedance levels. Moreover, multiple finger devices exhibit a decrease in the cut-off frequency caused by parasitic effects. We choose a 2 finger HEMT with 50-μm unit finger width for MMIC. The size of the mHEMT used was equal to that in 77 GHz MMIC. All input/output matching, inter-stage matching, and biasing networks were included in the MMIC design. In each stage of the MMIC, a microstrip line, an open stub, and a capacitor were connected between the HEMT and an input/output node to achieve enough return loss and rejection characteristic in the undesired frequency bandwidth. To achieve a small chip size, short series microstrip elements were used with the shunt open stubs, which produced compact matching circuits. All grounded parts of the LNA were processed via holes, whose front and backside dimensions were 80 μm and 120 μm, respectively. In the case of a low-noise amplifier, the input matching circuit is the most important matching circuit in determining the noise figure, so it must be designed to have the best low-noise matching characteristics. The source impedance (Γ_S) and load impedance (Γ_L) are as shown in (1) and (2):

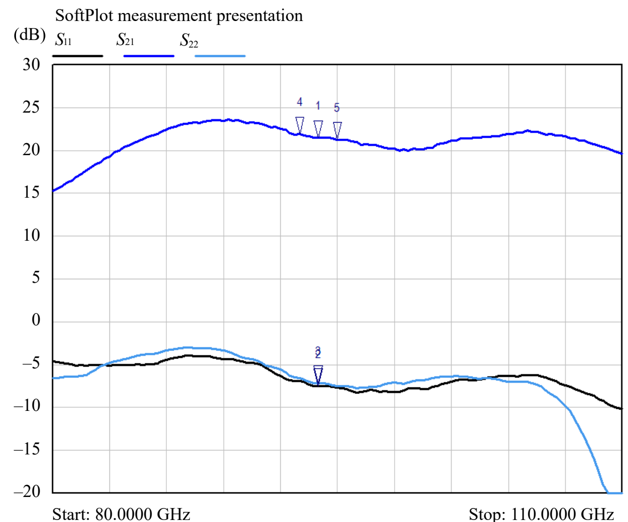


(A)

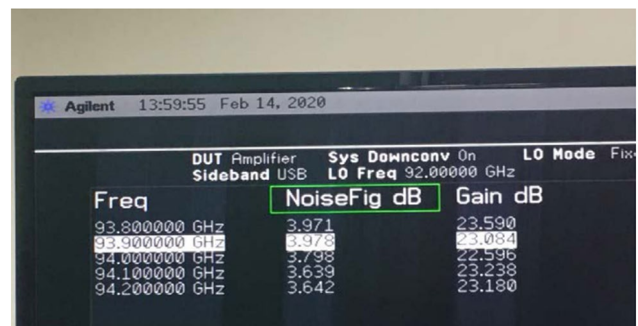


(B)

FIGURE 11 Circuit scheme and photograph of the single-ended MMIC low-noise amplifier: (A) circuit scheme of the MMIC LNA and (B) photograph of MMIC LNA



(A)



(B)

FIGURE 12 Measured results of the single-ended MMIC LNA: (A) small signal gain (S_{21}), input return loss (S_{11}), and output return loss (S_{22}) as a function of frequency (80 GHz–110 GHz) for the fabricated MMIC LNA and (B) noise figure as a function of frequency (94 GHz) for the fabricated MMIC LNA

TABLE 3 Comparison of the data of previously published W-band LNAs with this work

Technology	Freq (GHz)	Gain (dB)	NF (dB)	Size (mm^2)	P_DC (mW)	Ref.
0.05-μm mHEMT	97–164	30.8	3.4	2.0 × 0.75	57.6	[15]
0.10-μm mHEMT	97–155	23	4.7	N/A	31.5	[15]
90-nm BiCMOS	122–150	30	6.2	0.7 × 0.75	45	[16]
0.1-μm GaN HEMT	82–86	25	3.8	1.0 × 2.5	800	[17]
0.1-μm mHEMT	83–110	23	3.8	2 × 1.2	50	This work

$$\Gamma_S = \Gamma_{in}\left(\text{conjugate of } S_{11}\right),$$

$$\Gamma_S = \Gamma_{opt}\ (\text{optimal noise source impedance}), \quad (1)$$

$$\Gamma_S = \left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}\right), \ \Gamma_L = \left(S_{22} + \frac{S_{12}S_{21}\Gamma_{opt}}{1 - S_{11}\Gamma_{opt}}\right). \quad (2)$$

For input terminal matching, a matching circuit is constructed by setting appropriate trade off points for gain (Γ_{in}^*) and noise (Γ_{opt}) in the available power gain circle and optimum reflection coefficient for noise match. However, in this low-noise amplifier design, an input matching circuit was constructed to match the input-stage reflection coefficient, which has the best noise figure, although there is a slight loss in gain and input reflection characteristics.

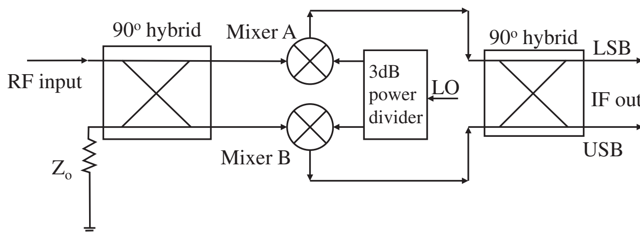


FIGURE 13 Block diagram of the designed W-band IRM

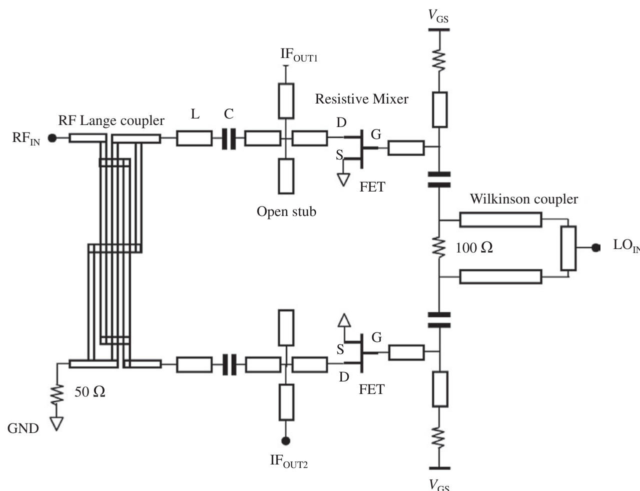


FIGURE 14 Schematic of the designed W-band IRM

In addition, to achieve the minimum noise figure, the first stage was designed to operate in the region near the pinch-off, and the other stage was designed to operate in the class A region to increase the gain. A microstrip thin film capacitor provided in the ETRI library was applied to the DC-block circuits to isolate the stages and to combine the RF signals. The bias networks consisted of high impedance transmission lines, with decoupling capacitors acting as RF short circuits. Furthermore, the gate bias circuits were designed using a 42-Ω NiCr resistor, generating a low gain flatness at the operating frequency. The LNA was also designed to operate at approximately half of the drain saturation current to achieve a minimum noise figure. The on-wafer measurement was performed using a HP PNA N5250A 110 GHz network analyzer. The circuit scheme and photographs of the fabricated single-ended LNA type, which achieved a gain of 20 dB at frequencies between 83 GHz and 110 GHz and a noise figure of lower

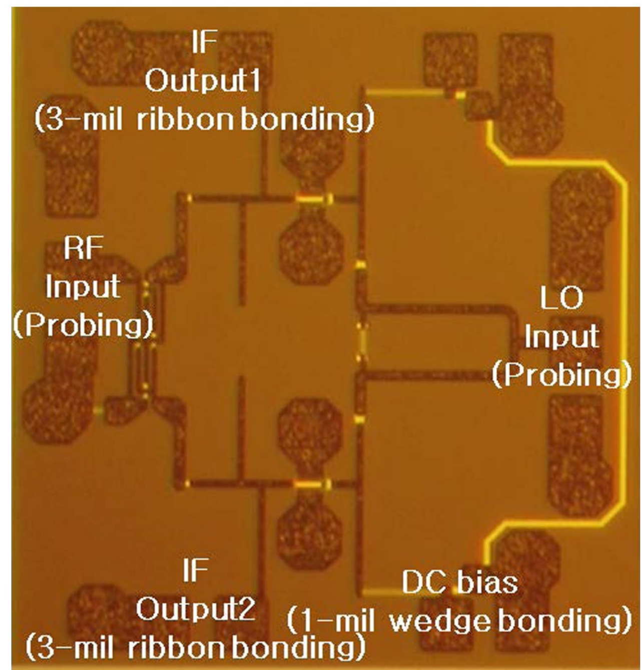
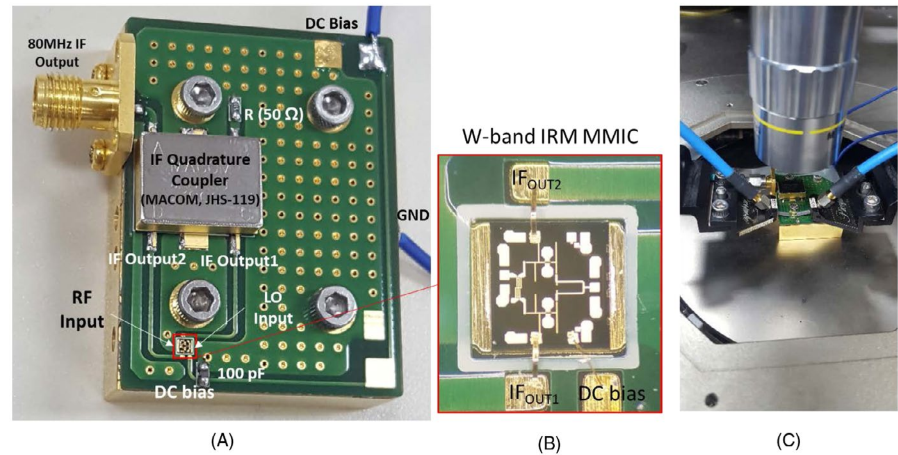
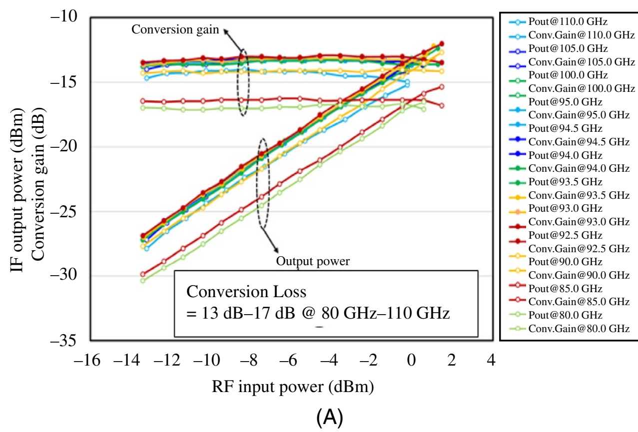


FIGURE 15 Photographic view of the fabricated W-band IRM in ETRI's 0.1-μm mHEMT process

FIGURE 16 W-band IRM with the external IF hybrid coupler on a printed circuit board



than 3.8 dB at 94 GHz, are presented in Figure 11. The external DC biasing conditions of VD and VG were 1 V and –0.1 V, respectively; the total current consumption of the LNA was 50 mA, and the manufactured chip size was 2 mm × 1.2 mm. Furthermore, the results of the fabricated single-ended LNA are presented in Figure 12. Moreover, the LNA results that have been recently obtained, at 94 GHz, by other studies are shown and compared with those obtained in this work in Table 3.



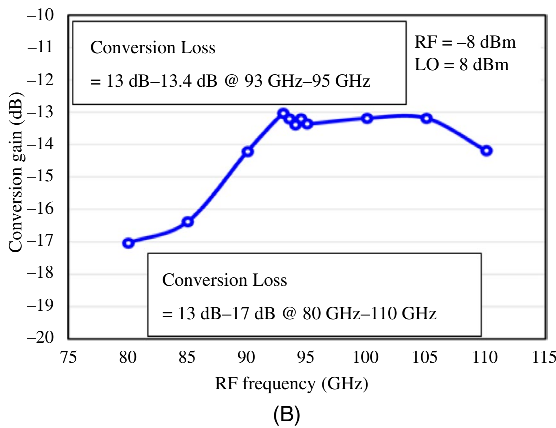
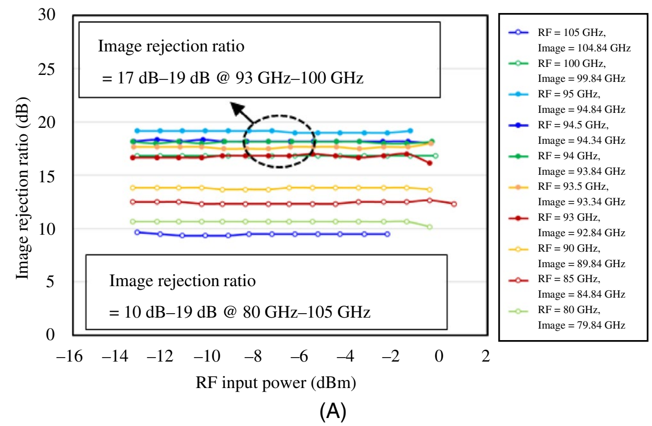


FIGURE 17 Measured results of conversion gain and IF output power for the fabricated W-band IRM: (A) IF output power and conversion gain of W-band IRM for RF input power and (B) conversion gain of W-band IRM for RF frequency at an RF power of −8 dBm and an LO power of 8 dBm



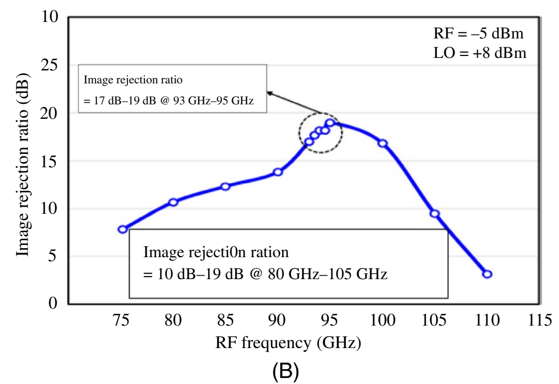


FIGURE 18 Measured results of image-rejection behavior for the fabricated W-band IRM: (A) image-rejection behavior of W-band IRM for RF input power and (B) image-rejection behavior of W-band IRM for RF frequency at an RF power of –5 dBm and an LO power of 8 dBm

TABLE 4 Comparison with other IRMs

Technology	RF (GHz)	LO (GHz)	LO power (dBm)	Conv. loss (dB)	Image-rejection (dB)	Ref.
0.15-μm GaAs mHEMT	71–76 81–86	70–90	4	9	25	[18]
0.15-μm GaAs pHEMT	90–112	85–105	9.4–11.3	10.8	10–29.2	[20]
GaAs mHEMT-based Diode	91.5	94	N/A	15	20	[21]
0.1-μm GaAs mHEMT	90–100	89.92–99.92	8	13–14	13–19	This work

2.3 | Image-rejection mixer

A W-band image-rejection mixer (IRM) consists of two resistive mixers, an RF Lange coupler, an LO Wilkinson power divider, and an external off-chip IF 90-degree hybrid coupler, as shown in Figure 13. Moreover, Figure 14 shows a schematic of the designed IMR. The selected resistive mixer exhibited low flicker noise and current consumption. Furthermore, its circuit structure was a simple circuit, as no drain bias is required by the HEMTs presented in the resistive mixer [18–21]. In the designed W-band IRM, the RF signal is decomposed by the RF Lange coupler into two 90-degree out-of-phase signals, which were simultaneously converted into two IF signals by a pair of resistive mixers that used in-phase LO signals inputted by the Wilkinson coupler. The external off-chip IF 90-degree hybrid coupler was used to combine and, thereafter, separate both IF signals into the desired signal and its image, which were sent through two IF output ports of the external IF hybrid coupler. Microstrip lines, two open stubs, and metal-insulator-metal capacitors were used to match the circuits, DC blocks, and RF decoupling elements. Two mHEMTs with two gate fingers, and a gate size of 0.1 μm × 100 μm were used in the design. Figure 15 shows the fabricated W-band IRM MMIC (1.15 mm × 1.19 mm) in the mHEMT process of the ETRI. The fabricated W-band IRM MMIC with the external IF hybrid coupler, was attached on a printed circuit board, as shown in Figure 16. The equipment was attached using an Ag-epoxy and was wired with a 3-mil ribbon bonding and a 1-mil wedge bonding for IF pads and DC bias pads, respectively. The power measurement of this equipment was performed with two signal generators and a spectrum analyzer. The RF and LO signals were fed through RF probes. The gate bias to the IRM was set to –0.2 V. The conversion losses ranged from 13 dB to 13.4 dB for RF frequencies of 93 GHz–95 GHz, LO frequencies of 92.92GHz–94.92 GHz, and an IF frequency of 80 MHz. The measured conversion losses were 13 dB–17 dB for RF frequencies of 80 GHz–110 GHz, LO frequencies of 79.92 GHz–109.92 GHz, and an IF frequency of 80 MHz, as shown in Figure 17. Figure 18 presents the measured results of the image-rejection behavior of the W-band IRM. The measured image-rejection ratios were 17 dB–19 dB for RF frequencies of 93 GHz–100 GHz, RF image frequencies of 92.84 GHz–99.84 GHz, LO frequencies of 92.92 GHz–99.92 GHz, and an IF frequency of 80 MHz. The measured image-rejection ratios were 10 dB–19 dB for RF frequencies of 80 GHz–105 GHz, RF image frequencies of 79.84 GHz–104.84 GHz, LO frequencies of 79.92 GHz–104.92 GHz, and an IF frequency of 80 MHz. Table 4 presents the results of this work compared with other IRMs.

3 | CONCLUSION

The development of an MMIC chipset using ETRI 0.1-μm mHEMT technology on a 4-in 100-μm-thick GaA substrate was described. In this paper, we report on the results of the development of an in-house mHEMT technology with a gate length of 0.1 μm, and the performance of a W-band MMIC to support the technology. It was demonstrated that the developed technology exhibited sufficient performance to manufacture W-band MMIC. The MMIC chipset, composed of a frequency multiplier, an LNA, and an image-rejection mixer, possessed suitable characteristics, enabling it to be used as a transceiver component for millimeter-wave system applications. Measurements on all circuits confirm the feasibility of the mHEMT technologies in W-band applications.

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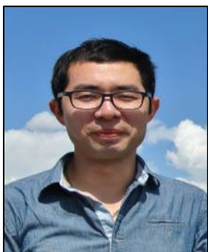

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