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8.2-GHz band radar RFICs for an 8 × 8 phased-array FMCW receiver developed with 65-nm CMOS technology

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We propose 8.2-GHz band radar RFICs for an 8 × 8 phased-array frequency-modulated continuous-wave receiver developed using 65-nm CMOS technology. This receiver panel is constructed using a multichip solution comprising fabricated 2 × 2 low-noise amplifier phase-shifter (LNA-PS) chips and a 4ch RX front-end chip. The LNA-PS chip has a novel phase-shifter circuit for low-voltage operation, novel active single-to-differential/differential-to-single circuits, and a current-mode combiner to utilize a small area. The LNA-PS chip shows a power gain range of 5 dB to 20 dB per channel with gain control and a single-channel NF of 6.4 dB at maximum gain. The measured result of the chip shows 6-bit phase states with a 0.35° RMS phase error. The input P1 dB of the chip is approximately –27.5 dBm at high gain and is enough to cover the highest input power from the TX-to-RX leakage in the radar system. The gain range of the 4ch RX front-end chip is 9 dB to 30 dB per channel. The LNA-PS chip consumes 82 mA, and the 4ch RX front-end chip consumes 97 mA from a 1.2 V supply voltage. The chip sizes of the 2 × 2 LNA-PS and the 4ch RX front end are 2.39 mm × 1.3 mm and 2.42 mm × 1.62 mm, respectively.

KEYWORDS
FMCW, phased array, phase shifter, radar, receiver

1 | 1 INTRODUCTION

The increasing popularity of unmanned aerial vehicles (UAVs), such as consumer drones, has given rise to many potential security threats; thus, it has become essential to develop countermeasures, such as a drone detection radar [1]. The radar system, which consists of an antenna, RF transceiver, signal processing and control unit, system power supply, and cooling part, should have a small size to be commercially successful. However, the development of a small radar detection system is challenging because the radar must be able to detect a drone with a radar cross section (RCS) as small as –20 dBsm, at a distance of a few kilometers [2,3].

A frequency-modulated continuous-wave (FMCW) radar emits a continuous-wave (CW) signal that is frequency-modulated. The required peak-transmit power is reduced for a given detection range compared with a pulsed radar, which has a high peak output power. Therefore, the transmitter of the FMCW radar can use power amplifiers with less saturation power than that of pulsed radar, while consuming less total power. Moreover, the signal processing required in the FMCW radar to obtain the range and velocity is performed by a fast Fourier transform (FFT) at a relatively low operating frequency, considerably simplifying the realization of the processing circuit. However, the FMCW radar requires a high isolation characteristic

between the transmitter and receiver for long-range coverage. Generally, the more power the transmitter emits, the more the isolation is required in the system to prevent receiver saturation [4–6].

The phased-array radar has the features of high antenna gain and fine-resolution beam steering, which enable long-range target detection coverage. For the architecture of such a phased-array radar, phase shifting in the RF domain has been predominantly used because of its advantages such as high pattern directivity of the beam and a simpler design compared with designs that employ local oscillators (LOs) or intermediate frequency (IF) phase shifting [7–9]. Digital beamforming in the radar for a large array size and small form factor is not suitable because of its high hardware complexity.

In this paper, we propose two receiver integrated circuits (ICs) for the FMCW radar structure to detect small drones with an RCS of −20 dBsm, while providing a maximum detection range of 1 km. Section 2 of this paper describes the specifications of the radar system, the radar structure, and the proposed structures of the two chip components. Circuit-level descriptions of the building blocks are presented in Section 3. Experimental results are discussed and summarized in Section 4.

2 | SPECIFICATION AND STRUCTURE

We referred to [10] to derive the design target parameters for small UAV detection. Table 1 briefly shows the design targets and specifications proposed for this work. The specification results are derived from the radar (1) to satisfy the target design parameters:

$$\mathrm{SNR} = \frac{P_{\mathrm{CW}} \bullet T_{\mathrm{Dwell}} \bullet G_{\mathrm{T}} \bullet G_{\mathrm{R}} \bullet \lambda^2 \bullet \sigma}{(4\pi)^3 \bullet R^4 \bullet k \bullet T_{\mathrm{e}} \bullet F \bullet L},$$

where P_{CW} is the average continuous-wave (CW) transmitted power, T_{Dwell} is the dwell time, G_{T} is the transmitter antenna gain, G_{R} is the receiver antenna gain, λ is the wavelength, σ is the RCS, R is the detection range, k is the Boltzmann constant, T_{e} is the effective noise temperature, F is the noise factor, L is the loss, and SNR is the output signal-to-noise ratio. The periodic repetition interval (PRI) is calculated from the target speed of 108 km/h. The antenna array size is derived from the angular resolution of 13°, and the resultant antenna gain is approximately 20 dB from the array size. An FMCW bandwidth of 150 MHz is chosen for the range resolution of 1 m. The transmitter power is derived from the measured isolation characteristic of approximately 50 dB between a transmitter array antenna and a receiver array antenna in our pre-fabricated system platform. The 50-dB isolation is measured at approximately 20 cm between the antennas. Therefore, the average input power of each patch antenna of the 8 × 8 array resulting from the TX-to-RX leakage is approximately –38 dBm; this power is typically the highest among the receiver input signals. Figure 1 shows the FMCW radar system structure for our receiver IC design work. The FMCW system is composed of an FMCW generator, 8 × 8 phased-array transmitter, four receivers that have a 4 × 4 phased array in each receiver path, and a digital signal processing part, including four analog-to-digital converters (ADCs). The FMCW generator is composed of a fractional-*N* phase-locked loop (PLL) with an f_{REF} of 50 MHz. The 8 × 8 phased-array transmitter adopts a conventional RF phase-shifting architecture. The four receivers are for fine-angle detection by the mono-pulse algorithm [11], and the 4 × 4 phased sub-array receiver also adopts the RF phase-shifting architecture. The sampling rate of the ADC is 12.5 mega samples per second (MSps) to cover a maximum beat frequency of 6.002 MHz.

TABLE 1 Design target and specification

	Value
Design target parameter	
Radar waveform type	FMCW
Carrier frequency	X-band (8.2 GHz)
Target speed (km/h)	108
Range (RCS = 0.01 m^2, P_d = 0.9, P_{fa} = 1e-6, Swerling case 3)	
Max (m)	1000
Min (m)	10
Field of view (deg)	
AZ	±45
EL	±45
Resolution	
Range (m)	1
Angle (deg)	13
Specification results	
Antenna array size	8 × 8
Antenna gain (dB)	20
Loss (dB)	6.02
Required SNR (dB)	13.37
Receiver NF (dB)	6
Waveform bandwidth (MHz)	150
PRI (us)	250
Dwell time (ms)	38.5
TX power (dBm)	30

Figure 2 shows the floor plan of the receiver panel [12]. It is composed of an 8 × 8 antenna array, which has four sectors of a 4 × 4 sub-array, 16 RF low-noise amplifier (LNA)-phase-shifter (PS) chips, on-board Wilkinson power combiners, and a four-channel (4ch) RX chip each. The antenna is a rectangular patch type. The 2 × 2 RF LNA-PS chip has four channels of a single-to-differential

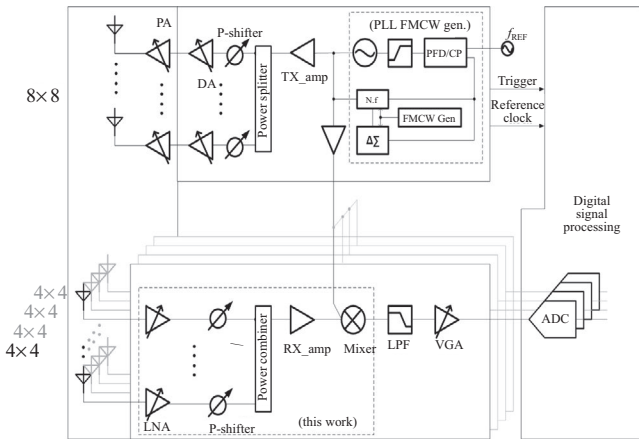


FIGURE 1 FMCW radar system structure

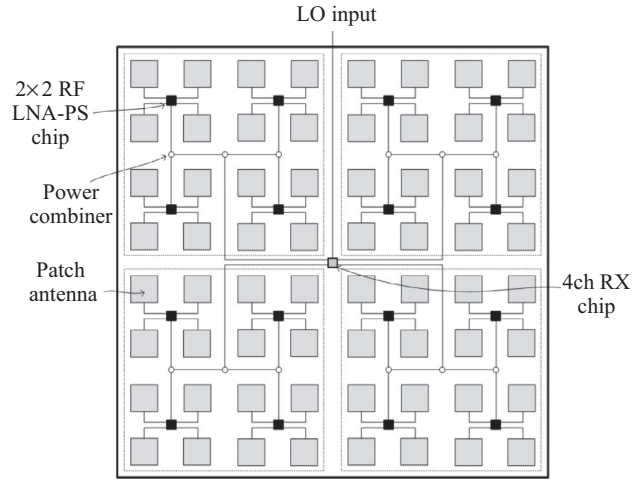


FIGURE 2 Floor plan of receiver panel

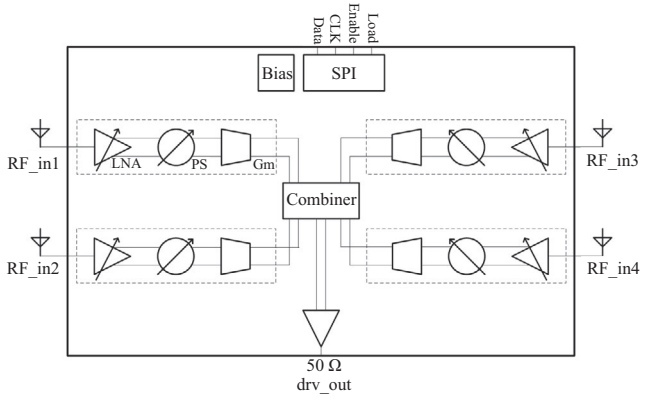


FIGURE 3 Block diagram of 2 × 2 RF LNA-PS chip

LNA and PS, four-channel combiner, and 50-ohm driver. It includes a serial-to-parallel interface (SPI) to control the internal blocks. Figure 3 shows the block diagram of the 2 × 2 RF LNA-PS chip. The four channels are combined by a current summing method using a trans-conductor (Gm) and combiner. The differential-to-single 50-ohm driver is

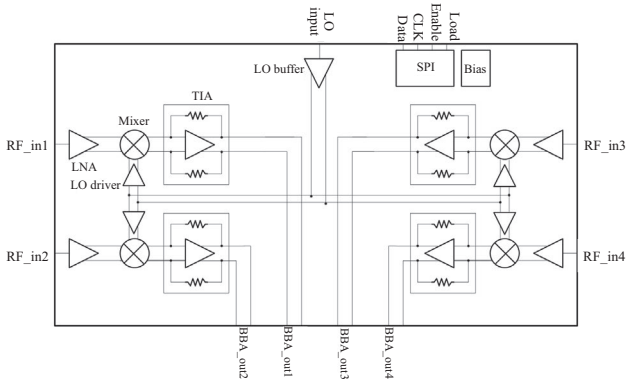


FIGURE 4 Block diagram of 4ch RX front-end chip

used for output driving. Figure 4 shows the block diagram of the 4ch RX front-end chip. The baseband analog (BBA) part of the 4ch RX chip will be integrated into our future work. The 4ch RX front-end chip has four channels of a single-to-differential LNA, passive mixer, trans-impedance amplifier (TIA), and single-to-differential LO buffer. It also includes an SPI to control internal blocks.

3 | CIRCUIT DESIGN

3.1 | LNA of the 2 × 2 LNA-PS chip

Figure 5 shows the circuit of the LNA designed for the 2 × 2 LNA-PS chip. All I/O pads, including RF, and power supply pads are protected using standard electrostatic discharge (ESD) cells supplied by the Taiwan Semiconductor Manufacturing Company (TSMC). The essential functions of the LNA are low-noise amplification, gain control, input impedance matching, and single-to-differential conversion for providing a differential signal to the next stage. The source-coupled first-stage cascode amplifier provides these functions, and the second differential inverter-amplifier drives the following quadrature generator of the phase shifter. The source-coupled first-stage amplifier for single-to-differential conversion saves

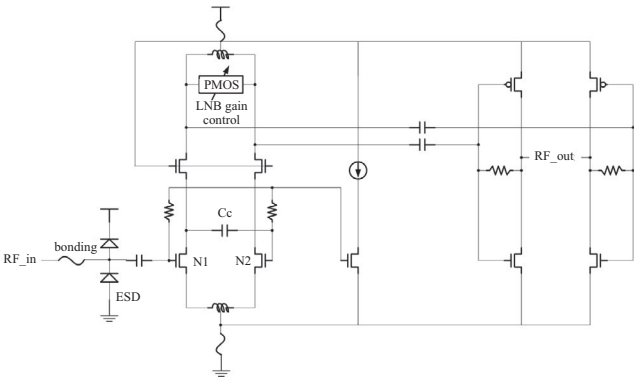


FIGURE 5 LNA circuit of 2 × 2 LNA-PS chip

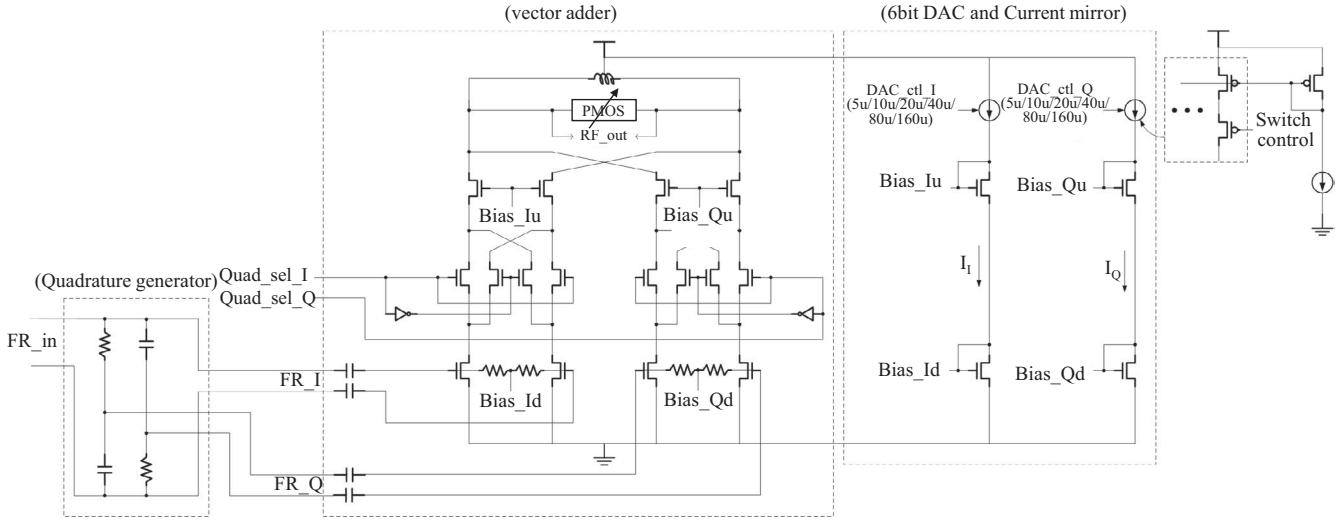


FIGURE 6 Phase-shifter circuit of 2 × 2 LNA-PS chip

substantial area compared with a transformer-based input stage [13,14]. The purpose of the capacitor, Cc, is to increase the differential gain. The RF front end of the FMCW receiver must cover a wide dynamic range because the RF input signal has a broad distance-based signal amplitude range and a broad signal range for various RCSs. In such cases, to avoid receiver saturation, the LNA has the function of gain control, which is performed by switching the P-type metal oxide semiconductor (PMOS) transistors in the LC (inductance-capacitance) tank load. The on-resistance of the switched PMOS controls the quality factor of the LC tank load.

3.2 | Phase shifter of the 2 × 2 LNA-PS chip

The integrated RF active phase shifter for the 2 × 2 LNA-PS chip is shown in Figure 6. It is composed of the quadrature generator, vector adder, 6-bit digital-to-analog converter (DAC), and current mirror. The quadrature generator is designed with a conventional resistance-capacitance (RC) poly-phase network because it is advantageous for integrated high-frequency and low-power consumption applications. The vector adder is constructed with two cascode variable gain amplifiers (VGAs). The two cascode VGAs with the

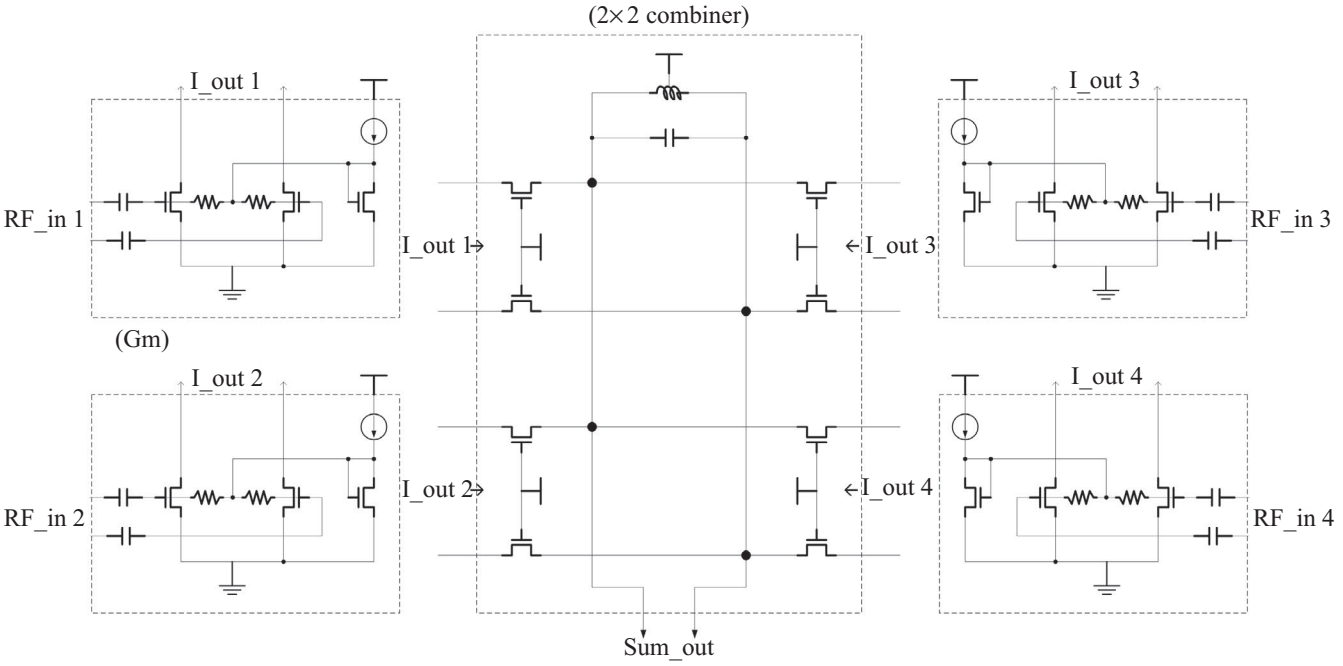


FIGURE 7 Current-mode channel combiner of 2 × 2 LNA-PS chip

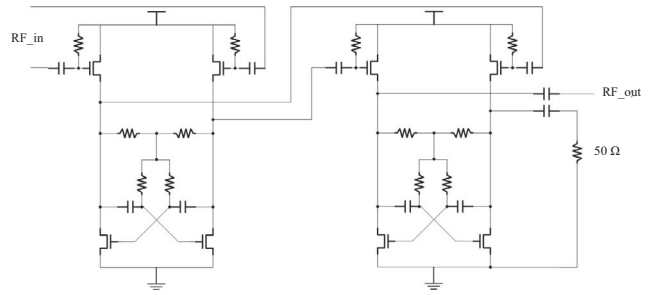


FIGURE 8 Differential-to-single output stage of 2 × 2 LNA-PS chip

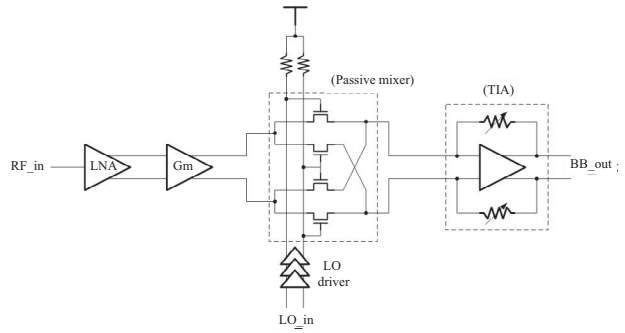


FIGURE 9 Single path RX front-end circuit of 4ch RX chip

quadrant selection switches in the middle are merged at the output node and synthesize the desired phase by adding RF_I and RF_Q from the previous quadrature generator with proper gains in the current domain. Two six-bit current-mode DACs control the bias ratio of I_Q/I_I for output phase generation, and the control inputs of the DACs are set such that $I_Q + I_I = \text{constant}$ for all phase states for a constant amplitude response at the output.

3.3 | Combiner and output stage of the 2 × 2 LNA-PS chip

The combiner is realized with cascode amplifiers for wideband signal combination, as shown in Figure 7. The input signal is converted to a current by the differential input pair in each channel and transferred to the cascode transistors of the 2 × 2 combiner. A short layout line from the transconductance (Gm) stage to the cascode transistors of the 2 × 2 combiner is used in our design for suitable current-mode operation, and the LC tank load is used for the final 4-channel combining. The differential-to-single output stage is shown in Figure 8. The first stage consists of a source follower and a cross-coupled common source to obtain gain. The second stage consists of a source follower providing wideband output matching and a cross-coupled common source stage with a unity gain. One of the differential output signals of the second stage drives a 50-ohm load, and an integrated 50-ohm resistor terminates the other.

3.4 | RX front end of the 4ch RX chip

The single path RX front-end circuit of the 4ch RX chip is shown in Figure 9. It is composed of an LNA, a transconductor (Gm), a passive mixer, a trans-impedance amplifier (TIA), and LO driver. The circuit topology of the LNA is the same as that of the 2 × 2 RF LNA-PS chip, but the gain is lower than the LNA as the linearity of the 4ch RX front-end chip is critical because of the high input signal amplitudes resulting from the previous power combiner output. The Gm converts the voltage signal to a current signal, the current passes to the passive mixer, and the current signal is converted to a voltage signal by the TIA. This current-mode RF front end is effective for a highly linear receiver. The LO driver is composed of one push-pull input amplifier and two inverter-type amplifiers. The single-to-differential LO buffer of the 4ch RX chip is shown in Figure 10. It is composed of a 50-ohm input matching resistor, a single-to-differential converter, and a differential push-pull amplifier. The single-to-differential converter design is based on a push-pull topology. The sizes of the source follower transistor and the common source amplifier transistor are the same; therefore, the gain and phase error are small during operation. The benefit of this LO buffer is its small area utilization compared with a passive transformer balun [12,13].

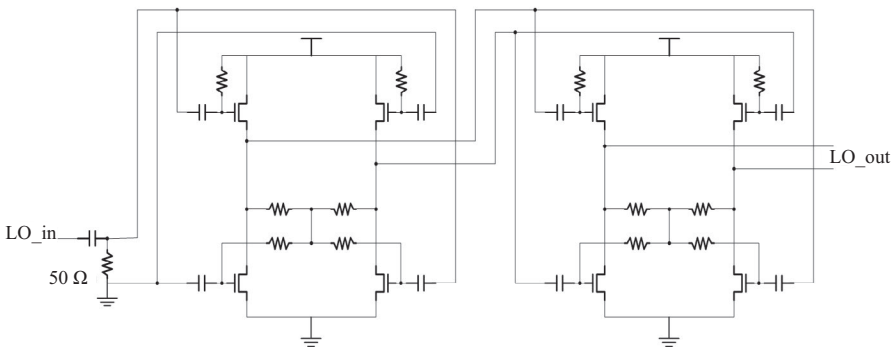
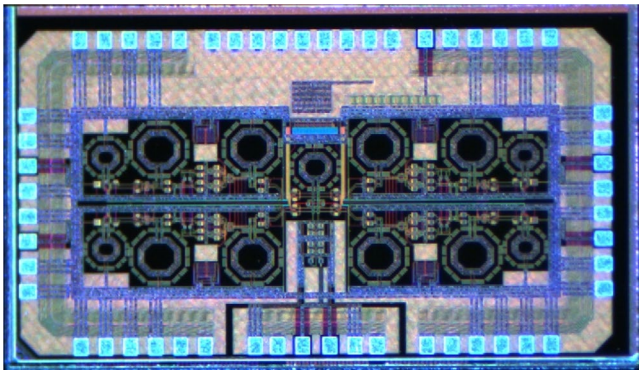


FIGURE 10 Single-to-differential LO buffer of 4ch RX front-end chip

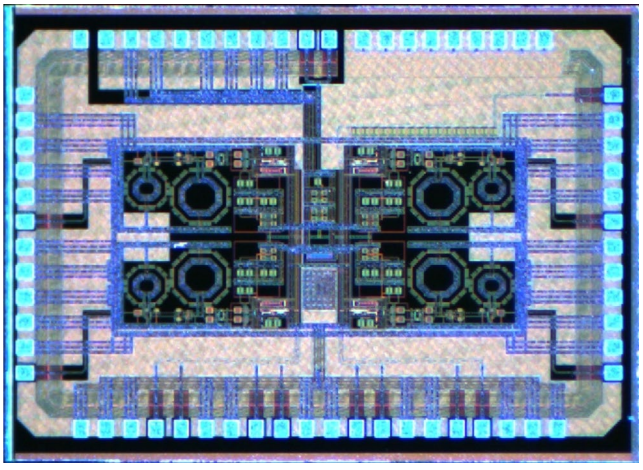
4 | MEASURED RESULTS AND DISCUSSION

The 2 × 2 RF LNA-PS chip and the 4ch RX front-end chip of the phased-array receiver are realized via a 65-nm CMOS 1P9M process. The chips are encapsulated in the 32-pin quad-flat no-leads (QFN) package and are tested on the Rogers PCB. Figure 11 shows the microphotographs of the chips. The sizes of the 2 × 2 RF LNA-PS chip and 4ch RX front-end chip are 2.39 mm × 1.3 mm and 2.42 mm × 1.62 mm, respectively.

Figure 12 presents the S-parameter measurement results of the 2 × 2 RF LNA-PS chip as a function of the gain control. The maximum gain (S_{21}) is approximately 20 dB, and the gain control range is 15 dB at 8.2 GHz. Comparing the simulation results, the S_{11} and S_{22} parameters are degraded by packaging effects. However, the system performance depends on the NF and gain of the receiver, which means that the S_{11} and S_{22} are not parameters that directly affect the system performance. Figure 13 shows the measured noise figure of the 2 × 2 RF LNA-PS chip at maximum gain. The noise figure is measured using the input and output of the single channel connected to the NF analyzer, and the input ports of the other channels terminated to 50 ohms. Therefore, the single-channel NF of the 2 × 2 RF LNA-PS chip is approximately 6.4 dB resulting from the measured system noise figure of 12.4 dB [15,16]. The measured NF value includes a PCB loss of approximately 0.7 dB, which is measured using an independent PCB pattern of the input trace. The measured phase responses at 8.2 GHz excited by the 6-bit digital data inputs to the I/Q DACs and the 2-bit quadrature selection digital data input are shown in Figure 14. The measured phase data are achieved by sweeping the phase control codes using a software program from 0° to 360°. For the linearized 6-bit phase resolution, we have extracted 6-bit codes from the 8-bit control codes of the 6-bit DAC control code and 2-bit quadrature selection code. The RMS phase error is approximately 0.35°, and the RMS gain error is approximately 2 dB over the sweep.



(A)



(B)

FIGURE 11 Chip microphotographs of (A) the 2 × 2 LNA-PS chip and (B) the 4ch RX front-end chip

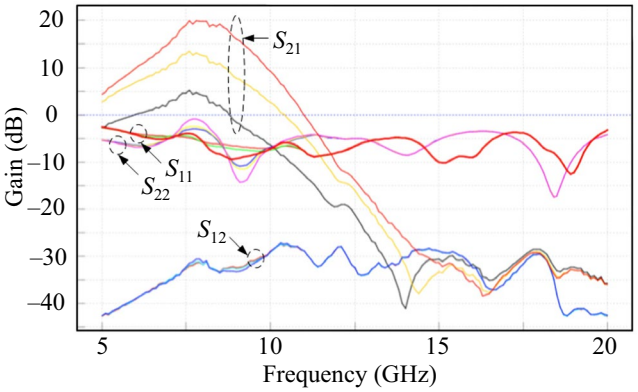


FIGURE 12 Measured S-parameter results of 2 × 2 RF LNA-PS chip

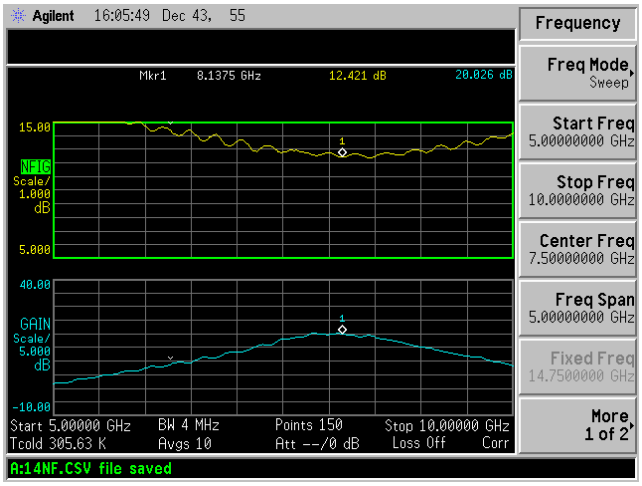


FIGURE 13 Measured noise figure results of 2 × 2 RF LNA-PS chip at maximum gain

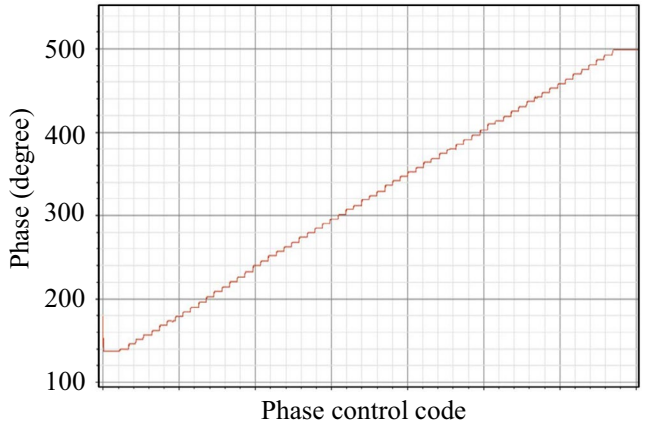


FIGURE 14 Measured 6-bit phase response at 8.3 GHz of 2 × 2 RF LNA-PS chip

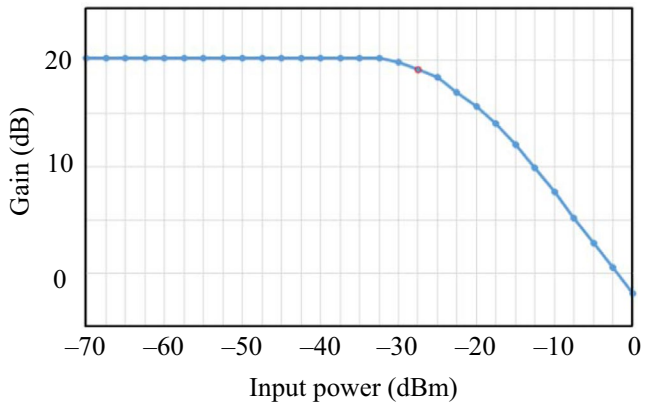


FIGURE 15 Measured 1-dB compression point of 2 × 2 RF LNA-PS chip

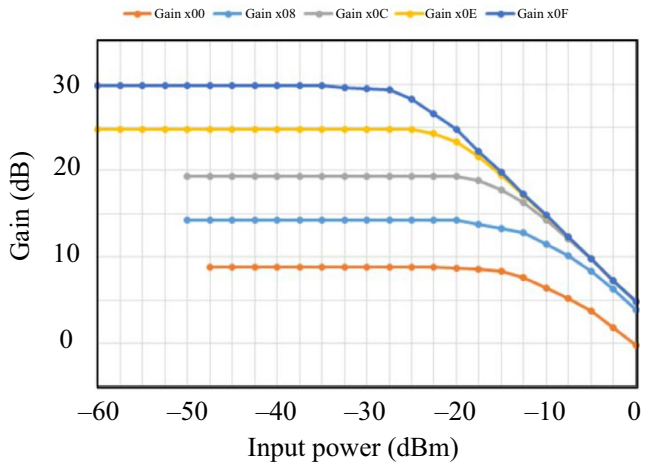


FIGURE 16 Measured 1-dB compression point of 4ch RX front-end chip

The isolation properties among the channels are critical in a 2 × 2 LNA-PS chip. The developed 2 × 2 LNA-PS chip shows an input port isolation of 24 dB between 1 and 2 of the left side or between 3 and 4 of the right side. The isolation between left-side ports and right-side ports is approximately 40 dB. In the worst case of an isolation of 24 dB, the resultant phase variation by the other channel is <0.5° with a phase difference of 22.5° between two channels in our simulation. The measured input 1-dB compression point of approximately –27.5 dBm of the 2 × 2 RF LNA-PS chip is shown in Figure 15 and is measured in a single channel. Moreover, the 1-dB compression point is higher than the highest average input power of −38 dBm of each patch antenna of the 8 × 8 array, resulting from TX-to-RX leakage. The 4ch RX front-end chip is measured with 0 dBm LO input power. Figure 16 shows the measured input 1-dB compression point of approximately −17.5 dBm at a gain of 14 dB. The gain of the 4ch RX front-end chip is controllable to cover a combined power level in the previous stage. The measured performance summary is shown in Table 2.

TABLE 2 Performance summary

Design technology	
Technology	TSMC 65-nm GP CMOS 1P9M
Supply voltage (V)	1.2
Frequency band (GHz)	8.2
2 × 2 RF LNA-PS chip	
Number of integrated channels	2 × 2 = 4
LNA gain (dB)	20(HG)/13(MG)/5(LG)
NF/ single-channel (dB)	6.4
Input P1dB (dBm)	–27.5 (@HG)
Phase-shifter resolution (bit)	6
DC current (mA)	82/4-channels
Area (mm^2), PADs included	2.39 × 1.3
4ch RX front-end chip	
Number of integrated channels	2 × 2 = 4
Gain range by TIA control (dB)	30–9
Input P1dB (dBm)	–17.5 (@Gain = 14 dB)
DC current (mA)	97/4-channels
Area (mm^2), PADs included	2.42 × 1.62

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Bon-Tae Koo received his MS degree in electrical engineering from Korea University, Seoul, Rep. of Korea, in 1991. In 1991, he joined the System Semiconductor Division, Hyundai Electronics Company, Ichon, Rep. of Korea, where he was involved in the chip design of video codecs and DVB modems. From 1993 to 1995, he was with HEA, San Jose, USA, where he was responsible for the design of the MPEG2 video codec chip. From 1996 to 1997, he was with TVCOM, San Diego, USA, where he worked on the design of a DVB modem chip. In 1998, he joined Dongbu Electronics as a team leader with the Semiconductor System Laboratory, where he focused on the methodology of semiconductor chip design. In 1999, he joined the Application SoC team, ETRI as a team leader and worked on the chip design of MPEG4 video, T-DMB receivers, LTE femtocell modems, and DSP processors. In 2016, he joined the RF research group in ETRI, where he is currently a project leader.