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Effect of Nitrogen, Titanium, and Yttrium Doping on High-K Materials as Charge Storage Layer

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Abstract: Non-volatile memory is approaching its fundamental limits with the Si_3N_4 storage layer, necessitating the use of alternative materials to achieve a higher programming/erasing speed, larger storage window, and better data retention at lower operating voltage. This limitation has restricted the development of the charge-trap memory, but can be addressed by using high-k dielectrics. The paper reviews the doping of nitrogen, titanium, and yttrium on high-k dielectrics as a storage layer by comparing MONOS devices with different storage layers. The results show that nitrogen doping increases the storage window of the Gd_2O_3 storage layer and improves its charge retention. Titanium doping can increase the charge capture rate of HfO_2 storage layer. Yttrium doping increases the storage window of the $BaTiO_3$ storage layer and improves its fatigue characteristics. Parameters such as the dielectric constant, leakage current, and speed of the memory device can be controlled by maintaining a suitable amount of external impurities in the device.

Keywords: Charge storage layer, Doping on high-k materials, Metal-oxide-nitride-oxide-semiconductor

1. INTRODUCTION

The evolution of metal-oxide-nitride-oxide-semiconductor (MONOS) memory forces to achieve faster programming/erasing speed, larger storage window, stronger fatigue resistance and better data retention at lower operating voltages as we move towards the further reduction in memory size. The basic structure of MONOS is composed of P-type Si substrate, the source and drain of N-type Si, the tunneling layer of dielectric, the silicon nitride (Si_3N_4) charge storage layer, the barrier layer of dielectric (SiO_2) and the metal gate from the bottom to top as shown in Fig. 1(a). Due to the influence of tunneling effect and leakage current increment, the minimum limit thickness of traditional dielectric silicon dioxide is about 1.4 nm [1]. Further, parameters such as the storage window, programming/erasing speed of Si_3N_4 storage layer are approaching their limits and are difficult to be improved. These problems limit the development of MONOS memory. Therefore, the search about new materials has become important in recent years. MONOS memory using different high-k materials have been investigated recently. Many studies shown that high-k materials are potential candidates to replace nitride layer in MONOS memory.

High-k material is a dielectric material whose dielectric constant is greater than 3.9. In the case of the same capacitance value, high-k material has a smaller equivalent oxide thickness [2]. The effective oxide thickness of the device can be effectively reduced by using high-k material. At present, high-k materials are mainly investigated as tunneling layer, blocking layer and storage layer. Table

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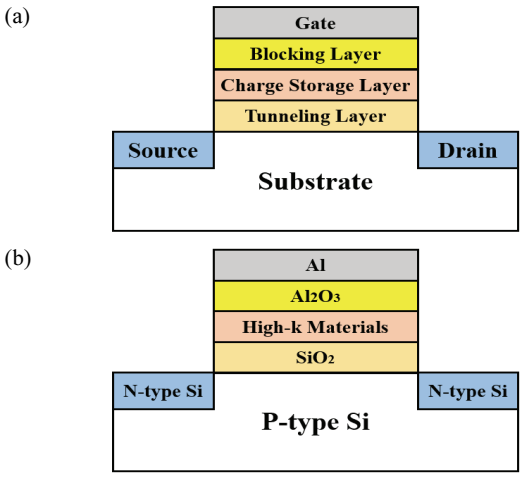

Fig. 1. (a) Structure of MONOS and (b) component of high-k MONOS.

Table 1. Dielectric constant and band gap of the materials.

Material	Dielectric constant	Band gap (eV)
SiO_2	3.9	8.9
Si_3N_4	7	5.1
Al_2O_3	9	8.7
HfO_2	25	5.9
ZrO_2	25	5.8
La_2O_3	30	4.3
TiO_2	80	3.5

1 shows the details of some high-k dielectrics utilized frequently for NVM applications. In this paper, MONOS memory structure shown in Fig. 1(b) has been reviewed as the function of high-k materials which act as the storage layer.

2. METHOD FOR EXPERIMENT

The deposition technique plays an important role to define the properties of the charge storage layer. Factors such as uniformity, crystallinity, growth control are the different parameters which decide the quality of the deposited layer. Among the different deposition techniques used to grow high-k dielectrics, sputtering deposition is utilized wisely to prepare high-k material as a storage layer. Since most high-k materials can be made into target materials for deposition, there are a wide range of materials for sputtering deposition. Here, the different high-k dielectrics grown by sputtering techniques are reviewed.

Atomic layer deposition (ALD) is another widely used deposition method to grow high-k dielectrics. ALD deposits high-k dielectrics layer by layer on the substrate surface in the form of a single atomic layer, which can prepare high quality dense film without defects.

3. RESULTS AND DISCUSSIONS

3.1 Effect of nitrogen doping in Gd_2O_3

Nitrogen can be doped into the high-k material storage layer during the deposition process or the annealing process. One method is to add N_2 to the atmosphere of sputtering deposition. When the target is deposited, nitrogen is also deposited together. The nitrogen content in the deposition can be controlled by changing the ratio of N_2 and Ar in the atmosphere. Annealing with nitrogen containing gas can also achieve the purpose of doping nitrogen. Available gases are N_2, NO_2, and NH_3. Among them, NH_3 has the best effect. The nitrogen content in the deposition is controlled by changing the annealing time and temperature [3-5]. The nitrogen doped in the storage layer will combine with the high-k material to form a strong metal-nitrogen bond. This deepens the energy level of charge traps and introduces a large number of charge traps [6]. The introduction of nitrogen can reduce the formation of metal-silicon bonds near the interface, that is, inhibit the formation of metal silicide. This can significantly improve the quality of the interface. The metal silicide near the interface will not only reduce the quality of the interface [7], but also reduce the dielectric constant of the storage layer [8]. Nitrogen increases the dielectric constant of the storage layer by inhibiting the formation of metal silicide. The increase in charge traps enlarges the storage window and increases the charge trapping rate. Because of the increase of charge trapping rate [9] and the dielectric constant, the programming/erasing speed is accelerated. The improvement of the interface quality and the deepening of the charge trap energy level improve the fatigue characteristics and retention characteristics.

The Liu et al. [10] investigates the application of Gd_2O_3 charge storage layer with different element composition of the Gd and N_2. The storage layer is made by sputtering deposition of Gd_2O_3 as a target. The storage layer deposited in an Ar atmosphere is named GN0. The storage layer deposited in an Ar and N_2 (2:1) environment is named GN1. Table 2 shows the Microscopic analysis of samples. The N_2 in the deposition atmosphere can be deposited together with the target. The nitrogen doped in the storage layer can increase the crystallization temperature, thereby making the material in an amorphous state. At the same time, the doping of nitrogen can reduce the Gd silicide at the interface, thereby improving the quality of the interface. As observed Fig. 2(a) that the programming/erasing speed of sample GN1 is faster than sample GN0. This is because nitrogen introduces more charge traps and improves the efficiency of charge capture [10]. Nitrogen contents also increases the dielectric constant of the storage layer and increases the current of the tunneling layer. Sample GN0 lost 42% of charge after 2.8 hours, and sample GN1 lost 3% of charge as observed from Fig. 2(b). The nitrogen increases charge retention by 12%. Because the doping of nitrogen deepens the energy level of the charge trap, more energy is needed to lose the charge. And the nitrogen element improves the quality of the interface, thereby reducing the chance of charge loss.

Table 2. Microscopic analysis of samples [10].

	GN0	GN1
Composition (XPS)	$Gd_{0.317}O_{0.683}$	$Gd_{0.368}O_{0.587}N_{0.045}$
Crystallinity (XRD)	Weak cubic-Gd_2O_3 (200) peaks	No clear diffraction peak
Surface quality (XPS spectrum)	More Gd silicide	Less Gd silicide

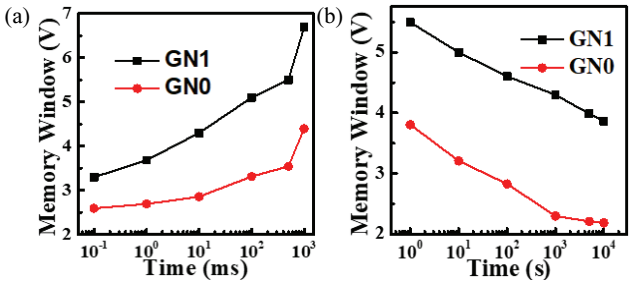

Fig. 2. Characteristic of sample GO/GN (a) programming/erasing speed at +/-13 V and (b) retention characteristic at +/-13 V for 100ms [10].

3.2 Effect of titanium doping in HfO_2

The method of doping titanium is to use high-k material target and titanium target for co-sputtering deposition. The content of titanium doping is controlled by changing the ratio of the sputtering power of the two targets [11]. This method can easily control the doping concentration, but the process is a bit complicated [12]. The dielectric constant of titanium oxide is relatively large [13], so the dielectric constant of the titanium-doped high-k storage layer will increase. And titanium doping will increase the effective charge trapping cross- sectional area [14-16]. This will increase the carrier injection efficiency and charge trapping rate. However, titanium will diffuse to the vicinity of the interface and form titanium-silicon bond with silicon, that is, titanium consumes SiO_2 to form titanium silicide. The transition layer composed of titanium silicide will reduce the interface quality. The high dielectric constant can increase the storage window of the device. High carrier injection efficiency and charge trapping rate can effectively increase the programming/erasing speed. However, the degradation of interface quality caused by titanium doping will severely weaken the charge retention of the device.

Three samples with different titanium doping in HfO_2 are analyzed to determine the proportion of titanium to be added for the improvement of retention properties were reported by Chen et al. [17] The titanium content of samples increases in turn. Figure 3(a) shows the respective P/E properties of the NVM device as a function of titanium contents in HfO_2 film. It is seen that, the increase in the Ti content tends to faster speed of programming/erasing of sample. The titanium content improves the dielectric constant and the charge capture efficiency of the film. Figure 3(b) shows the respective charge retention properties get worse with the increase in the Ti content. This is because of the excess Ti content forms the titanium silicide near the interface [18]. The silicide accelerates charge leakage. Considering the functional

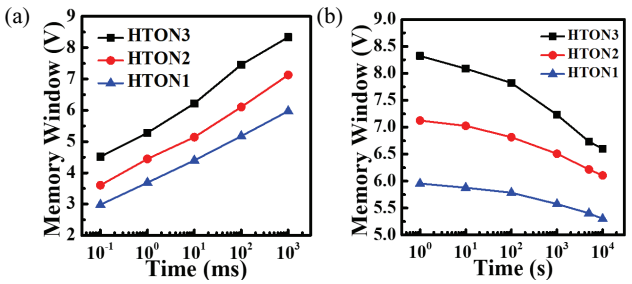

Fig. 3. Characteristic of sample HTON (a) programming/erasing speed at +/-12 V and (b) retention characteristic curves at +/-12 V for 1s [17].

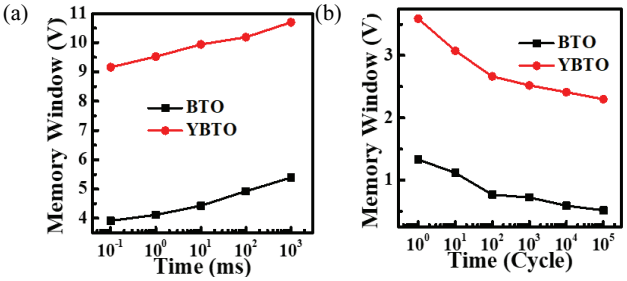

Fig. 4. Characteristic of sample BTO and YBTO (a) programming/erasing speed at +/-12 V and (b) endurance characteristic curves at +/-12 V for 100ms [25].

requirements of the thin film, when the proportion of titanium and hafnium is 1:1, the comprehensive performance of the device is optimal [19].

3.3 Effect of yttrium doping in $BaTiO_3$

The method of doping yttrium is sputtering deposition with a specific target material. The high-k material powder and the yttrium metal powder are uniformly mixed in proportion and made into a target. The yttrium doping content of the film deposited by sputtering with this target is the same as the mixing ratio of the target [20]. The advantages of this method are simple process and stable doping concentration. But the disadvantage is that the doping concentration cannot be changed [21]. Doped yttrium has a strong binding energy. It can form a large number of metal-oxygen- yttrium bonds with high-k materials. On the one hand, a large number of charge traps are introduced, and on the other hand, the metal silicide produced by the reaction of high-k materials with silicon is reduced. The generation of metal silicide is suppressed, so the interface quality is improved [22]. But at the same time, the yttrium element diffuses a little to other layers and the charge trap energy level becomes slightly shallower [23]. The increase in charge traps expands the storage window. Although the diffusion of yttrium element and the shallowing of the trap energy level have a bad influence on the retention characteristics and endurance characteristics of the device, the yttrium element can largely improve interface quality [24]. So overall, the doping of yttrium element can improve the retention characteristics and endurance characteristics of the device.

Another group memory devices having $BaTiO_3$ storage layer doped with and yttrium or not has been analyzed by Shi et al. [25], and the performance changes after doping are compared. Figure 4(a) shows the programming/erasing speed of yttrium $BaTiO_3$ (YBTO) sample as compared to $BaTiO_3$ (BTO) sample. The programming/erasing speed of YBTO sample exceeds twice that of BTO sample. Because yttrium introduces a large number of charge traps [25] and increases the dielectric constant of the storage layer. The relatively shallow charge trap energy level also helps to increase the programming/erasing speed. Figure 4(b) shows after 10^5 programming/erasing cycles, the storage window of BTO sample was reduced by 61.1% and YBTO sample was reduced by 35.9%. Because there are many body traps and few interface traps, the probability of charge loss is relatively small. And the improved interface quality due to yttrium doping reduces the possibility of tunneling from the charge storage layer to the gate.

4. CONCLUSION

In summary, the compatibility of different groups of high-k dielectrics such as Gd_2O_3, HfTiO, BaTiO3 doping with nitrogen, titanium, or yttrium were investigated as the storage layer used in memory devices. The overall results show that, doping of external impurities (Y, Ti) in controlled manner is an important tool to decide the overall retention property of the memory device. Further, the content of nitrogen in the deposition atmosphere also

effects significantly to the memory performance. The doping of titanium can improve the dielectric constant, carrier injection efficiency and charge trapping rate of the high-k storage layer. And the doping of yttrium in $BaTiO_3$ can introduce more charge traps and reduce the formation of metal silicide at the interface. Overall, it is possible to achieve higher storage window at lower voltages with the use of high-k material with doping. The parameter such as dielectric constant, leakage current, speed of the memory device can be controlled by maintaining the proper amount of external impurities in the device. The expected results may vary when these doping elements were interchanged in different dielectrics.

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REFERENCES

[1] J. Robertson, *Eur. Phys. J. Appl. Phys.*, **28**, 265 (2004). [DOI: https://doi.org/10.1051/epjap:2004206]

[2] C. Zhao, C. Z. Zhao, S. Taylor, and P. R. Chalker, *Materials*, **7**, 5117 (2014). [DOI: https://doi.org/10.3390/ma7075117]

[3] R. P. Shi, X. D. Huang, J.K.O. Sin, and P. T. Lai, *Microelectron. Reliab.*, **65**, 64 (2016). [DOI: https://doi.org/10.1016/j.microrel.2016.07.148]

[4] L. N. Liu, W. M. Tang, and P. T. Lai, *Coatings*, **9**, 217 (2019). [DOI: https://doi.org/10.3390/coatings9040217]

[5] M. Kadoshima, M. Inoue, T. Maruyama, and M. Matsuura, *Jpn. J. Appl. Phys.*, **58**, SBBA10 (2019). [DOI: https://doi.org/10.7567/1347-4065/ab002c]

[6] S. Ozaki, T. Kato, T. Kawae, T. Ksto, and A. Morimoto, *J. Vac. Sci. Technol., B*, **32**, 031213 (2014). [DOI: https://doi.org/10.1116/1.4876135]

[7] Z. Y. Lu, C. J. Nicklaw, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, *Phys. Rev. Lett.*, **89**, 285505 (2002). [DOI: https://doi.org/10.1103/PhysRevLett.89.285505]

[8] H. Bachhofer, H. Reisinger, E. Bertagnolli, and H. von Philipsborn, *J. Appl. Phys.*, **89**, 2791 (2001). [DOI: https://doi.org/10.1063/1.1343892]

[9] H. X. Xu, J. P. Xu, C. X. Li, C. L. Chan, and P. T. Lai, *Appl. Phys. A*, **99**, 903 (2010). [DOI: https://doi.org/10.1007/s00339-010-5665-5]

[10] L. Liu, J. P. Xu, F. Ji, J. X. Chen, and P. T. Lai, *Appl. Phys. Lett.*, **101**, 033501 (2012). [DOI: https://doi.org/10.1063/1.4737158]

[11] S. Maikap, P. J. Tzeng, T. Y. Wang, C. H. Lin, L. S. Lee, J. R. Yang, and M. J. Tsai, *Electrochem. Solid-State Lett.*, **11**, K50 (2008). [DOI: https://doi.org/10.1149/1.2839762]

[12] W. Banerjee and S. Maikap, *Proc. 2009 IEEE International Workshop on Memory Technology, Design, and Testing* (IEEE, Hsinchu, Taiwan, 2009) p. 31. [DOI: https://doi.org/10.1109/MTDT.2009.15]

[13] W. Zhang, R. Liang, L. Liu, G. Yu, J. Wang, J. Xu, and T. L. Ren, *IEEE Trans. Nanotechnol.*, **17**, 1089 (2018). [DOI: https://doi.org/10.1109/TNANO.2018.2810885]

[14] H. W. You and W. J. Cho, *Appl. Phys. Lett.*, **96**, 093506 (2010). [DOI: https://doi.org/10.1063/1.3337103]

[15] S. Maikap, T. Y. Wang, P. J. Tzeng, C. H. Lin, T. C. Tien, L. S. Lee, J. R. Yang, and M. J. Tsai, *Appl. Phys. Lett.*, **90**, 262901 (2007). [DOI: https://doi.org/10.1063/1.2751579]

[16] Q. Wang, X. Kong, Y. Yu, H. Han, G. Sang, G. Zhang, Y. Yi, and T. Gao, *Phys. Chem. Chem. Phys.*, **21**, 20909 (2019). [DOI: https://doi.org/10.1039/C9CP04502C]

[17] J. X. Chen, J. P. Xu, L. Liu, and P. T. Lai, *Appl. Phys. Lett.*, **103**, 213507 (2013). [DOI: https://doi.org/10.1063/1.4829880]

[18] Y. A. Bachtiar and M. A. Sulthoni, *Proc. 2019 International Symposium on Electronics and Smart Devices (ISESD)* (IEEE, Badung-Bali, Indonesia, 2019) p. 1. [DOI: https://doi.org/10.1109/ISESD.2019.8909559]

[19] P. Han, T. C. Lai, M. Wang, X. R. Zhao, Y. Q. Cao, D. Wu, and A. D. Li, *Appl. Surf. Sci.*, **467**, 423 (2019). [DOI: https://doi.org/10.1016/j.apsusc.2018.10.197]

[20] S. Zhang and Y. Kuo, *ECS J. Solid State Sci. Technol.*, **7**, Q97 (2018). [DOI: https://doi.org/10.1149/2.0231805jss]

[21] T. Li, L. Wu, Y. Wang, G. Liu, T. Guo, S. Song, and Z. Song, *Mater. Lett.*, **247**, 60 (2019). [DOI: https://doi.org/10.1016/j.matlet.2019.03.090]

[22] M. L. Lee, H. Chen, C. H. Kao, R. K. Mahanty, W. K. Sung, C. F. Lin, C. Y. Lin, and K. M. Chang, *Vacuum*, **140**, 47 (2017). [DOI: https://doi.org/10.1016/j.vacuum.2017.02.009]

[23] T. Pan, L. Yen, S. Mondal, C. Lo, and T. Chao, *ECS Solid State Letters*, **2**, 83 (2013). [DOI: https://doi.org/10.1149/2.002310ssl]

[24] Y. Zhang, J. Xu, D. Y. Zhou, H. H. Wang, W. Q. Lu, and C. K. Choi, *Ceram. Int.*, **44**, 12841 (2018). [DOI: https://doi.org/10.1016/j.ceramint.2018.04.093]

[25] R. P. Shi, X. D. Huang, J.K.O. Sin, and P. T. Lai, *IEEE Electron Device Lett.*, **37**, 1555 (2016). [DOI: https://doi.org/10.1109/LED.2016.2615063]