Original Article

Feasibility study of multiplexing method using digital signal encoding technique

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ABSTRACT

Radiation imaging systems consisting of a large number of channels greatly benefit from multiplexing methods to reduce the number of channels with minimizing the system complexity and development cost. In conventional pixelated radiation detector modules, such as anger logic, is used to reduce a large number of channels that transmit signals to a data acquisition system. However, these methods have limitations of electrical noise and distortion at the detector edge. To solve these problems, a multiplexing concept using a digital signal encoding technique based on a time delay method for signals from detectors was developed in this study.

The digital encoding multiplexing (DEM) method was developed based on the time-over-threshold (ToT) method to provide more information including the activation time, position, and energy in one-bit line. This is the major advantage of the DEM method as compared with the traditional ToT method providing only energy information.

The energy was measured and calibrated by the ToT method. The energy resolution and coincidence time resolution were observed as 16% and 2.4 ns, respectively, with DEM. The position was successfully distributed on each channel. This study demonstrated the feasibility that DEM was useful to reduce the number of detector channels.

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1. Introduction

Silicon-photomultipliers (SiPMs) are utilized in various studies for radiation detectors in the positron emission tomography (PET) or gamma-camera because of advantages, such as higher gain, more compactness, higher photo-detection efficiency, and lower operating voltage [1–5]. The radiation imaging systems based on the SiPMs composed of a large of number of detectors to provide high sensitivity and high quality imaging. The radiation imaging systems, such as gamma camera, single photon emission computed tomography (SPECT) and positron emission tomography (PET), greatly benefit from multiplexing methods to reduce the number of data acquisition channels with preserving signal-to-noise ratio

(SNR) and minimizing development cost and system complexity [6]. The conventional multiplexing methods, such as resistive charge network circuit, could provide high channel reduction ratio, whereby the analog signal encoding [7,8]. However, these approaches often slow pulse down and degrade the amplitude of the sensor output, resulting in degradation of SNR [6]. In addition, these approaches required the high speed analog-digital converter (ADC) to provide the accurate analog signal encoding. This might increase the load of development cost and the power consumption in the imaging systems [9]. The time-over-threshold (TOT) method is one of the signal processing scheme which could reduce the cost and the complex electronics in PET system. The TOT method provides time and energy information by measuring the pulse arrival time and pulse duration over a preset threshold. The TOT method has significant advantages which are a simple system design and a low cost data acquisition (DAQ) system as compared with a conventional DAQ system using ADC [12–15].

In this study, the multiplexing concept based on digital encoding scheme was proposed to overcome the drawbacks of the conventional multiplexing methods and estimated by the feasibility study. The proposed multiplexing circuit can reduce the data acquisition channels without the ADCs, minimizing the degradation of analog signal. In proposed multiplexing method, output signals from SiPMs were directly encoded to one-bit digital signal involving arrive time, radiation energy, and activated position in a detector. The information can be acquiesced by one-channel time-to-digital converter (TDC) based on carry chain delay line in field programmable gate arrays (FPGA) without ADC. Although we prototype the idea with only eight channels, the performance of the proposed multiplexing method was evaluated by measuring energy resolution, coincidence timing resolution, and position identification.

2. Materials and methods

2.1. Principle of multiplexing method using digital signal encoding technology

Fig. 1 shows the digital signal processing of the proposed multiplexing method, called the digital encoding multiplexing (DEM) method in this study. The DEM method was developed based on time-over-threshold (ToT) method to provide the more information including the activation time, position, and energy in one-bit line. This is the major advantage of the DEM method as compared with the traditional ToT method providing only energy information.

Output of each SiPM splits two ToT outputs and one of the ToT outputs was delayed by the buffered delay line. The delay interval time of each channel was increased by 10 ns in order to distinguish channel positions (D1 = 10 ns, D2 = 20 ns, …, D8 = 80 ns). The encoded digital signal, configured by two square pulses in the single bit line, was modulated by the XOR-gate binary operation of the delayed ToT output and the non-delayed ToT output. The width value in first square pulse, first leading-edge in the encoded digital signal, and width value between first leading-edge and second leading-edge in the encoded digital signal means the channel position, time, and energy, respectively.

2.2. Digital encoding multiplexing circuit

The PET detector was composed of LYSO (Cerium-doped Lutetium Yttrium Orthosilicate) and GAPD (Geiger-mode Avalanche Photodiode) arrays of 4×4 individual pixels arranged with a pitch of 3.3 mm (Fig. 2). The LYSO array (Sinocera, China) was polished and separated with white epoxy, except for the entrance face, and the individual crystal size was $3 \times 3 \times 20$ mm^3. An individual LYSO crystal was coupled one-to-one to a separate pixel of the GAPD (SensL, Ireland).

The DEM method scheme, as shown in Fig. 3 (a), was based on an individual readout to prevent the distortion and degradation of pulses and time delay of pulses to classify the information of energy, timing, and position. The new multiplexing circuit consisted of amplifiers (AD8000, Analog devices, US), splitters (ADP-2-1, mini-circuit, US), comparators (ADCMP608, Analog devices, US), delay active elements (DS1100, Maxim integrated, US), and logic gate elements including the exclusive-OR logic gates (XOR, HMC851, Analog devices, US).
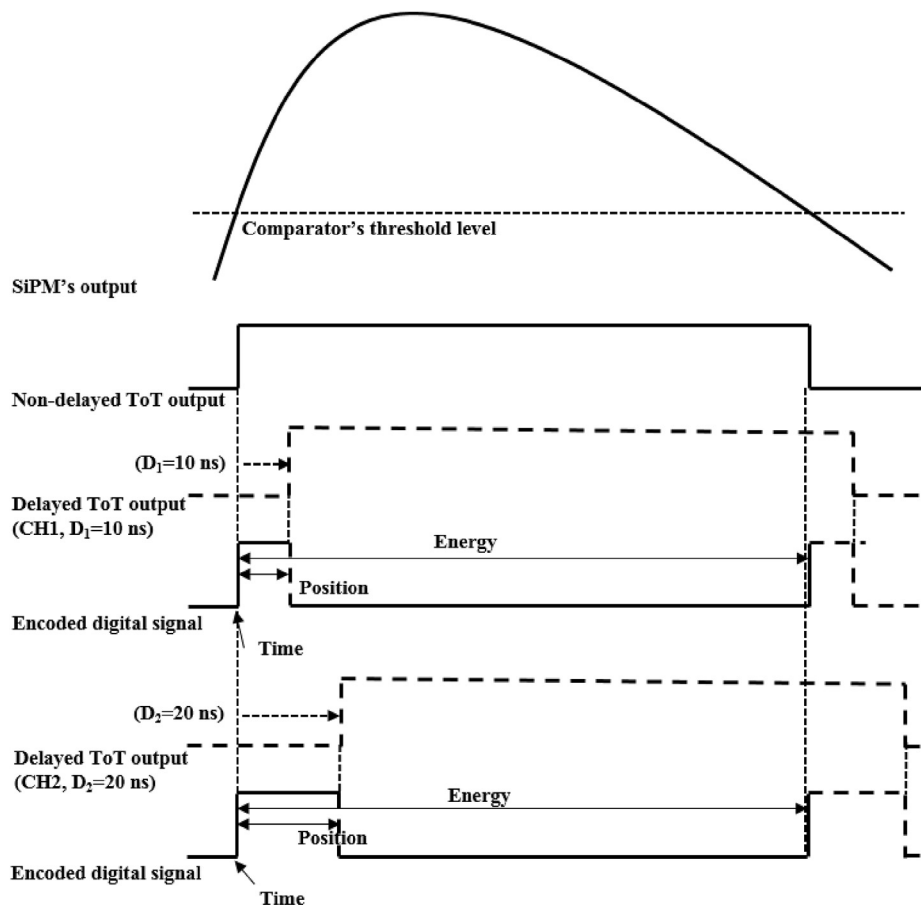

Fig. 1. Encoded digital signal processing in DEM circuit: The delay interval time of each channel was increased by 10 ns (D1 = 10 ns, D2 = 20 ns, …, D8 = 80 ns).
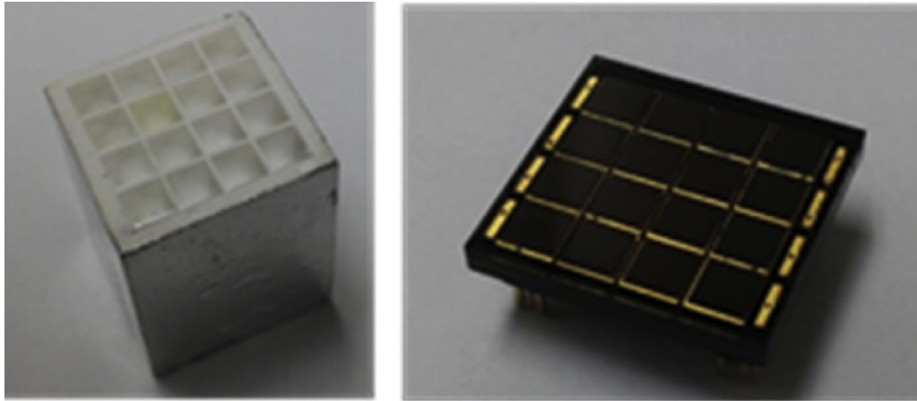
Fig 2. 4 × 4 matrix of 3 × 3 × 20 mm³ (a) LYSO crystal and SiPM array.
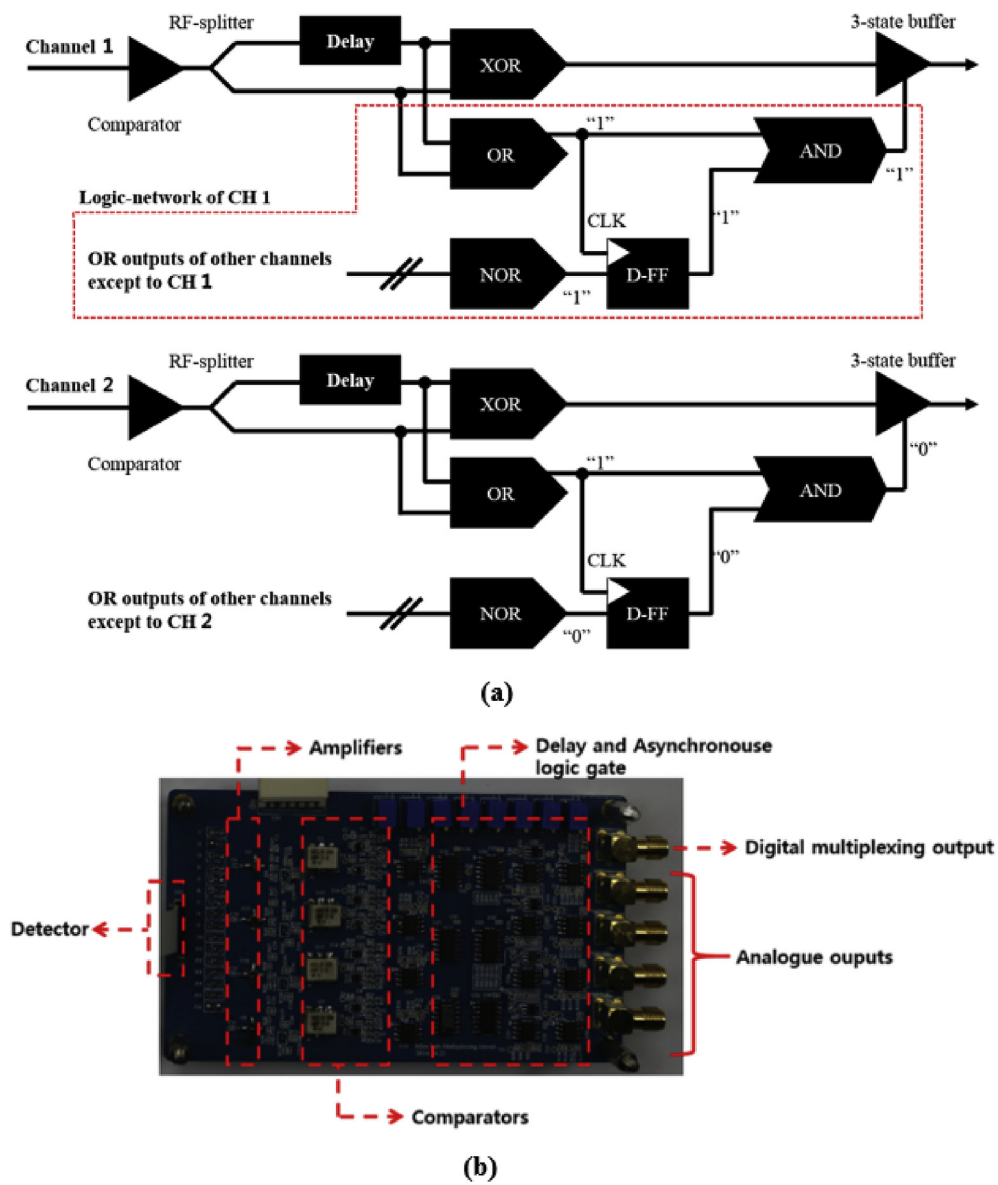

(a)

(b)

Fig. 3. Schematic diagram of the DEM circuit (a) and the constructed DEM circuit (b).

The signal from a channel was split into two split signals by the splitter after the amplifier, and the split signals were switched by ToT outputs using comparators. One of the digital signals was delayed as much as the set delay interval time, and the other was not delayed. The XOR implemented the logical synthesis using both delayed and non-delayed ToT output to generate the encoded digital signal.

The encoded digital signal can be transmitted to a logic-network consisting of logic-gate elements for the fastest signal among many channels of the detector before the Time-to-digital converter (TDC) in the FPGA. The logic-network of each channel was able to discriminate the fastest signal.

Fig. 3 (a) also shows a block diagram of the logic-network. Each channel had the logic-network consisting of logic-chips. NOR-gate, D-FF and three-state buffer play a role in discrimination of the first arrived signal. The D-FF used to distinguish the fastest signal or not by fading the OR-gate output combined by the delayed ToT signal and the non-delayed ToT signal into an operation clock of D-FF. If signal in CH 1 arrived earlier than the other signals, NOR-gate outputted "1" and the state of D-FF was "1" at the rising-edge of D-FF. This permitted the three-state buffer to pass the encoded digital signal of channel 1 until end of encoded digital signal. However, the three-state buffers of other channels were closed because their D-FF maintained "0" state. Fig. 3 (b) shows the proposed DEM circuit.

2.3. Principle of multiplexing method using digital signal encoding technology

Time-to−digital converter (TDC) implemented in FPGA (Spartan-6 LX45, Xilinx, USA) was designed using a tapped-delay line method composed of delay components and 2 flip-flop lines located beside CARRY4 chain [10]. The CARRY4 chain consisted of the series of delay components. Dual delay lines, consisting of two tapped-delay lines, were implemented to improve timing performance and differential non-linearity of TDC as shown in Fig. 4 [11]. Two-time stamp data of two tapped delay line were transmitted to host-PC using Chipscope soft and average value of 2 two tapped delay lines was calculated after adjusting the time difference of two tapped delay lines. The TDC designed in the FPGA was composed of

fine and coarse counters for the time of the tapped delay line. A ring oscillator to compensate for voltage and temperature (PVT) effect was placed close to the delay buffer line. Fig. 5 shows the manual placement of logic cells in FPGA. The TDC input needs to record the DNL histogram and generate a calibration Look-up table (LUT). The average and maximum time bin widths were 25 ps and 153 ps, respectively. Total delay bin size of carry chain was measured by 13 ns (496 bins). The intrinsic timing resolution was 41.6 ps (time jitter = ~7 ps).

3. Results

3.1. Pulse waveform of the encoded digital signal from the logic-network

Fig. 6 shows the analog signal and the encoded digital signal after the logic-network. The preamp output signal was converted into the ToT signal. Owing to the postponement of the logic-
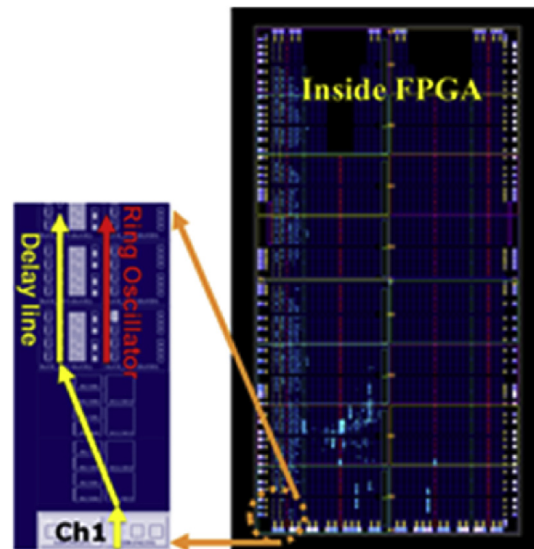

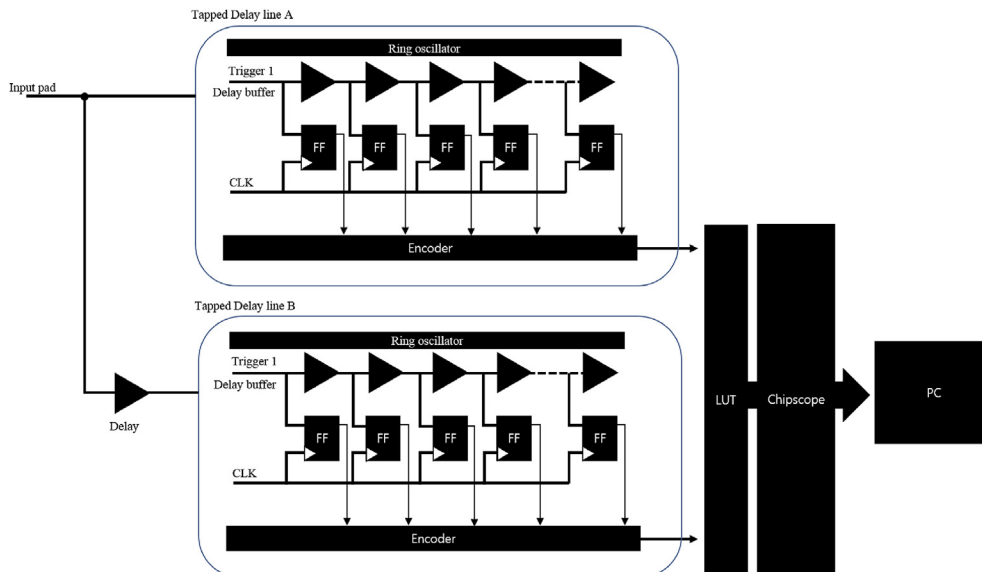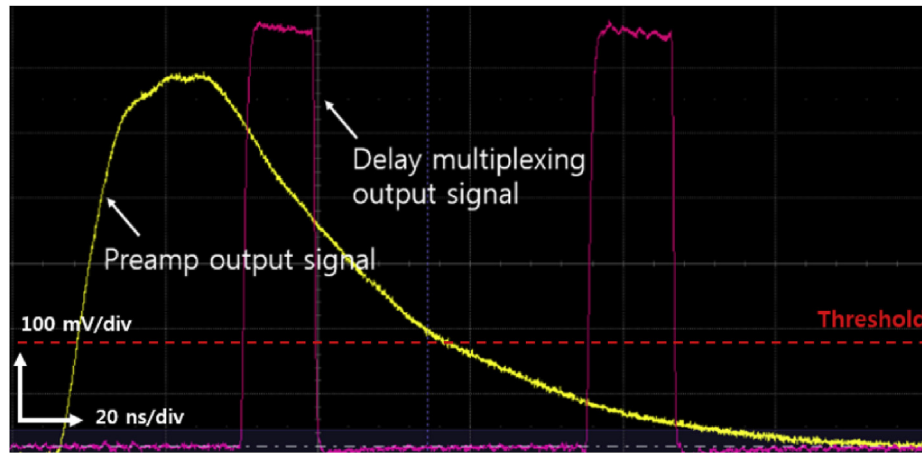**Fig. 5.** Logic cell manual placement of TDC in FPGA.

Fig. 4. Structure of dual-tapped delay line TDC implemented in FPGA.

Fig. 6. Output of preamplifier (yellow) was converted into the compressive digital signal after the process of the logic-network (red) acquired in the oscilloscope (20 GHz/sample). (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

network process, the encoded digital signal was delayed by approximately 18 ns. The rising and falling times of the encoded digital signal were under 3 ns. It was also demonstrated that eight channels were distinguished by delay interval times. The threshold level of comparators was set by 100 mV.

3.2. Energy resolution and coincidence resolving time (CRT)

The energy resolution and CRT were 16 ± 0.2% and 2.4 ± 0.3 ns, respectively. The gamma photons (511 keV and 1275 keV) from Na-22 were excellently measured although the ToT method has poor energy resolution and is nonlinear. The CRT was not applied to individual energy window for each channel of the SiPM. Fig. 7 shows the energy spectrum and CRT. The energy resolution was not calibrated.

3.3. Position identification accuracy

Fig. 8 shows the position histogram for eight channels. The positions of each channel were successfully discriminated by the predefined delay time intervals. However, two channels (1 and 2 channels), having small time width, showed nonlinear delay time because of errors in the logic-network. The time interval between Channel 1 and Channel 2 was under 8 ns that was not enough to distribute channel positions. The average full-width half maximum (FWHM) for all positions was 3.5 ns, and average time interval from peak to peak was 10 ns, which corresponds to the value in advance using the delay active elements.

4. Discussion and conclusion

This study demonstrated the feasibility that the multiplexing method using the digital encoding technique was useful to reduce the complexity of a large number of channels that transmit signals to a data acquisition system without ADC. The energy resolution, the CRT, and the position histogram for eight channels were obtained by using the dual delay line TDC in FPGA having 25 ps of the time bin width. We obtained the energy resolution of ~16% FWHM and the CRT of ~2.4 ns FWHM. The position histogram was identified by 10 ns of delay time interval for eight channels. The energy resolution shows almost the similar performance of ~20% but the timing performance was not good as compared with the previous study [12,19].

The encoded digital pulse of the DEM circuit included the activation time, energy and position information in only 1-bit line as shown in Fig. 6. This could be advantages to reduce the waste of I/O-pin in FPGA and logic-cells because the DEM based on TOT was the convenient method as compared to ADC using LVDS-serial interface method. If LVDS-serial interface method was implemented, a deserializer converting ADC output to energy value should be designed in FPGA. That could be the heavy load to FPGA building the dual tapped delay-line TDC occupying many logic-cells. Therefore, the DEM allowed that the low-cost FGPA could be applied in the radiation imaging system having the thousands of channels such as PET system and gamma-camera. The channels could be reduced by 8 times when using the prototype DEM method in this study as compared with individual readout method.
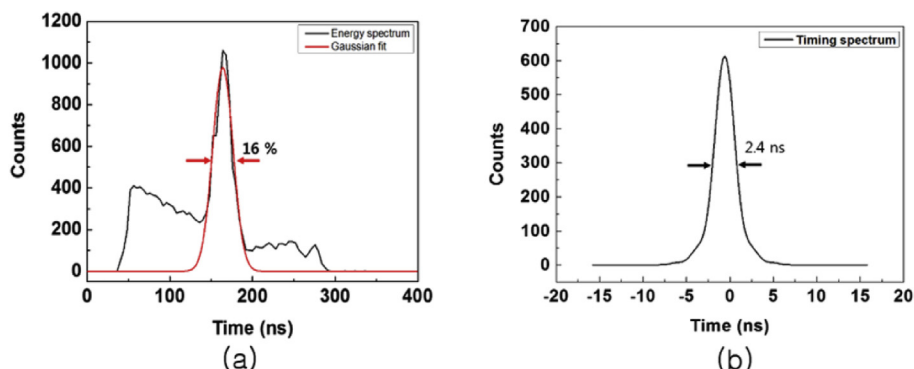
Fig. 7. (a) Energy spectrum acquired with one-detector channel and new multiplexing method using delay and asynchronous logic gate, and (b) CRT spectrum with Na-22.
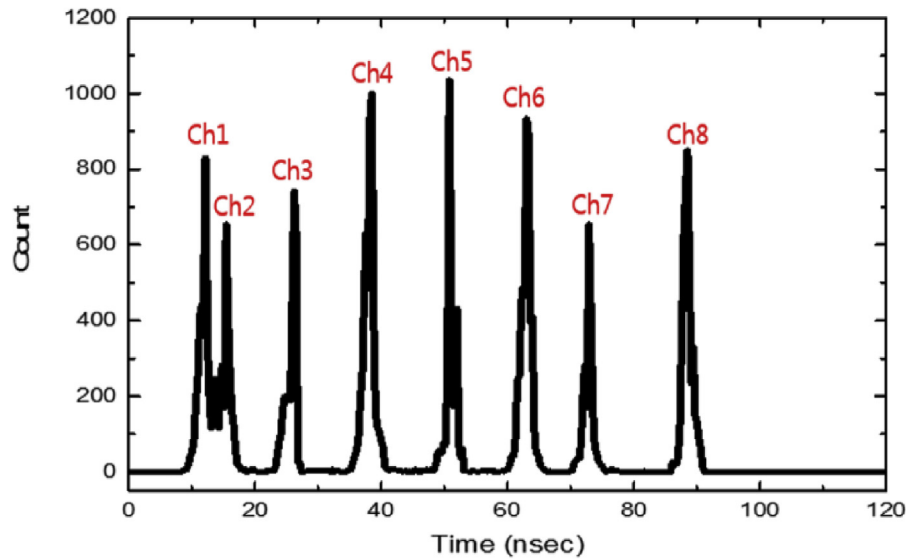
Fig. 8. Position histogram of eight channels according to different time intervals (10 ns, 20 ns, …, 80 ns)

Although the prototype DEM method had the limitation to increase the multiplexing ratio as compared with the traditional analog multiplexing methods such as Anger logic circuit (maximum multiplexing ratio of 64:4) and Row-sum column sum circuit (maximum multiplexing ratio of 128:8), the DEM method could minimize the error in outside of the detector because the DEM method could digitalize the position using the pulse width while the traditional analog multiplexing methods were vulnerable to electrical noise and ADC error [20]. The 18 ns of time delay due to the logic components and the high threshold level in comparator occurred the deterioration of CRT decreasing the accuracy of time pick-off.

Each position was successfully distinguished depending on 10 ns of the delay interval times. The FWHMs of each channel was about 3 ns in the position histogram as shown in Fig. 8. These results show that the encoded digital signal was useful to identify channels, but the channels having small position width such as 1 Ch and 2 Ch had the poor accuracy due to the slow slew rate (~1 V/ns) of comparator and logic-components. The channels such as 3 Ch and 7 Ch had lower counts than the neighbor channels because that channels had the low sensor gain. In order to improve the position accuracy, the DEM method required the high speed comparator to reduce the position histogram error and the TDC operating high speed clock in FPGA.

In addition, the current prototype DEM method will be limited by low count per second (CPS) with increasing dead-time caused by delay interval time of 10 ns. The maximum dead time was 80 ns which could block the after pulse. Therefore, the current DEM method will be necessary to reduce the dead-time with short pulse shaping time for improving the sensitivity.

As shown in the energy spectrum, the DEM circuit had the poor energy linearity caused by the exponential decay of scintillation pulse is the major drawback of that. The multi-time-over-threshold (MTOT) method is one of the digitalization method that acquiring time and energy information by measuring arrival time and pulse duration [16−19]. The MTOT method improves the energy linearity by employing multiple triggering threshold as compared with the conventional TOT method using only one threshold.

The CRT of over 2 ns was sufficient performance for non-time of flight PET system such as small animal PET. However, this timing performance had some limitations for time-of-flight PET system required very low CRT (~300 ns).

The developed multiplexing method that reduces the complexity of thousands of readout channels for the PET or gamma-camera has also the potential of replacing ADC. Indeed, the data acquiring device can be simply designed as FPGA by reducing when designing the PET and gamma-camera system through acquirement in only one FPGA for a detector block.

In the further study, we will develop the channel expansion circuit based on the row-column summing readout to improve increasing the number of channels and the dead-time reduction circuit in the logic-network to improve CPS. In addition, the prototype PET system using the DEM method will be developed and evaluated by measuring SNR, spatial resolution in phantom images.

Acknowledgements

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