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Enhancement of energy efficiency of 3-phase inverter using LFS UMOSFET

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Abstract

In this paper, the energy efficiency of a 4H-SiC UMOSFET with a local floating superjunction (LFS UMOSFET) was compared with a conventional P-shielding UMOSFET. For analysis, P-shielding UMOSFET and LFS UMOSFET were modeled for energy loss and junction temperature. As a result, LFS UMOSFET showed switching loss reduction of 20.6%. In addition, it was confirmed that LFS UMOSFET is applied to a 3-phase inverter, resulting in 33.2% lower power efficiency and 28.1% lower junction temperature than P-shielding UMOSFET. Electrical characteristics were simulated using Sentaurus TCAD, and the power circuit was simulated with the modelled UMOSFET using PSIM, a power circuit simulator.

Key words : 4H-SiC, UMOSFET, local floating superjunction, Energy loss, Efficiency

Ⅰ. Introduction

4H-SiC MOSFETs are widely considered to be the leading next-generation power semiconductor devices due to their superior material properties such as high critical electric field, high thermal conductivity, and ability to operate at high temperatures [1-3]. Of the various SiC MOSFET structures, gate-trench MOSFETs (UMOSFETs) typically have lower on-resistance compared to planar MOSFETs (VDMOSFETs) [4]. UMOSFETs have higher channel density and mobility than VDMOSFETs due to their ability to form vertical channels on the trench sidewalls and their ability to reduce cell pitch. However, the biggest problem with UMOSFETs is the appearance of gate oxide reliability issues that arise from the gate oxide at the bottom of the trench when UMOSFET operates in the off-state [5]. Because SiC, a wide bandgap material, has a small offset between the conduction band and the valance band with respect to the SiC and the gate oxide, Fowler Nordheim tunneling (FN tunneling) will occur in the electric field smaller than Si. This FN tunneling current leads to oxide degradation. Therefore, in the case of SiC UMOSFETs, it is important to suppress electric field crowding at the gate oxide edge. To address this problem, the P-shielding UMOSFET has been proposed [2]. Fig. 1-(a) shows the structure of the P-shielding UMOSFET. However, P-shielding causes a few problems in conduction mode. A parasitic JFET region exists between

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the P-base and P-shielding; and the current pathway is reduced due to the expansion of the depletion region between the P-shielding and the N-drift.

4H-SiC UMOSFET with local floating superjunction structure (LFS UMOSFET) (Fig. 1-(b)) is presented [6] to solve above problem. This structure utilizes the existing P-shielding while improving the characteristics of the conduction mode. The Sentaurus TCAD simulation results demonstrated that the LFS UMOSFET has superior properties of on-resistance while maintaining a breakdown voltage that is comparable to the P-shielding UMOSFET [7]. In addition, PSIM simulation results demonstrated an improvement in energy efficiency.

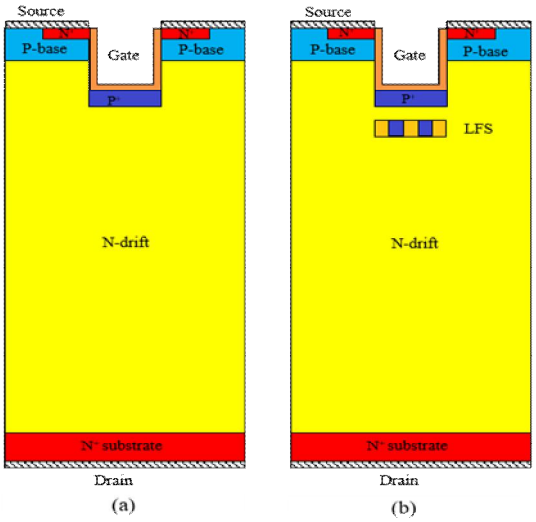


Fig. 1. Schematic cross-sectional views of (a) P-shielding UMOSFET, and (b) LFS UMOSFET.

II. Static characteristic of LFS UMOSFET

1. Device concept

In power devices, the main feature of a conventional superjunction is that the drift region comprises multiple alternate N- and P-stripes with relatively high doping, compared with a single region with low doping. This has a favourable outcome of increasing blocking capability. Thus, the limits of 1-D Poisson theory can be overcome by 2-D Poisson theory. The improved off-state characteristic can compensate for the on-state characteristic by adjusting the drift layer doping concentration [8]. Therefore, by placing a local superjunction beneath the P-shielding, the current pathway is widened, and the on-resistance is lowered by doping higher than the N-drift region. The n-region of both ends of the superjunction can be a current spreading layer with high doping [9]. The p-region of the superjunction can be shielded by redistributing the electric field when operating in blocking mode. Accordingly, the ratio of doping concentration in each region is significant. The optimization process for all device parameters is described in [6], and Table 1 lists values of the parameters.

Table 1. Parameters of the simulation.

Parameters	Value
Cell pitch	5.55 μm
Trench depth	1.5 μm
Trench width	1.5 μm
N-epitaxy layer doping concentration	3 x 10^{15}cm^{-3}
N-epitaxy layer depth	16.5 μm
P-base doping concentration	1 x 10^{17}cm^{-3}
P-base depth	0.7 μm
P-shielding doping concentration	5 x 10^{18}cm^{-3}
P-shielding depth	0.3 μm
Superjunction depth	0.3 μm
Depth between P-shielding and superjunction	0.4 μm
Superjunction doping concentration	2.5 x 10^{17}cm^{-3}

2. Static characteristics

Fig. 2 shows the on-state output characteristics of the two UMOSFETs, where the gate voltage is varied from 2 to 10 V in five steps. The on-resistance of the P-shielding UMOSFET was 13.75 mΩ-cm^2 when the gate voltage was 10 V, and the on-resistance of the LFS UMOSFET was 8.68 mΩ-cm^2, which represents an improvement of 36.86%. The current density was improved owing to the placement of the LFS beneath the P-shield. The superjunction effect reduced the

expansion of the depletion region between the P-shield and the N-drift, thus increasing the current flow pathway in the drift layer, and in turn increasing the maximum current density in the channel [10]. The LFS UMOSFET exhibited a lower on-resistance than the P-shielding UMOSFET, owing to the weaker JFET effect and the reduced drift resistance [11].

Fig. 3 shows the breakdown voltage of the two UMOSFETs. The breakdown voltages of the P-shielding UMOSFET and LFS UMOSFET were 1752 V and 1619 V, respectively. The LFS UMOSFET exhibited a slight decrease in the breakdown voltage in the off-state, with a significant improvement in the on-state characteristics. This is due to the relatively highly doped N-region of the superjunction compared with the N-drift.

Table 2 summarizes the performance of the two UMOSFETs. The higher is the doping concentration, the lower is the on-resistance and breakdown voltage because of the superjunction effect. As indicated in Table 2, when the breakdown voltage is slightly reduced, with a maximum on-resistance current density, an increase in the FOM is observed.

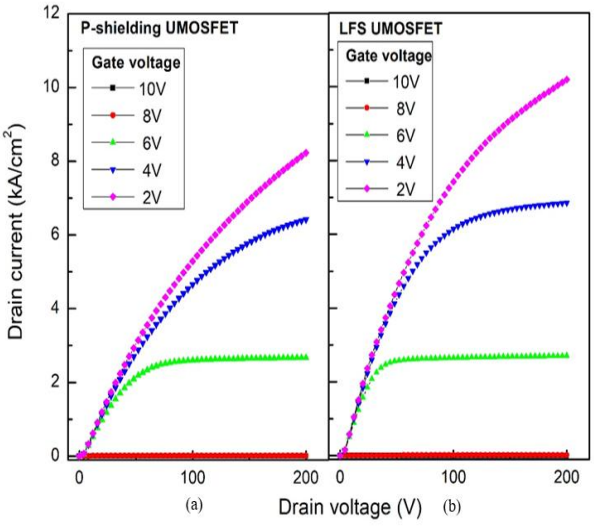


Fig. 2. On-state output characteristics of (a) P-shielding UMOSFET and (b) LFS UMOSFET.

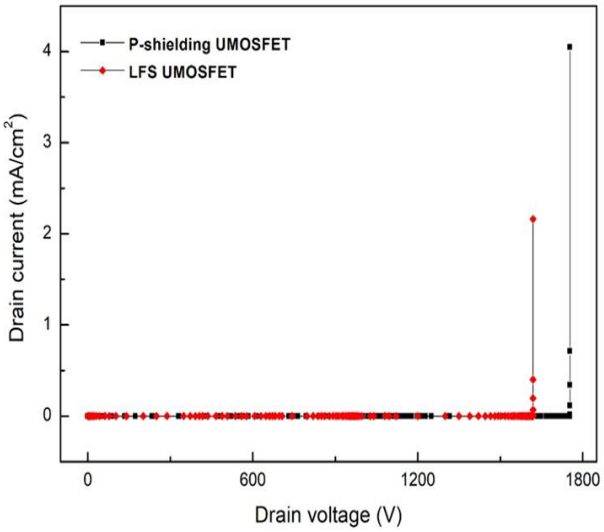


Fig. 3. Off-state characteristic curves of the P-shielding UMOSFET and LFS UMOSFET.

Table 2. Performance of UMOSFETs

Performance parameters	P-shielding UMOSFET	LFS UMOSFET
Breakdown Voltage (V)	1752	1619
$R_{on,sp}$ (mΩ-cm^2)	13.75	8.68
Figure of Merit(FOM) (MW-cm^{-2})	223.38	301.84

III. Switching characteristic of LFS UMOSFET

1. Switching energy loss

The switching characteristics of UMOSFETs were analyzed. Fig. 4-(a) and (b) shows the P-shielding UMOSFET and LFS UMOSFET switching waveforms and test circuit. First, UMOSFETs are assumed to be packages for use with the actual power circuit. The UMOSFET is a packaged device with an active area of 0.34 cm^2. Test conditions included a drain voltage of 1200 V, a gate external resistance of 10 Ω, and a junction temperature of 25 °C. Table 3 summarizes the switching times and energy losses of the two UMOSFETs. The LFS UMOSFETs has longer switching times, but has less total switching energy loss compared to P-shielding UMOSFETs. Because LFS UMOSFET demonstrated a lower turn-off energy loss of 33.6% compared with the

P-shielding UMOSFET. As a result, the LFS UMOSFET has a 20.6% reduction in total switching energy loss from 109.25 to 86.66 respectively compared to P-shielding UMOSFET.

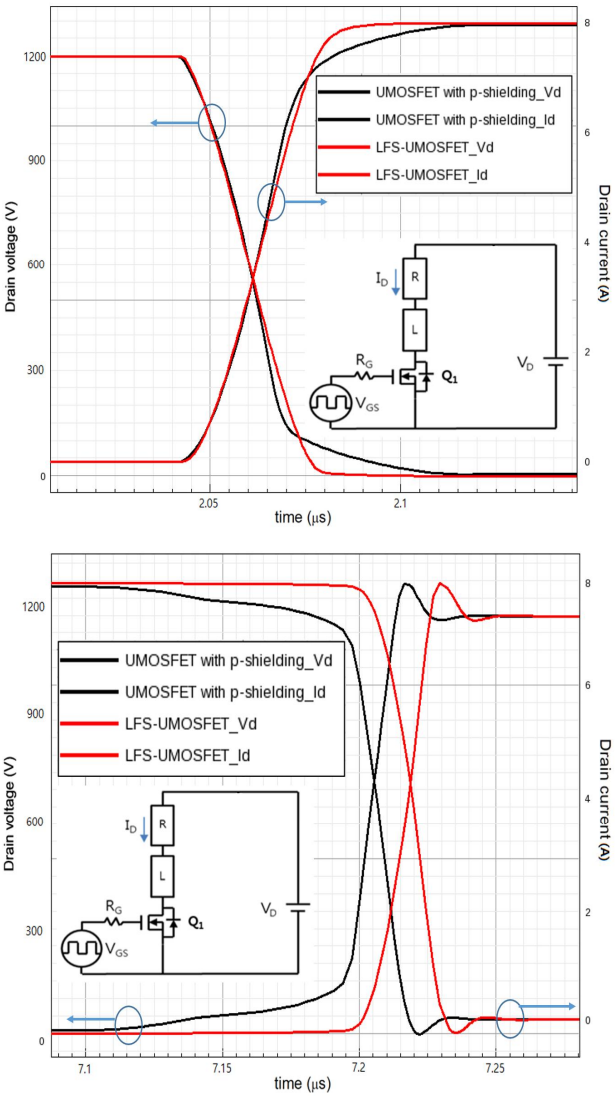


Fig. 4. Switching wave forms of (a) turn-on and (b) turn-off (Test condition: Vg=0~20V, Vd=1200V, Id=8A, Rg=10Ω, T_j=25°C)

Table 3. Switching energy loss characteristic of UMOSFETs

Performance parameter	P-shielding UMOSFET	LFS UMOSFET
T_{ON} (ns)	34.1	34.7
T_{OFF} (ns)	87.4	99.4
E_{ON} (μJ)	32.48	35.72
E_{OFF} (μJ)	76.77	50.94
E_{Total} (μJ)	109.25	86.66

2. Switching energy loss modeling

For a switching device to be used in a power circuit, analysis is required at the power device level. Therefore, it is necessary to estimate the energy loss of the switching device in the actual power circuit and design a suitable device for the power circuit.

Modeling was performed to account for the energy loss improvement of the LFS UMOSFET. Figures 5-8 show the relationship between energy loss and various variables. For PSIM simulation, we have obtained more modeling data for energy loss, but only a few representative data are shown in this paper. In all graphs, the black line represents the P-shielding UMOSFET and the red line represents the LFS UMOSFET. In addition, modelling of junction temperature was also performed in the circuit simulation. Thermal resistance between the junction and the case is taken into account for calculating the junction temperature [12]. The value of thermal resistance between the junction and the case was 1.1 °C/W. The energy loss was proportional to the drain current (Fig. 5), the gate external resistance (Fig. 6) and the drain voltage (Fig. 7, 8). As shown in all graphs, energy loss increased with temperature. [13-14].

The junction temperature was also simulated. In this study, a calculation method was used using the relationship between case temperature and power consumption. The relationship between junction temperature and power consumption can be expressed as

$$T_j = T_C + R_{th(j-c)} \times P \quad (1)$$

T_C is the case temperature, $R_{th(j-c)}$ is the thermal resistance between junction and case, and P is the average power loss. Junction-case thermal resistance $R_{th(j-c)}$ is a value used when a standalone device is fixed to the heat sink. In this case, because the case-heat sink is the main heat dissipation path, the junction temperature can be accurately determined by measuring the

case temperature along this path. Assuming that a heat sink with ideal heat dissipation is used, considering the heat dissipation capacity to infinity, it can be calculated as case temperature=25°C, with case temperature=ambient temperature. Thermal resistance of the heat sink is $R_{th(c-a)}$=0, thus $R_{th(j-a)}$ =$R_{th(j-c)}$ [15].

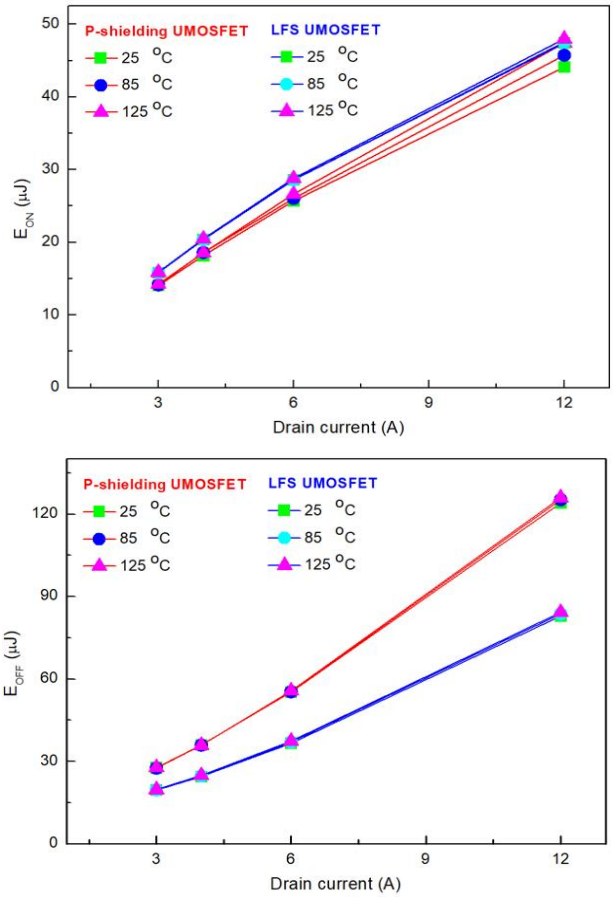
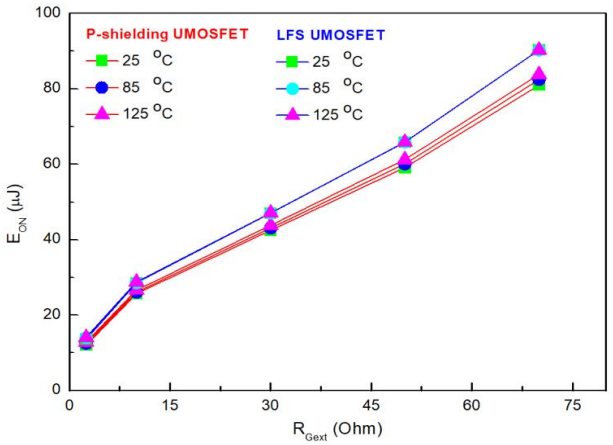


Fig. 5. Energy loss as a function of drain current of (a) turn-on and (b) turn-off (Test condition : Vg=0~20V, Vd=1200V, Rg=10Ω).



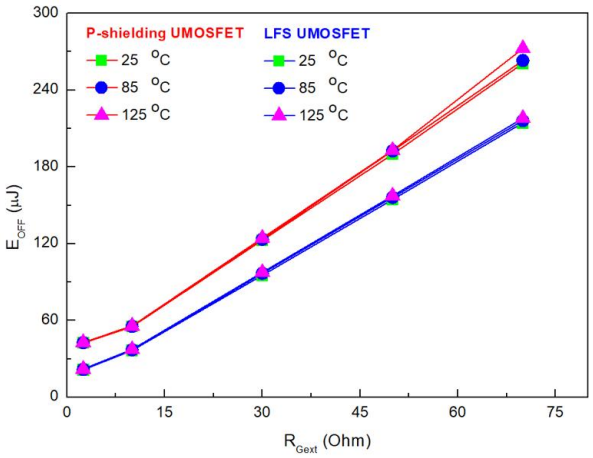


Fig. 6. Energy loss as a function of gate external resistance of (a) turn-on and (b) turn-off (Test condition: Vg=0~20V, Id=6A, Vd=1200V).

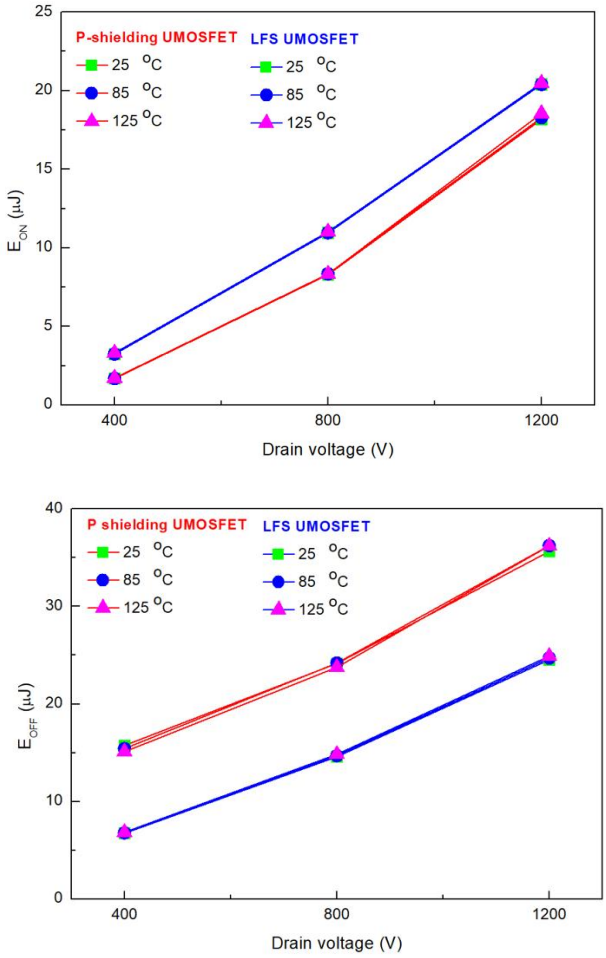


Fig. 7. Energy loss as a function of drain voltage of (a) turn-on and (b) turn-off at Id=4A(Test condition: Vg=0~20V, Rg=10Ω).

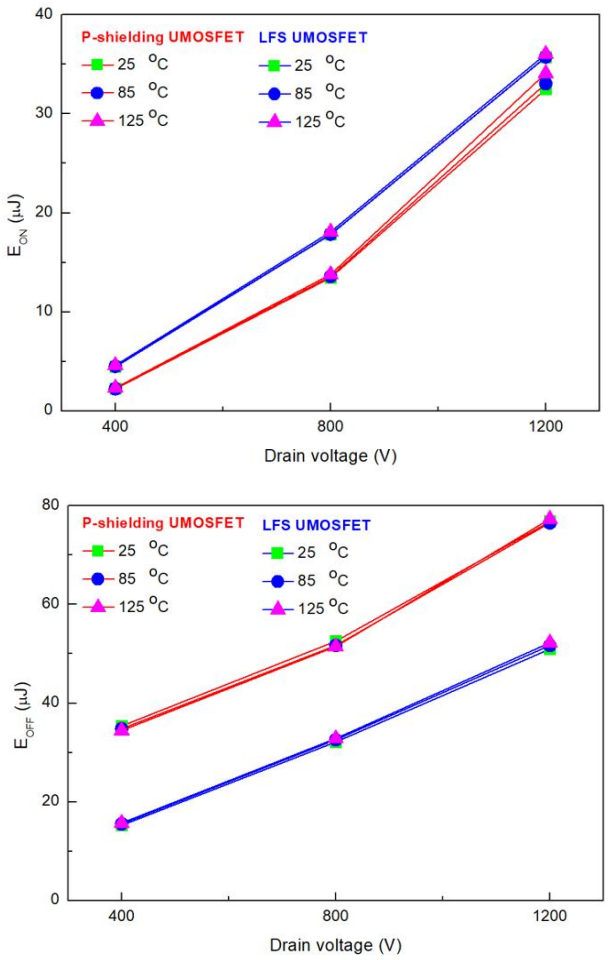


Fig. 8. Energy loss as a function of drain voltage of (a) turn-on and (b) turn-off at Id=8A (Test condition: Vg=0~20V, Rg=10Ω).

IV. 3-phase inverter energy efficiency

3-phase inverters are typically used in electric vehicles. Therefore, to verify the efficiency of the LFS UMOSFET, it was applied to a 3-phase inverter circuit and verified through simulation. Figure 9 shows the 3-phase inverter used in the simulation. 3-phase inverter consisted of an RLC passive element, a diode, six switching UMOSFETs and complementary switches. Inductor (L) and Capacitor (C) serve as filters to remove unnecessary ripple components of the output voltage. Resistor (R) is the load resistance and the output voltage measured. The input voltage was 1000 V, the duty cycle of the gate was 0.5, and as a result, the output voltage was 1000 V (AC). Fig. 10 and 11 show the power loss and junction temperature simulation results of a 3-phase inverter designed with P-shielding UMOSFET and LFS UMOSFET, respectively.

Power losses and junction temperatures at steady state are summarized in Table 4. Table 4 indicates that the LFS UMOSFET has a lower junction temperature and lower power loss than the P-shielding UMOSFET. In the 3-phase inverters using LFS UMOSFET, junction temperature decreased by 28.15%, conduction power losses improved by 31.8% and switching power losses improved by 43.36% compared to the inverter with P-shielding UMOSFET. The total power loss, which is the sum of the conduction power loss and the switching power loss, was improved by 33.23%. In addition, junction temperature measurements for power dissipation provide reliability verification at the circuit level, enabling predictive design of devices.

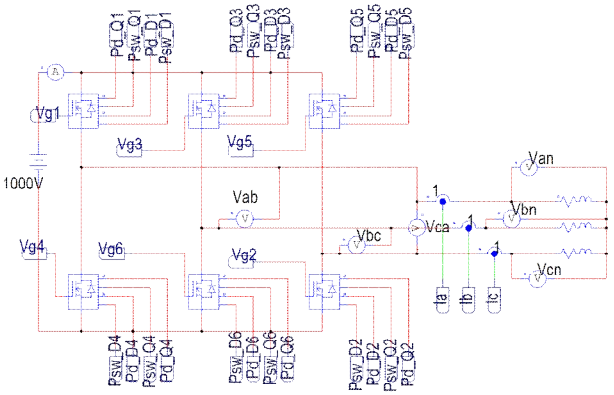
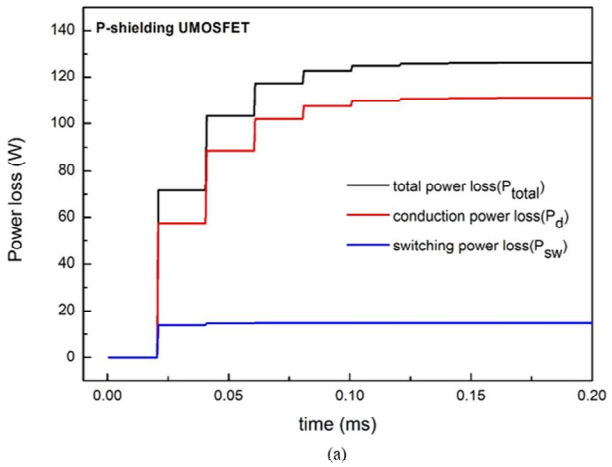


Fig. 9. 3-phase inverter circuit for PSIM simulation.



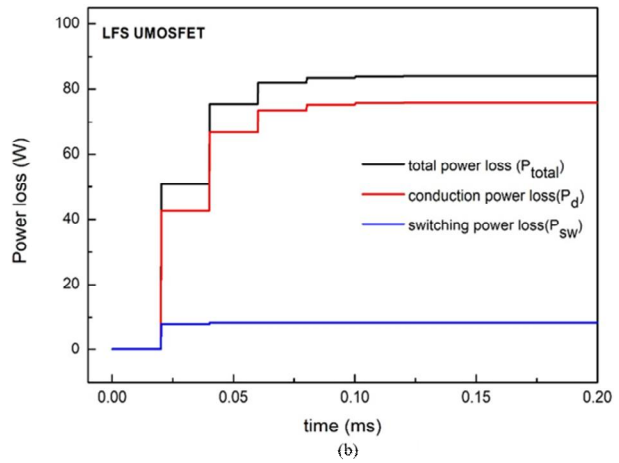


Fig. 10. Power loss of (a) P-shielding UMOSFET (b) LFS UMOSFET.

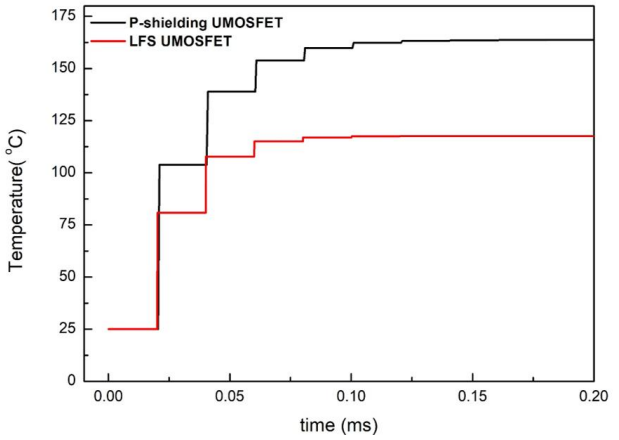


Fig. 11. Junction temperature of UMOSFETs.

Table 4. Summary of efficiency for 3-phase inverter.

3-phase inverter	P-shielding UMOSFET	LFS UMOSFET
T_j (℃)	34.1	34.7
P_d (W)	87.4	99.4
P_{SW} (W)	32.48	35.72
P_{total} (W)	76.77	50.94

V. Conclusion

This study investigated a 4H-SiC UMOSFETs with a breakdown voltage of 1700 V. The on-state and off-state characteristics were improved by incorporating a local floating superjunction in the P-shielding UMOSFET. The LFS UMOSFET provided a low on-resistance while maintaining the breakdown voltage. The LFS UMOSFET exhibits an on-resistance reduction of 36.8%, and a 35.1% increase in the FOM compared with the P-shielding UMOSFET. This is an improvement in the efficiency of conduction power loss. The presence of the superjunction around the shielding increased the suppression of the JFET effect between the P-base and the P-shield and the current flow pathway in the N-drift region. The local p-region of the superjunction helped mitigate the electric field crowding at the P-shielding edge, providing a better trade-off between the on-resistance and the breakdown voltage. In addition, UMOSFETs were modelled with energy loss. The LFS UMOSFET have a lower power loss of 33.23% compared with the P-shielding UMOSFET. In addition, the reduction of the junction temperature by 28.15% makes the cooling system smaller and thus higher integration efficiency.

References

[1] B. J. Baliga, *Fundamentals of Power Semiconductor Devices,* USA: Springer, 2008.

[2] B. J. Baliga, *Advanced power MOSFET concepts*, USA: Springer, 2010.

[3] B. J. Baliga, *Silicon Carbide Power Devices*, USA: Springer, 2006.

[4] R. S. Saxena and M. J. Kumar, "Trench gate power MOSFET: Recent advances and innovations," in *Advances in Microelectronics and Photonics. Commack,* ch.1, pp.1-23, 2012.

[5] C. Hu and Q. Lu, "A unified gate oxide reliability model," *IEEE International Reliability Physics Symposium Proceeding*, pp.47-51, 1999. DOI: 10.1109/RELPHY.1999.761591

[6] J. Goh and K. Kim. "Low on-resistance 4H-SiC UMOSFET with local floating superjunction," *Journal of Computational Electronics*, Vol.19, No.1, pp.234-241, 2020.
DOI: 10.1007/s10825-019-01408-1

[7] T.C.A.D. Synopsys Sentaurus Device Manual

Synopsys, Inc, Mountain View, CA, USA, 2012.
[8] F. Udrea, G. Deboy, T. Fujihira, "Superjunction power devices history development and future prospects," I*EEE Trans. Electron Devices*, vol.64, no.3, pp.713-727, 2017. DOI: 10.1109/TED.2017.2658344
[9] K. Tian, J. Liu, J. Cui, C. Zhou, A. Zhang, "Novel designs of 4H-SiC trench gate metal-oxide-semiconductor field effect transistors (UMOSFETs) with low on-resistance," *2016 13th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China* (SSLChina: IFWS), pp.35-37, 2016.
DOI: 10.1109/IFWS.2016.7803750
[10] X. Zhou, R. Yue, J. Zhang, et al, "4H-SiC trench MOSFET with floating/grounded junction barrier-controlled gate structure," *IEEE Transactions on Electron Devices*, Vol.64, No.11, pp.4568-4574, 2017. DOI: 10.1109/TED.2017.2755721
[11] S. Harada, Y. Kobayashi, K. Ariyoshi, T. Kojima, et al, "3.3kV-class 4H-SiC MeV-implanted UMOSFET with reduced gate oxide field," *IEEE Electron Device Lett.,* vol.37, no.3, pp.314-316, 2016. DOI: 10.1109/LED.2016.2520464
[12] P. Szabo, O. Steffens, M. Lenz, G. Farkas, "Transient junction-to-case thermal resistance measurement methodology of high accuracy and high repeatability," *IEEE Transactions on Components and Packaging Technologies*, Vol.28, No.4, pp. 630-636, 2005. DOI: 10.1109/TCAPT.2005.859768
[13] D. Graovac, M. Purschel, A. Kiep, "MOSFET power losses calculation using the data-sheet parameters, Infineon application note," Vol.1, pp. 1-23, 2006.
[14] X. Li, L. Zhang, S. Guo, Y. Lei, A. Q. Huang, B. Zhang, "Understanding switching losses in SiC MOSFET: Toward lossless switching," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, pp. 257-262, 2015. DOI: 10.1109/WiPDA.2015.7369295
[15] "Junction Temperature," Rohm technical support, 2019.
https://www.rohm.com/electronics-basics/transistors/calculating-transistor-temperature

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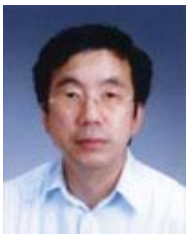

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