Journal of Semiconductor Engineering Vol. 1, Issue 2, September 2020
https://doi.org/10.22895/jse.2020.0006
Received 13 August 2020, Accepted 2 September 2020 ISSN(On-line) 2733-6719

Time-Domain Analog Signal Processing Techniques

Jin-Gyu Kang[1], Kyungmin Kim[2], and Changsik Yoo[1]

[1] Department of Electronic Engineering, Hanyang University, Seoul 04763, South Korea
[2] DRAM Design Team, Samsung Electronics, Hwaseong, Kyonggi-do 18450, South Korea

Corresponding Author: Changsik Yoo (csyoo@hanyang.ac.kr)

Funding Information: This research was supported by the Samsung Research Funding Center of Samsung Electronics under Project Number SRFC-IT1501-52 and by the Samsung Future Interconnect Technology Cluster Program.

ABSTRACT

As CMOS technology scales down, the design of analog signal processing circuit becomes far more difficult because of steadily decreasing supply voltage and smaller intrinsic gain of transistors. With sub-1V supply voltage, the conventional analog signal processing relying on high-gain amplifiers is not an effective solution and different approach has to be sought. One of the promising approaches is "time-domain analog signal processing" which exploits the improving switching speed of transistors in a scaled CMOS technology. In this paper, various time-domain analog signal processing techniques are explained with some experimental results.

KEY WORDS

Amplifier, analog circuits, analog filter, CMOS, data converter, operational amplifier, power-management integrated circuit (PMIC), time-domain analog signal processing.

1. INTRODUCTION

The rapid advances of semiconductor technologies have been and will be the driving force for the proliferation of electronic devices and information technology. Fueled by the demands for even better performance, complementary metal-oxide-semiconductor (CMOS) technologies are evolving into sub-10-nm gate length and sub-1-V supply voltage era. With scaled-down CMOS technologies, more functionalities can be integrated on an integrated circuit (IC) with improved performance, allowing the lower cost implementation of an information processing system [1].

Although humans perceive information in analog manner (no quantization and no sampling), information processing is performed mostly by digital systems because digital signal processing offers lots of advantages such as the ease of information storage, flexibility and programmability of signal processing and computing, and immunity to noise and error. Even if the information processing is performed by a digital system, there must be analog circuits preceding and following the digital system for the conversion to and from analog and digital signals and signal conditioning in between. Unlike digital systems, analog circuits cannot fully benefit from scaled-down CMOS technologies and it becomes more challenging to achieve the same performance with smaller feature size and lowered supply voltage because the advance of CMOS technologies has been geared towards the optimum performance of digital systems [1]-[3].

In analog circuits, information is represented as either current or voltage level among which the latter is the usual selection. With the lowered supply voltage of scaled-down CMOS technologies, the dynamic range (DR) of an analog signal is reduced proportionally as shown in Figure 1 and the noise level of analog circuits has to be reduced to maintain the same signal-to-noise ratio (SNR). The equivalent noise power spectral density (PSD) referred to the gate of a transistor is given as;

$$\overline{v_{ng}^2} = 4kT\left(\frac{2/3}{g_m} + \frac{K}{c_{OX}WLf}\right) \quad (1)$$

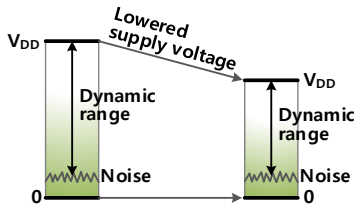


Figure 1. Reduced dynamic range of voltage signals in scaled-down CMOS technologies.

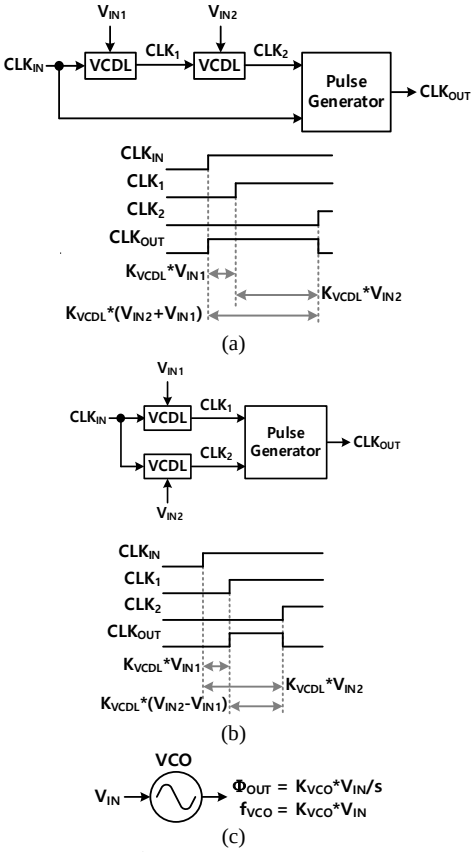


Figure 2. Examples of time-domain analog signal processing; (a) addition, (b) subtraction, and (c) integration.

where g_m is the transconductance, c_{OX} is the gate-oxide capacitance, W is the channel width, and L is the channel length of the transistor. The first-term of the equation (1) is the thermal noise which is inversely proportional to the DC bias current of the transistor and therefore more power has to be consumed for a high SNR, negating the advantage of the low-voltage operation in scaled-down CMOS technologies. The second-term of the equation (1) is the flicker noise whose magnitude is inversely proportional to the product of W and L all of which become smaller in scaled-down CMOS technologies. For smaller flicker noise, the channel length and width have to increased, negating the advantage of the small area of scaled-down CMOS technologies once again.

The intrinsic gain of MOS transistors becomes smaller as CMOS technologies scale down because of the shorter channel length. Moreover, the gain-enhancement by stacking more number of transistors between the supply rails is not easy because of the lowered supply voltage. Therefore, the conventional amplifier-based analog signal processing becomes very challenging.

The reduced DR of analog signals in scaled-down CMOS technologies can be attributed to the representation of analog signals with voltage level while the supply voltage has to be lowered for device reliability. The reduction of DR due to the shrinking voltage headroom can be coped with by employing a current-mode approach [4]. For current-mode analog signal processing, however, the signal nodes of analog circuits should have low impedance, requiring large branch current and subsequently high power consumption. Therefore, the current-mode approach is not a suitable choice to overcome the lowered DR in scaled-down CMOS technologies.

The improving switching speed of MOS transistors offers an excellent timing accuracy and therefore the time resolution can easily surpass the voltage resolution in scaled-down CMOS technologies. If an analog signal is represented as a time stamp, its DR is not limited by the lowered supply voltage and may even increase in scaled-down CMOS technologies. Also, we do not need any high-gain voltage amplifiers because analog signals represented as time-stamps can be processed in the time-domain. Therefore, time-domain signal processing is gaining popularity in designing high-performance analog circuits. In this paper, various time-domain analog signal processing techniques are reviewed.

2. BASIC CONCEPT

The key feature of the time-domain analog signal processing is the representation of analog signals as time stamps. Analog signals represented as time stamps are processed by various kinds of timing circuits such as delay line, oscillator, and so on. Figure 2 shows several examples of time-domain analog signal processing circuits. The addition and subtraction can be performed with voltage controlled delay lines (VCDL) and a voltage controlled oscillator (VCO) can perform the integration exploiting its voltage-to-phase integration property.

The biggest advantage of a VCO-based integrator is its infinite DC gain while it is not trivial to have larger than 40-dB DC gain with an amplifier-based integrator in scaled-down CMOS technologies. Because a VCO-based integrator transforms analog signals from the voltage-domain to the time-domain, the signal DR becomes independent of the lowered supply voltage in scaled-down CMOS technologies, which is another advantage of a VCO-based integrator. The VCO-based integrator can be employed in analog circuits requiring power-hungry amplifier-based integrators to reduce the power consumption and avoid the challenges for achieving high DR. The promising nature

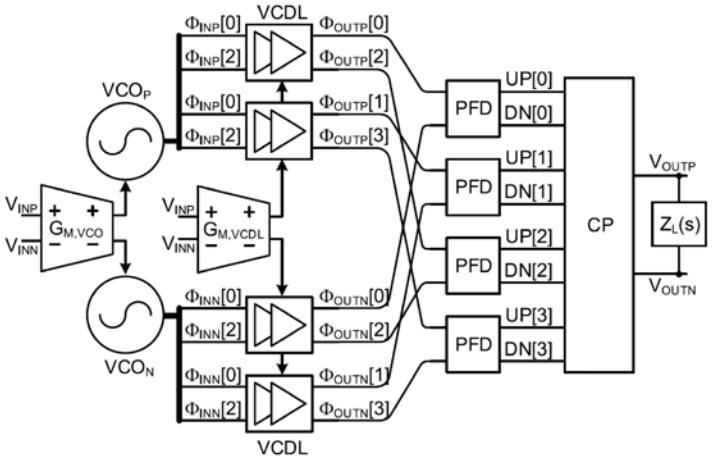


Figure 3. Operational amplifier emulated by time-domain circuits.

of a VCO-based integrator can be utilized to realize a time-domain oversampling analog-to-digital converter (ADC) and/or time-domain analog filter by replacing analog integrators with time-domain ones.

The different form of the input (voltage or current) and output (clock phase) of a VCO-based integrator hinders the design of a fully time-domain oversampling ADC and analog filter. For oversampling ADC and analog filter, amplifier-based active analog filters and/or resistor-capacitor-based passive filters are often still required. Among multiple integrators of a high-order sigma-delta modulator, usually only the last one can be replaced with a VCO-based integrator. Therefore, for fully time-domain oversampling ADC and analog filter, a conversion technique to and from voltage level and clock phase has to be developed or a totally different form of time-domain integrator has to be devised that can be cascaded in series without any conversion between the two different signal forms.

The integrating nature of a VCO can also be utilized for various control networks such as the proportional-integral-derivative (PID) controller of a switching DC-DC converter. Although a digital PID controller is a popular choice to replace an area- and power-hungry analog PID controller in switching DC-DC converters, an ADC is required to sample and feedback the output level of a switching DC-DC converter, which may be a big burden.

3. OPERATIONAL AMPLIFIER EMULATED BY TIME-DOMAIN CIRCUITS

The performance of an operational amplifier (op-amp) based analog signal processing circuit is determined by the open-loop gain and the bandwidth (BW) of op-amp. For this, various techniques such as cascading of high-gain amplifiers and/or cascoding of transistors are employed in conventional voltage-domain operational amplifier. The cascading of high-gain amplifiers and cascoding of transistors, however, result in high power consumption, reduced DR, and lowered BW. Moreover, it becomes much more difficult to follow this design approach in scaled-down CMOS technologies.

The voltage-to-phase integration property of a VCO can be exploited to implement an op-amp with infinite DC-gain. The output of a VCO appearing as the phase of a clock signal, however, has to be converted to a voltage level for the VCO to be used as op-amp. Figure 3 shows the time-domain op-amp developed by the authors [5]. The differential input V_{INP} and V_{INN} are used as the control voltages of the VCOs and the voltage controlled delay line (VCDL). The frequencies of the VCOs are controlled by the differential output current of the transconductor $G_{M,VCO}$ and therefore the frequencies of VCO_P and VCO_N are proportional to $V_{INP} - V_{INN}$ and $V_{INN} - V_{INP}$, respectively. The delays of the four VCDLs are controlled by the differential output current of the transconductor $G_{M,VCDL}$. The quadrature-phase output clocks $\Phi_{INP}[0:3]$ and $\Phi_{INN}[0:3]$ of the VCOs are applied to the VCDLs to get the clocks $\Phi_{OUTP}[0:3]$ and $\Phi_{OUTN}[0:3]$ whose phases are compared with each other by the four phase-frequency detectors (PFD). The outputs $UP[0:3]$ and $DN[0:3]$ of the PFDs are applied to the charge-pump (CP) which pumps differential current to the load $Z_L(s)$ to get the differential voltage output V_{OUTP} and V_{OUTN}. For the load impedance $Z_L(s)$ at the differential output, the gain of the proposed time-domain op-amp can be written as;

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \left(\frac{K_{VCO}}{s} + K_{VCDL}\right) \cdot \frac{N \cdot I_{CP}}{2\pi} \cdot Z_L(s) \quad (2)$$

where N is the number of clock phases (= 4 in the quadrature-phase architecture), K_{VCDL} is the voltage-to-phase gain of the VCDL and I_{CP} is the pumping current of the CP. Due to the infinite DC-gain of the voltage-to-phase transfer characteristic of the VCO, the time-domain op-amp can also have very large DC-

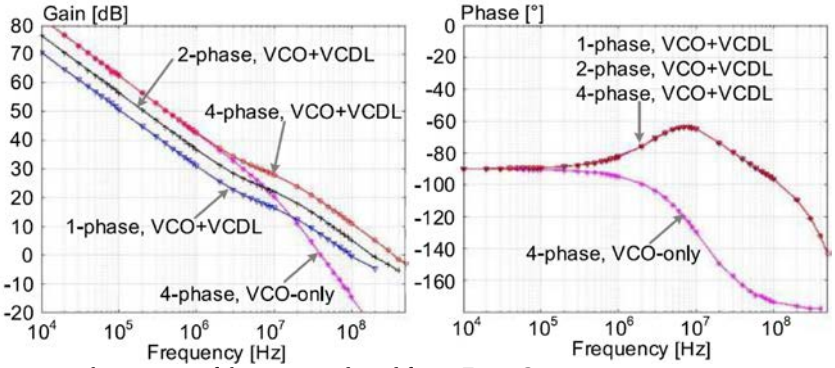


Figure 4. Open-loop frequency characteristic of the operational amplifier in Figure 3.

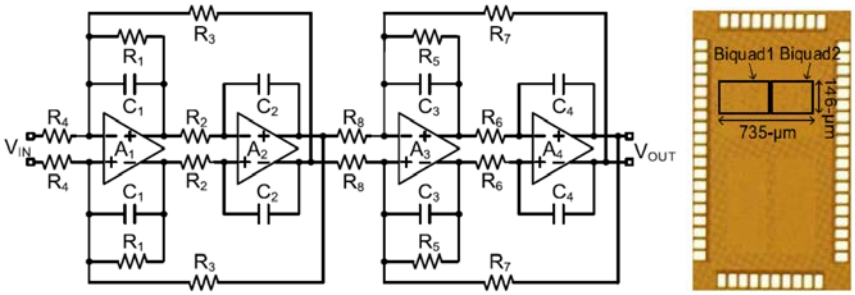


Figure 5. Fourth-order analog filter implemented with the operational amplifier in Figure 3 and its chip microphotograph.

gain. As can be seen in (2), the time-domain op-amp has two or more poles, one at the DC due to the VCO itself and the others due to the load impedance $Z_L(s)$. Therefore, the phase margin has to be ensured by frequency compensation. In [6], a series-connected RC-network at the output creates a left-half plane (LHP) zero for the frequency compensation of a time-domain op-amp. The RC-network at the output, however, generates additional pole and changes the pole frequency created by $Z_L(s)$. In the proposed time-domain op-amp, a LHP zero is generated by the VCDL at $s = -K_{VCO}/K_{VCDL}$ which does not create additional pole and have any impact on the pole by $Z_L(s)$.

Because the differential output voltage V_{OUTP} and V_{OUTN} is generated by comparing the phases of the output $\Phi_{OUTP}[0:3]$ and $\Phi_{OUTN}[0:3]$ of the VCDLs, there is inherent sampling operation of the differential input V_{INP} and V_{INN} in the time- domain op-amp. The sampling rate of the time-domain op-amp is equal to the oscillation frequency of the VCO and may limit the achievable gain and BW of the time-domain op-amp. For the op-amp to have high gain and BW, it is required to increase the sampling rate and thus the oscillation frequency of the VCO, meaning large power consumption. In this work, the effective sampling rate is four times larger than the oscillation frequency of the VCO because the differential input V_{INP} and V_{INN} is sampled by the quadrature-phase clocks.

Figure 4 shows the simulated frequency characteristic of the time-domain op-amp. We performed transient simulation at circuit level with a small amplitude single-tone sinusoidal input for different frequencies. The ratio of the output amplitude to that of the input is calculated to get the gain at each frequency and the delay from the input to the output is used to get the phase response. The gains K_{VCO} and K_{VCDL} of the VCO and the VCDL are 9.73 Grad/s/V and 135.6 rad/V, respectively and the CP current I_{CP} is 200 μA. To see the effect of the multi-phase architecture and the frequency compensation by the VCDL, the frequency responses of four configurations are plotted. As can be seen in the figure, multi-phase architecture allows the time-domain op-amp to have larger DC-gain and BW and the VCDL creates a LHP zero, compensating the frequency response. The unity-gain BW and phase margin of the time-domain op-amp with the quadrature-phase architecture are 350 MHz and 54°, respectively while the time-domain op-amp built only VCO has the phase margin of 15°.

With the time-domain op-amp, the fourth-order low-pass filter (LPF) has been implemented in a 65 nm CMOS technology as shown in Figure 5. The LPF occupies 0.107 mm^2 active silicon area. The time-domain op-amp consumes 2.2 mA from a 0.9 V supply and thus the total power consumption of the LPF is 8.2 mW. From the measured frequency response shown in Figure 6, the cut-off frequency is 25 MHz and the in-band ripple is less than +/-0.3 dB. The nominal oscillation frequency of the VCO is 600 MHz and thus the effective sampling rate of the time-domain op-amp is 2.4 GS/s with the quadrature-phase architecture. As shown in Figure 7(a) and (b), the measured in-band

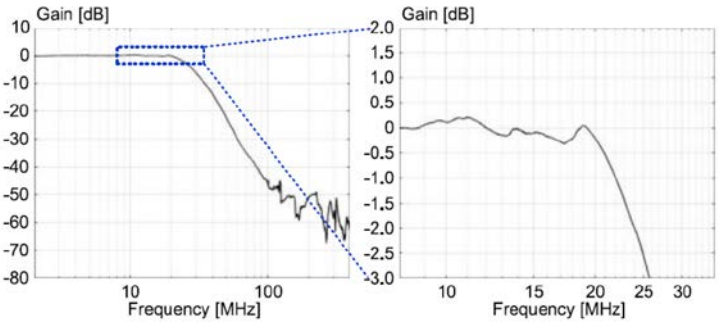
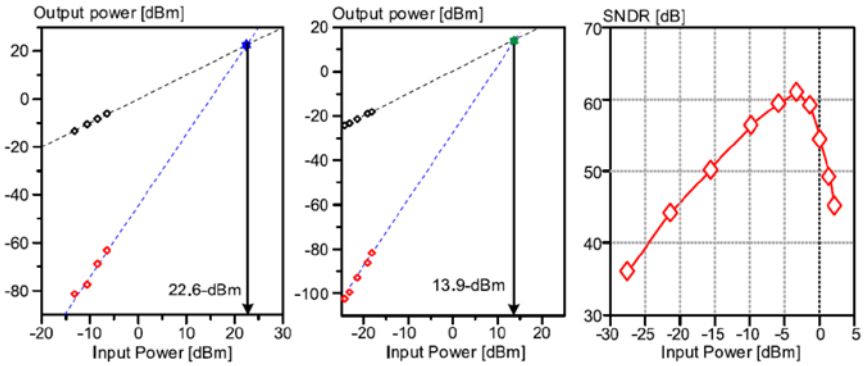


Figure 6. Measured frequency characteristic of the forth-order analog filter.



(a) (b) (c)

Figure 7. (a) In-band and (b) out-of-band input third-order intercept points and (c) SNDR versus the input power.

and out-of-band input third-order intercept points (IIP3) of the LPF are 22.6 dBm and 13.9 dBm, respectively. The signal-to-noise+distortion ratio (SNDR) is plotted versus the input signal magnitude in Figure 7(c) and the peak SNDR is 60.9 dB.

4. CURRENT-MODE BUCK CONVERTER WITH TIME-DOMAIN CONTROLLER

In a modern electronic system, multiple supply voltages with different levels are usually required to achieve the optimum trade-off between power consumption and performance. For efficient generation of required supply voltage levels, switching DC-DC converter is widely used. Although switching DC-DC converter has been around for a long time, its control scheme is relying on the continuous or sampled output voltage [7]-[8]. The control of a switching DC-DC converter with its continuous or sampled output voltage necessitates op-amp based analog control circuitry and/or ADC, which is not an efficient solution in terms of power and silicon area in a scaled-down CMOS technology. Recently, several time-domain control schemes of switching DC-DC converter were proposed [9]-[11]. The time-domain controllers consist of only time-domain circuits such as VCOs, VCDLs, and phase detectors (PD). Because time-domain controllers do not use any wide-BW error amplifier, voltage comparator, and passive RC filter required for conventional voltage-domain controllers, they consume much less power and occupy smaller silicon area.

Current-mode DC-DC converters shown in Figure 8(a) offer various advantages over voltage-mode DC-DC converters such as much simpler frequency compensation, automatic over-current protection, and faster transient response. For current-mode control, however, an accurate inductor current sensor is required which can be very sensitive to noise. Another concern in designing a current-mode DC-DC converter is the instability under certain operating conditions known as subharmonic oscillation. A peak-current-mode buck converter, for example, may become unstable when its switching duty cycle is larger than 50% and slope compensation is required to ensure stable operation.

The time-domain current-mode controller shown in Figure 8(b) eliminates the need for an inductor current sensor and prevent sub-harmonic oscillation. Because the time-domain controller does not use voltage comparators, the switching duty cycle is not limited by the delay of the voltage comparator and can range from 8.5 % to 93 % for the 10 MHz current-mode buck converter, resulting in an output voltage range of 0.15 V to 1.69 V from 1.8 V input [11]. The PD of the time-domain controller replaces the voltage comparator of conventional voltage-domain controller and provides the switching signal V_{PWM} whose pulse width is proportional to the phase difference between the clocks CLK_{SET} and CLK_{RST}. The error voltage $V_{OUT} - V_{REF}$ is applied to the control ports of VCO1 and VCDL. Therefore, the phase ϕ_{SET} of CLK_{SET} is the sum of the integral term provided by VCO1 and the proportional

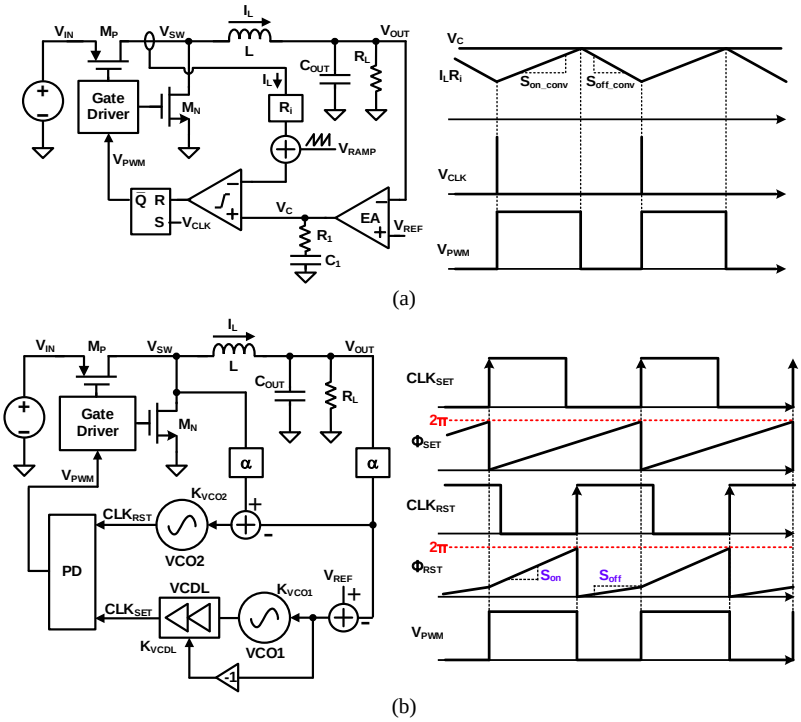


Figure 8. Current-mode buck converter with (a) the conventional voltage-domain controller and (b) the proposed time-domain controller.

term provided by VCDL of the error voltage $V_{OUT}-V_{REF}$ and can be written as;

$$\phi_{SET}(s) = \frac{\omega_{O1} - K_{VCO1}\cdot(V_{OUT}-V_{REF})}{s} + K_{VCDL}\cdot(V_{OUT}-V_{REF}) \quad (3)$$

where ω_{O1} is the free-running frequency of VCO1, K_{VCO1} is the VCO gain of VCO1, and K_{VCDL} is the voltage-to-delay gain of VCDL. The proportional term $K_{VCDL}\cdot(V_{OUT}-V_{REF})$ generates a zero to stabilize the feedback loop like the resistor R_1 of the conventional voltage-domain controller. Because the frequency of VCO2 is proportional to the voltage $V_{SW}-V_{OUT}$ across the inductor, the phase ϕ_{RST} of CLK_{RST} is given as;

$$\phi_{RST}(s) = \frac{\omega_{O2} + K_{VCO2}\cdot(V_{SW}-V_{OUT})}{s} \quad (4)$$

where ω_{O2} is the free-running frequency of VCO2, and K_{VCO2} is the VCO gain of VCO2. As can be seen in (4), the phase ϕ_{RST} of CLK_{RST} is proportional to the integral of the voltage $V_{SW}-V_{OUT}$ across the inductor, which means VCO2 performs the inductor current sensing. Figure 8(b) shows the operation waveforms of the clock signals CLK_{SET} and CLK_{RST} and their phases ϕ_{SET} and ϕ_{RST} at steady-state. Because V_{OUT} is equal to V_{REF} at steady state, the phase ϕ_{SET} of CLK_{SET} increases from 0 to 2π with the constant slope of ω_{O1} as can be seen in the equation (3) and Figure 8(b).

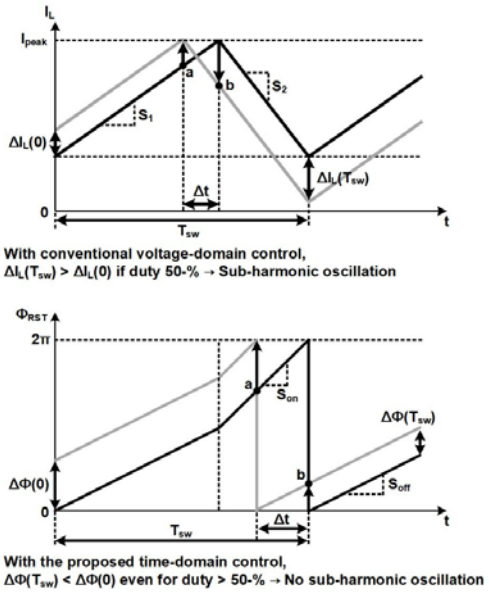


Figure 9. Sub-harmonic oscillation problem in a current-mode buck converter.

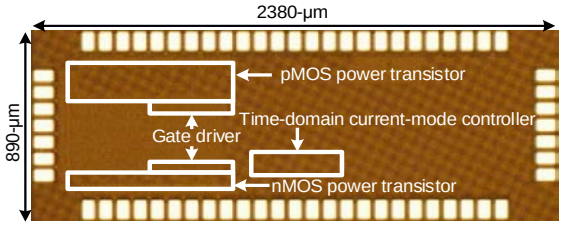


Figure 10. Chip microphotograph of the current-mode buck converter with the proposed time-domain controller.

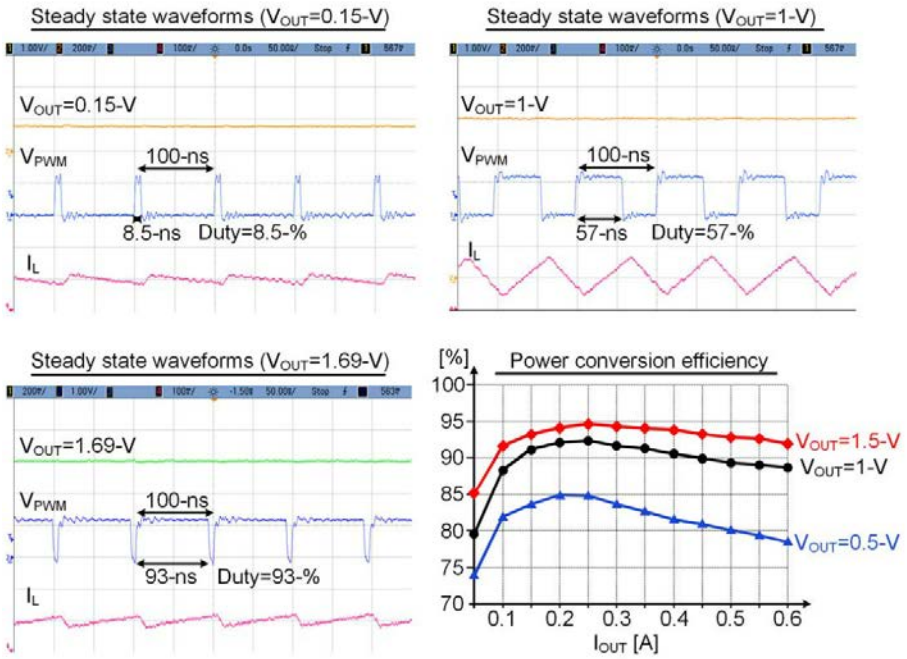


Figure 11. Measured operating waveforms at the steady state and the power conversion efficiency versus the load current.

The phase ϕ_{RST} of CLK_{RST} increases with the different slopes S_{on} and S_{off} depending on the switch voltage V_{SW}. With the voltage-domain peak current-mode control, a perturbation of inductor current becomes larger over time as shown in Figure 9, which is called the sub-harmonic oscillation. To prevent this, slope compensation is required with an external ramp signal V_{RAMP} as shown in Figure 8(a). On the contrary, the proposed time-domain current-mode controller does not have the sub-harmonic oscillation problem even without slope compensation. Assuming the perturbation $\Delta I_L(0)$ of the inductor current appears as a variation $\Delta\phi(0)$ of ϕ_{RST} as shown in Figure 9, the variation of ϕ_{RST} becomes $\Delta\phi(T_{SW})$ after one switching cycle. Denoting the variation of the switch-ON time by the phase variation $\Delta\phi(0)$ as Δt, $\Delta\phi(0)$ and $\Delta\phi(T_{SW})$ can be written as $S_{on}\cdot\Delta t$ and $S_{off}\cdot\Delta t$, respectively. From the equation (4), the ramping slopes S_{on} and S_{off} of ϕ_{RST} are given as;

$$S_{on} = \omega_{O1} - K_{VCO2}\cdot(V_{IN} - V_{OUT}) \quad (5)$$

$$S_{off} = \omega_{O2} - K_{VCO2}\cdot V_{OUT} \quad (6)$$

Because the input V_{IN} is larger than the buck converter output V_{OUT}, S_{on} is larger than S_{off} and $\Delta\phi(T_{SW}) = S_{off}\cdot\Delta t$ is smaller than $\Delta\phi(0) = S_{on}\cdot\Delta t$ even when the switching duty cycle is larger than 50%. This means the variation of the phase ϕ_{RST} resulting from the perturbation of inductor current decreases over time and the subharmonic oscillation is prevented if employing the proposed time-domain current-mode control.

The current-mode buck converter with the proposed time-domain controller has been implemented in a 65 nm CMOS process and the chip microphotograph is shown in Figure 10. The measured switching duty cycle ranges from 8.5% to 93%, allowing the converter to regulate the output from 0.15 V to 1.69 V from an input voltage of 1.8 V. The measured waveforms are shown in Figure 11 for various switching duty cycles and the power conversion efficiency versus the load current I_{OUT} is shown in the same figure as well. The peak power efficiency is 94.9 % when the load current is 250 mA and the output is 1.5 V.

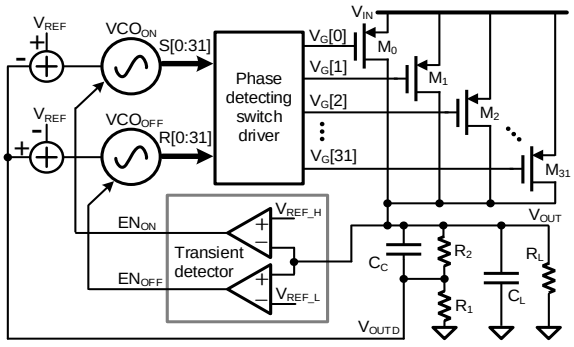


Figure 12. Digital LDO regulator with time-domain controller.

5. LOW-DROPOUT REGULATOR WITH TIME-DOMAIN CONTROLLER

Digital low-dropout (LDO) regulator is gaining popularity for its excellent process scalability and ease of frequency compensation [12]-[16]. The transient response of a conventional digital LDO regulator, however, is limited by its clock frequency because the output voltage level is compared with a reference level

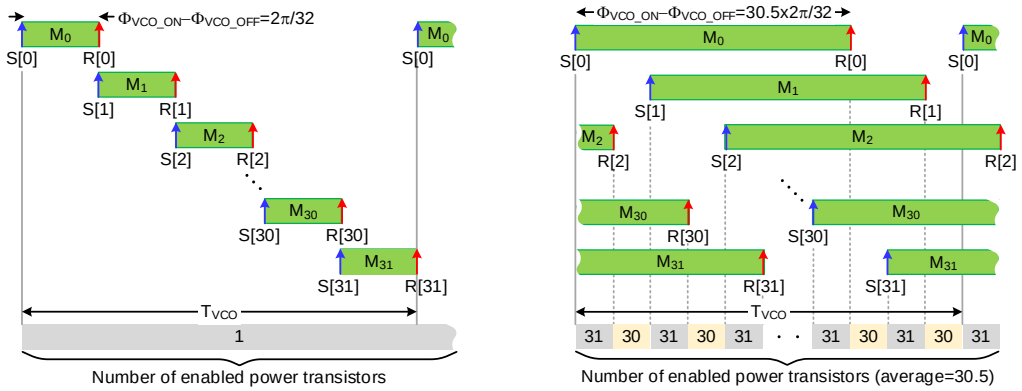


Figure 13. Rising edges of S[0:31] and R[0:31] and the ON-times of the power transistors shown as shaded rectangles with transistor names when the phase error Φ_{ERR} is (a) $2\pi/32$ and (b) $30.5x2\pi$.

and corrected only once per clock cycle. Higher clock frequency and/or multi-bit quantization of the output by an ADC can improve the transient response but at the cost of poor power efficiency. For fast transient response without ADC, complex digital control logic is required.

With the VCO-based time-domain controller shown in Figure 12, the digital LDO regulator has (1) fractionally controlled strength of power transistor, (2) fast transient response, and (3) small output voltage ripple [17]. Only two VCOs (VCO_{ON} and VCO_{OFF}) and a phase detecting switch driver (PDSD) are required for the time-domain control. During the normal operation, the enable signals EN_{ON} and EN_{OFF} of the VCOs are all "1" to enable their oscillation. The oscillation frequencies of VCO_{ON} and VCO_{OFF} are proportional to $V_{REF}-V_{OUTD}$ and $V_{OUTD}-V_{REF}$, respectively where V_{OUTD} is the scaled output and V_{REF} is the reference. The PDSD detects the phase difference between S[0:31] of VCO_{ON} and R[0:31] of VCO_{OFF} and generates the gate driving signals V_G[0:31] of the power transistors M_0~M_{31}. Denoting the phases of S[0:31] and R[0:31] as Φ_{VCO_ON} and Φ_{VCO_OFF}, respectively, the pulse widths of V_G[0:31] are proportional to $\Phi_{ERR}=\Phi_{VCO\_ON}-\Phi_{VCO\_OFF}$. At the rising edge of S[k], V_G[k] is pulled down to turn on the power transistor M_k and pulled up at the rising edge of R[k] to turn off M_k. Therefore, the ON-time of the power transistors is proportional to Φ_{ERR} which is a function of the output V_{OUT} and the load current I_{OUT}. The capacitor C_C generates a zero to ensure the stability of the control loop which has two poles, one generated by the load capacitor C_L and the other one by the VCOs.

Figure 13 shows how S[0:31] and R[0:31] determine the number of enabled power transistors and their ON-times (shown as shaded rectangles with transistor names) for different values of Φ_{ERR}. At steady state, VCO_{ON} and VCO_{OFF} have constant phase difference Φ_{ERR} and the same period (T_{VCO}) and their multiphase outputs S[0:31] and R[0:31] have constant phase spacing of $2\pi/32$. When Φ_{ERR} is $N\times2\pi/32$ (N; integer), N power transistors among M_0~M_{31} are enabled sequentially with the ON-time equivalent to Φ_{ERR}. For example, when Φ_{ERR} is $2\pi/32$, one power transistor among M_0~M_{31} is enabled one by one for $T_{VCO}/32$ (equivalent to the phase of $2\pi/32$) as shown in Figure 14(a). This is equivalent to having one power transistor enabled at all times. When Φ_{ERR} is $30.5\times2\pi/32$, 30 or 31 power transistors are enabled with the ON-time equivalent to the phase of $30.5\times2\pi/32$ as shown in Figure 14(b). This is equivalent to having 30.5 power transistor enabled at all times. In summary, both the number of enabled power transistors and their ON-times are controlled by the time-domain controller, allowing the digital LDO regulator to have fractionally controlled power transistor strength. The output voltage ripple is small because the number of switching (on and off) power transistors is either zero or one at steady state.

When V_{OUT} is outside the window defined by V_{REF_H} and V_{REF_L} of the transient detector, either EN_{ON} or EN_{OFF} becomes "0", enabling the transient mode operation. If $V_{OUT}>V_{REF\_H}$, EN_{ON}="0" disables VCO_{ON} and only the rising edges of R[0:31] are generated to turn off power transistors one by one at every $T_{VCO\_OFF}/32$ where T_{VCO_OFF} is the period of VCO_{OFF}. Because power transistors are turned off at every rising edge of R[0:31], V_{OUT} decreases quickly to a desired level. If $V_{OUT}<V_{REF\_L}$, EN_{OFF}="0" disables VCO_{OFF} and only the rising edges of S[0:31] are generated to turn on power transistors one by one at every $T_{VCO\_ON}/32$ where T_{VCO_ON} is the period of VCO_{ON}. Because power transistors are turned on at every rising edge of S[0:31], V_{OUT} increases quickly to a desired level.

The chip microphotograph of the digital LDO regulator with the proposed time-domain controller implemented in a 65 nm CMOS technology is shown in Figure 14. The output V_{OUT} can be regulated from 0.5 V to 1.1 V with the input V_{IN} ranging from 0.9 V to 1.2 V. The measured line and load regulations are better than 2.63 mV/V and 0.15 mV/mA, respectively.

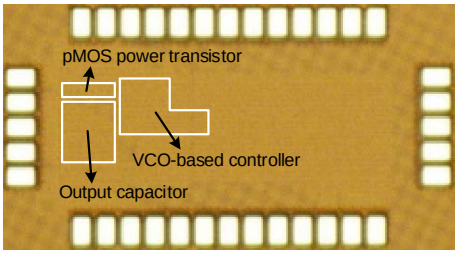
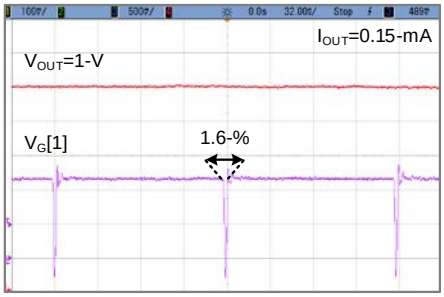
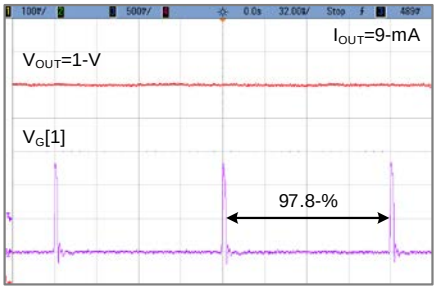


Figure 14. Chip microphotograph of digital LDO regulator with the proposed time-domain controller.



(a)



(b)

Figure 15. Duty cycles of the gate driving signal V_G[1] of the digital LDO regulator when I_{OUT} is (a) 0.15 mA and (b) 9 mA.

The peak current efficiency is 99.3 % with the maximum load current I_{OUT} of 19 mA. Figure 15 is the measured waveforms of V_{OUT} and the gate driving signal V_G[1] of the power transistor M_1 when I_{OUT} is 0.15 mA and 9 mA for V_{IN}=1.2 V and V_{OUT}=1.0 V. The ON-time (duty cycle) of power transistor becomes larger to supply more current for larger load current. The output voltage ripple is smaller than 7 mV at steady state.

6. CONCLUSION

As CMOS technology continues to scale down to sub-10-nm, the importance and necessity of alternative analog signal processing technique other than the conventional amplifier-based one is becoming intensified. As a strong and promising alternative analog signal processing technique, the basic concepts and some design examples of time-domain analog signal processing are provided.

ACKNOWLEDGMENT

This work was supported by the Samsung Research Funding Center of Samsung Electronics under Project Number SRFC-IT1501-52 and by the Samsung Future Interconnect Technology Cluster Program. The CAD tools and chip fabrication were supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] H. Iwai, "Roadmap for 22 nm and beyond," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1520-1528, Sep. 2009.

[2] T. Mogami, "CMOS scaling and variability," *WIMNACT WS & IEEE EDS Mini-Colloquium on Nano-CMOS Technology*, Jan. 2012.

[3] L. L. Lewyn, T. Ytterdal, C. Wulff, and K. Martin, "Analog circuit design in nanoscale CMOS technologies," *Proc. IEEE*, vol. 97, no. 10, pp. 1687-1714, Oct. 2009.

[4] B. Gilbert, "Current mode, voltage mode, or free mode? A few sage suggestion," *Analog Integrated Circuits and Signal Processing*, vol. 38, pp. 83-101, 2004.

[5] K. Kim and C. Yoo, "Time-domain operational amplifier with voltage-controlled oscillator and its application to active-RC analog filter," *IEEE Trans. Circuits and Systems-II*, vol. 67, no. 3, pp. 415-419, Mar. 2020.

[6] C.-W. Hsu and P. R. Kinget, "A 40 MHz 4th-order active-UGB-RC filter using VCO-based amplifier with zero compensation," *Proc. IEEE Eur. Solid-State Circuits Conf.* pp. 359-363, 2014.

[7] Y. Hwang, A. Liu, Y. Chang, and J. Chen, "A high-efficiency fast-transient response buck converter with analog voltage dynamic estimation techniques," *IEEE Trans. Power Electronics*, vol. 30, no. 7, pp. 3720-3730, Jul. 2015.

[8] L. Cheng, Y. Liu, and W.-H. Ki, "A 10/30 MHz fast reference tracking buck converter with DDA-based type-III compensator," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2788-2799, Dec. 2014.

[9] S. J. Kim, Q. Khan, M. Talegaonkar, A. Elshazly, A. Rao, N. Griesert, G. Winter, W. McIntyre, and P. K. Hanumolu, "High frequency buck converter design using time based control techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 990-1001, Apr. 2015.

[10] S. J. Kim, R. K. Nandwana, Q. Khan, R. Pilawa-Podgurski, and P. K. Hanumolu, "A 4-phase 30-70 MHz switching frequency buck converter using a time-based compensator," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2814-2824, Dec. 2015.

[11] J.-G. Kang, M.-G. Jeong, J. Park, and C. Yoo, "A 10 MHz time-domain controlled current-mode buck converter with 8.5% to 93% switching duty cycle," *Dig. Tech. Paper, IEEE Solid-State Circuits Conf.* pp. 424-425, 2018.

[12] Y.-H. Lee, S.-Y. Peng, C.-C. Chiu, A. C.-H. Wu, K.-H. Chen, Y.-H. Lin, S.-W. Wang, T.-Y. Tsai, C.-C. Huang, and C.-C. Lee, "A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1018-1030, Apr. 2013.

[13] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P.-H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65-nm CMOS," *Proc. IEEE Custom Integrated Circuits Conf.* pp. 1-4, 2010.

[14] Y. Lu, F. Yang, F. Chen, and P. K. T. Mok, "A 500 mA analog assisted digital-LDO-based on-chip distributed power delivery grid with cooperative regulation and IR-drop reduction in 65nm CMOS," *Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf.* pp. 310-312, 2018.

[15] M. Huang and Y. Lu, "An analog-proportional digital-integral multi-loop digital LDO with fast response, improved PSR and zero minimum load current," *Proc. IEEE Custom Integrated Circuits Conf.* pp. 1-4, 2019.

[16] X. Liu, H. K. Krishnamurthy, T. Na, S. Weng, K. Z. Ahmed, K. Ravichandran, J. Tschanz, and V. De, "A modular hybrid LDO with fast load-transient response and programmable PSRR in 14nm CMOS featuring dynamic clamp tuning and

time-constant compensation," *Dig. Tech. Paper, IEEE Int. Solid-State Circuits Conf.* pp. 234-236, 2019.
[17] J.-G. Kang, M.-G. Jeong, J. Park, and C. Yoo, "Time-based digital LDO regulator with fractionally controlled power transistor strength and fast transient response," *Proc. IEEE Asian Solid-State Circuits Conf.* pp. 45-46, 2019.

AUTHOR BIOGRAPHIES

Jin-Gyu Kang received the B.S. degree in electronic engineering from Hanyang University, Seoul, Korea in 2014 where he is currently working towards the Ph.D. degree. His main research interest is the power management integrated circuit design.

Kyungmin Kim received the B.S. and Ph.D. degrees all in electronic engineering from Hanyang University, Seoul, Korea in 2013 and 2020, respectively. Dr. Kim is currently working as a DRAM design engineer at Samsung Electronics, Hwaseong, Korea.

Changsik Yoo received the B.S. (Highest Honor), M.S., and Ph.D. degrees from Seoul National University, Seoul, Korea, in 1992, 1994, and 1998, respectively, all in electronic engineering. From 1998 to 1999, he was with the Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland, as a Research Staff. From 1999 to 2002, he was with Samsung Electronics, Hwaseong, Korea, as a Senior Engineer. Since 2002, he has been a Professor of Hanyang University, Seoul, Korea. From 2008 to 2009, he worked as a Senior Engineer of Silicon Image Inc. California, USA during the sabbatical leave. In 2018, he was a visiting scholar of Swiss Federal Institute of Technology, Lausanne, Switzerland. From 2019 to 2020, he was a visiting scholar of Samsung Electronics, Hwaseong, Korea where he worked on the next-generation DRAM interface. His main research interest is the mixed mode CMOS integrated circuit design. He served as a Technical Committee Member for several international conferences, such as the IEEE International Solid-State Circuits Conference, the IEEE VLSI Circuits Symposium, and the IEEE European Solid-State Circuits Conference. He was an Associate Editor of the IEEE Microwave and Wireless Components Letters.