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멀티레벨 승압 DC-DC 컨버터와 구성된 독립형 부하를 위한 단상 5레벨 인버터

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Single Phase Five Level Inverter For Off-Grid Applications Constructed with Multilevel Step-Up DC-DC Converter

Ibadullaev Anvar[1] and Sung-Jun Park†

Abstract

The recent use of distributed power generation systems constructed with DC-DC converters has become extremely popular owing to the rising need for environment friendly energy generation power systems. In this study, a new single-phase five-level inverter for off-grid applications constructed with a multilevel DC-DC step-up converter is proposed to boost a low-level DC voltage (36 V-64 V) to a high-level DC bus (380 V) and invert and connect them with a single-phase 230 V rms AC load. Compared with other traditional multilevel inverters, the proposed five-level inverter has a reduced number of switching devices, can generate high-quality power with lower THD values, and has balanced voltage stress for DC capacitors. Moreover, the proposed topology does not require multiple DC sources. Finally, the performance of the proposed topology is presented through the simulation and experimental results of a 400 W hardware prototype.

Key words: Off-grid, Multilevel inverter, Switched-capacitor, High efficiency, DC-link capacitors voltage balancing issue

1. Introduction

The renewable energy production systems are utilized nowadays mainly in two fundamental groups: the stand-alone PV systems and grid-connected PV systems. The stand-alone PV systems are utilized with a battery bank for charging and discharging operations. Because both of this systems have DC output characteristics, they require dc-ac inverters to send harvested energy to the AC grid or to AC loads as shown in Fig. 1. Generally, two-level inverters are applied in such a systems. And also, in the systems, the inverters need to be interfaced with a step-up DC-DC converter, because PV or Fuel Cell Systems have low output voltage characteristics. Different topology of inverters are presented to produce and transmit high efficient AC power to AC grid[1]-[3]. But, the harmonics of the output AC currents and voltage stress of the components are very high. To solve the current harmonic and another power quality related problems, Multilevel inverters are being created. Multilevel inverters (MLI) are introduced as a high quality devices, which has a better electromagnetic characteristics, lower voltage stress on switches and so on. Typically MLIs are divided into three main classifications: diode-clamped MLI, flying-capacitor MLI and cascaded H-bridge MLI.

The economically available MLI topologies are diode-clamped MLI, flying-capacitor MLI and also H-bridge MLI[4]-[6]. But on the other hand, the topologies require a large number of passive elements and semiconductors and one more DC sources to voltage levels, which in some situations cannot be available.

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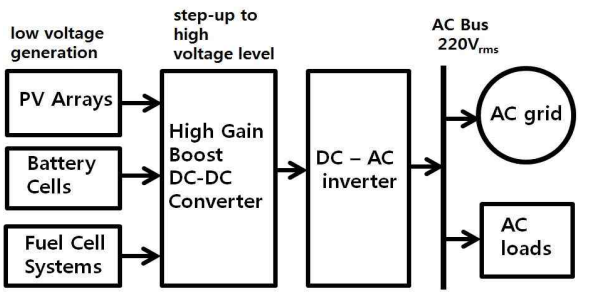

Fig. 1. Renewable voltage source based power generation system.

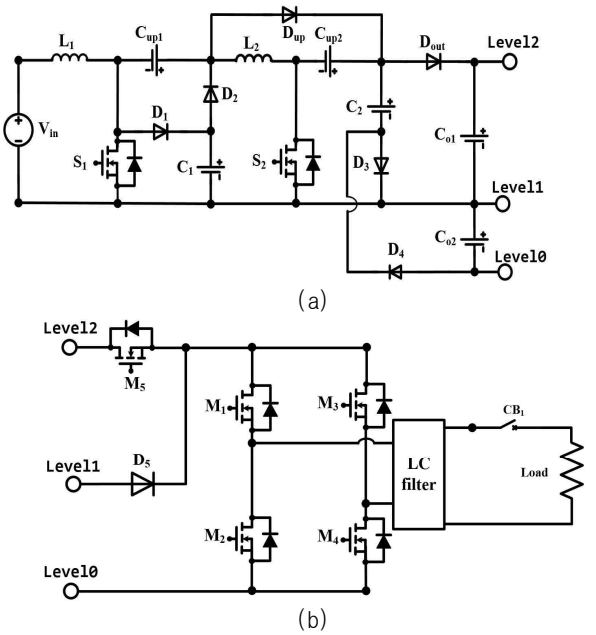

Fig. 2. Two stage circuit of the proposed topology. (a) step-up multilevel DC-DC converter, (b) Five level inverter.

To overcome these problems, various topologies of MLI are presented in the papers[7]-[10]. One of them is switched-capacitor(SC) and switched-inductor(SL) based MLI topologies. The topologies certainly have many advantages, such that a boost capability and self-balanced DC-link capacitor voltage, but the boosting voltage gain of the topologies is still low. Also single-phase step-up SC-cell based (2n+1) level inverter was presented in [11]. This topology can step-up the input DC voltage and invert them to multilevel AC voltage. In [12] a transformeless five level inverter consisting of SC cells and power switches was proposed. However, the cost problem and the efficiency decreasing due to output power increasing still serious in above mentioned papers.

From the view of industrial application, it would be a more desirable if the cost of the inverter can be reduced. So, in order to obtain high gain, high efficient distributed power generation systems, in this paper Single Phase Five level Inverter for Off-Grid applications constructed with multilevel DC-DC step-up converter is proposed. The proposed topology is structured in two stage. In the first stage a low DC voltage level is increased to high DC voltage level and in the second stage high DC voltage is inverted to five level AC voltage. Then through LC filter it will be connected with AC load. The proposed topology is controlled by closed-loop digital dual PI controller, adding AC voltage control method. The advantages of the proposed topology include:

① It has high voltage gain DC-DC converter;
② No need for DC-link capacitor voltage balancing hardware circuit or control method;
③ Requires lower number of power semiconductors;
④ Stress voltage of power semiconductors are decreased;
⑤ Input voltage range of the topology is wide;
⑥ It requires the only input DC source.

This paper is discussed as follow: Section Ⅱ introduces the proposed topology hardware configuration. In Section Ⅲ operating principles will be discussed. The components selections are presented in Section Ⅳ. Simulation results, the hardware implementation and experiment results are shown in Section Ⅴ. The next Section Ⅵ provides a conclusion of the proposed topology.

2. The Circuit Configuration of the Proposed Topology

The circuit of the proposed topology consist on two stage: the first stage is high gain step-up multilevel DC-DC converter which is shown in Fig. 2 (a). And the second stage is five level single phase inverter which is presented in Fig. 2 (b). Step-up multilevel DC-DC converter is made by two MOSFETs S_1 and S_2, inductors L_1 and L_2, capacitors C_1, C_2, C_{UP1}, C_{UP2} C_{o1}, C_{o2}, diodes D_1, D_2, D_3, D_4, D_{up} and D_{out}. Output capacitors C_{o1} and C_{o2} are connected in series. C_{o1} capacitor have common ground with the input DC source, but C_{o2} capacitor has different ground. Thus C_{o1} capacitor holds $\frac{2}{3} * V_{out}$ equal voltage and C_{o2} capacitor have $\frac{1}{3} * V_{out}$ equal voltage. Capacitors C_{UP1} and C_{UP2} are connected in switched-capacitor technique. Output DC voltage is made by summing

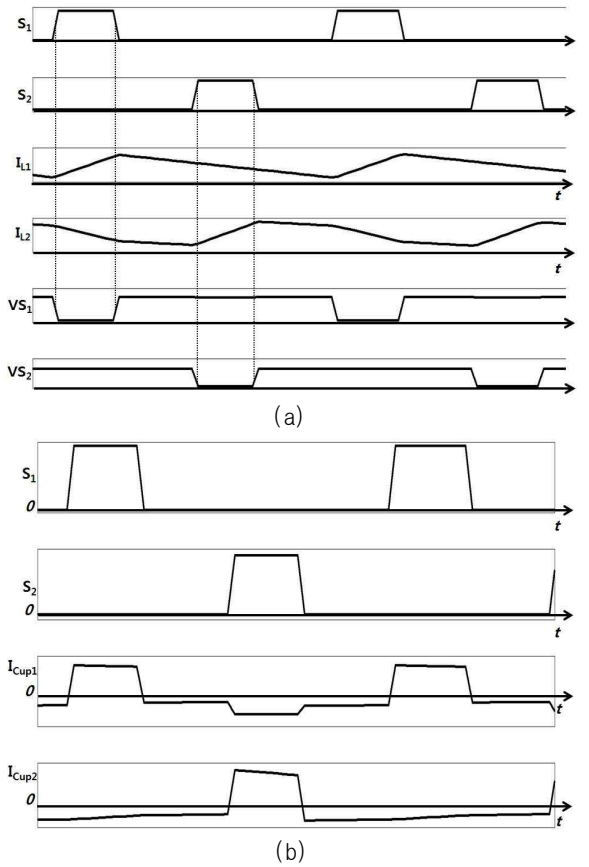

Fig. 3. Main waveforms of the DC-DC converter of the proposed topology.

C_{o1} and C_{o2} capacitors voltage and will be sent to the next DC-AC inverter stage. The second stage of the proposed topology is five level inverter which is presented in Fig. 2. (b). The inverter is made from five MOSFETs M_1, M_2, M_3, M_4, M_5 , one diode D_5 and LC filter.

3. Operating Analysis of the Proposed Topology

3.1 DC-DC Converter Operation and Analysis

In order to explain the steady state operation of the DC-DC converter, some assumptions are made as below:

① All the components are ideal with no loss;
② The summarized capacitance of the two output capacitor is capable to maintain constant voltage;
③ Inductors current increases and decreases linearly.

Two switches S_1 and S_2 have the same duty value, but their gate driving signals has 180^0 phase shifting. There are four different switching states "S_1S_2" = [10, 00, 01, 11], where "0" means that switch is in "OFF"

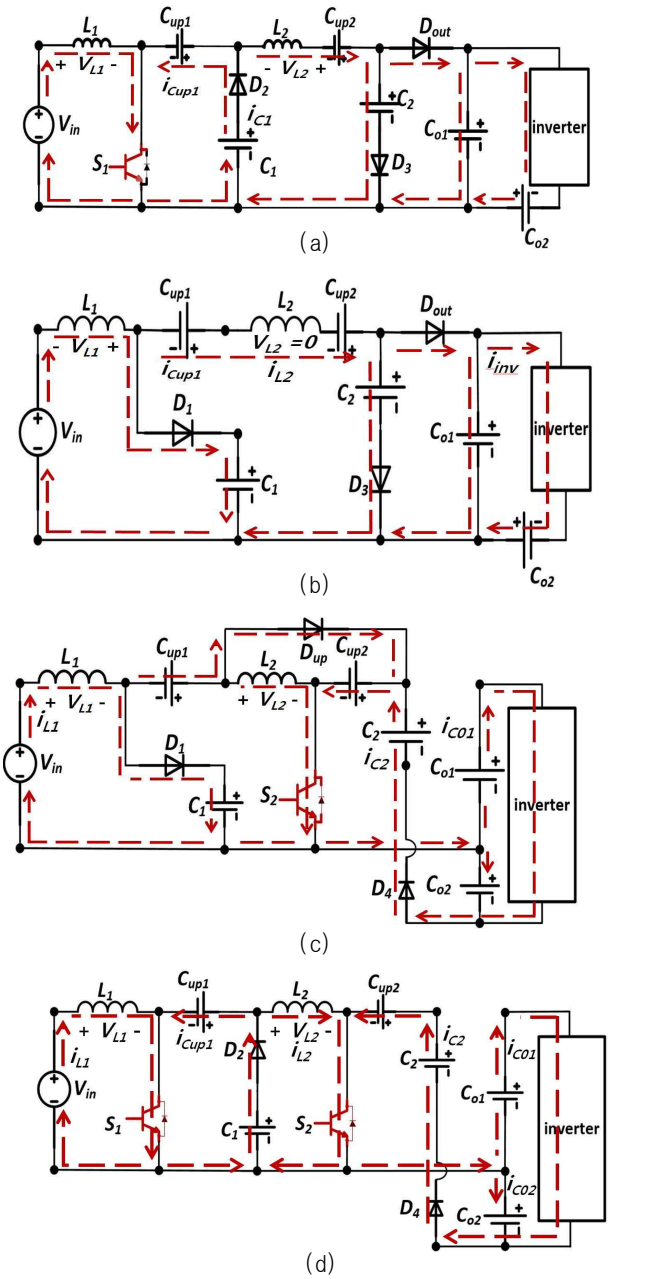

Fig. 4. Power flowing waveforms of the switching states of the DC-DC converter of the proposed topology. (a) S1S2 = [10] mode, (b) S1S2 = [00] mode, (c) S1S2 = [01] mode, (d) S1S2 = [11] mode.

state and "1" means switch is in "ON" state. L_1 inductor is charged when S_1 switch is in "ON" state and consequently is discharged when S_1 switch is in "OFF" state which is seen from the Fig. 3. Energy flowing paths of each switching states of the DC-DC converter are shown in Fig. 4. Simulation results of the DC-DC converter of the proposed topology are shown in Fig. 8.

In switching state "S_1S_2" = [10] S_1 is in ON state and oppositely S_2 is in OFF state. In this switching

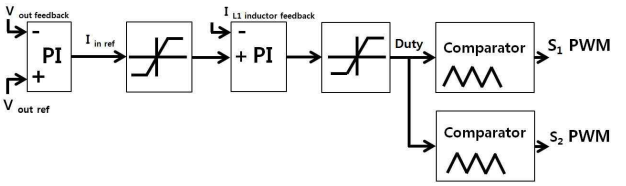

Fig. 5. Output voltage control scheme of the DC-DC converter of the proposed topology.

state which can be seen in Fig. 4(a) inductor L_1 is charged with i_{L1} current from input DC source and capacitor C_{up1} is charged by C_1 capacitor. And also C_{up2} and C_{o2} capacitors are discharged. The load is supplied by summarizing C_1, C_{up2} and C_{o2} capacitors voltages. Therefore, in this switching state the following equations are made:

$$V_{L1} = V_{dcsource} = L_1 * \frac{dI_{L1}}{dT} \quad (1)$$

$$V_{C_{o1}} = V_{C_1} - V_{C_{up2}} - V_{L2} \quad (2)$$

$$V_{LOAD} = V_{C_1} - V_{C_{up2}} - V_{L2} - V_{Co2} \quad (3)$$

$$i_{LOAD} = i_{C_{o2}} + i_{L2} + i_{C_{up2}} \quad (4)$$

where $V_{C_{up2}}$ is C_{up2} capacitor voltage;
i_{L1} is L_1 inductor current;
$V_{dcsource}$ is input DC source voltage;
V_{C_1} is C_1 capacitor voltage;
V_{C_2} is C_2 capacitor voltage;
$V_{C_{01}}$ is C_{o1} capacitor voltage;
$V_{C_{02}}$ is C_{o2} capacitor voltage;
V_{LOAD} is the load voltage.

In the next "S_1S_2" = 00 switching state both of the switches are in OFF state, which energy flowing path is pictured in Fig. 4(b). C_1, C_{o1} and C_2 capacitors are charged, the other C_{up1} , C_{up2} and C_{o2} capacitors are discharged. Diode D_4 is turned off. The currents of the inductors I_{L1} and I_{L2} are linearly decreased. The following equations are made in "S_1S_2"= 00 switching state:

$$V_{C_1} = V_{dcsource} - V_{L1} \quad (5)$$

$$V_{C_2} = V_{dcsource} - V_{L1} - V_{C_{up1}} - V_{C_{up2}} \quad (6)$$

$$V_{C_{o1}} = V_{dcsource} - V_{L1} - V_{C_{up1}} - V_{C_{up2}} \quad (7)$$

$$V_{LOAD} = V_{dcsource} - V_{L1} - V_{C_{up1}} - V_{C_{up2}} - V_{Co1} \quad (8)$$

In the next S_1S_2" = 01 switching state S_1 is in OFF state and S_2 is in ON state as shown in Fig. 4(c). $L_2$is being charged.C_1, C_{up2} and C_{o2} capacitors are discharged. D_{out} diode is turned off and the load is supplied in accordance to the next equation:

$$V_{C_{o2}} = V_{C2} - V_{C_{up2}} \quad (9)$$

$$V_{C_{up2}} = V_{dcsource} - V_{L1} - V_{C_{up1}} \quad (10)$$

$$V_{LOAD} = V_{C_{o1}} + V_{C_2} - V_{C_{up2}} \quad (11)$$

In this switching state the load voltage is formed by summarizing C_{o1}, C_2 and C_{up2} capacitors voltages. In the next "S_1S_2" = 11 switching state both of the switches are in ON state, which power flowing path is pictured in Fig. 4(d). C_{up1}, C_{up2} and C_{o2} capacitors are charged. The other C_1, C_2 and C_{o1} capacitors are discharged. Diode D_{out} is turned off. The currents of the inductors I_{L1} and I_{L2} are linearly increased. The following equations are made in "S_1S_2" = 11 switching state:

$$V_{C_1} = V_{dcsource} - V_{L1} \quad (12)$$

$$V_{C_{02}} = V_{C2} - V_{C_{up2}} \quad (13)$$

$$V_{C_2} = V_{C_{up2}} + V_{C_{o2}} \quad (14)$$

$$V_{LOAD} = V_{C_{o1}} + V_{C_2} - V_{C_{up2}} \quad (15)$$

3.1.1 Voltage gain and input current ripple of the DC-DC converter

Applying voltage-second balance of the L_1 and L_2 inductors during the steady-state operation and above menthioned equations (1-15), the following equations of the DC-DC converter of the proposed topology can be made:

$$V_{out} = V_{dcsource} * \frac{6-(4*D)}{(1-D)^2} \quad (16)$$

$$G = \frac{6-(4*D)}{(1-D)^2} \quad (17)$$

$$\triangle I_{L1} = \frac{(1-D)^{2*} V_{dcsource}}{L_1 * f_{sw} * (6-(4*D))} \quad (18)$$

$$\triangle I_{L2} = \frac{2* V_{dcsource}}{L_2 * f_{sw} * (1-D)} \quad (19)$$

TABLE I
FIVE LEVEL INVERTER TRUTH TABLE

stages	M_1	M_2	M_3	M_4	M_5	V_{AC}
I	0	1	0	1	0	0
II	1	0	0	1	0	$\frac{1}{3}*V_{DC}$
III	1	0	0	1	1	V_{DC}
IV	0	1	1	0	0	$-\frac{1}{3}*V_{DC}$
V	0	1	1	0	1	$-V_{DC}$

where V_{out} is out DC voltage, G is DC voltage gain, $\triangle I_{L1}$ and $\triangle I_{L2}$ are L_1 and L_2 inductors current ripple consequently and $V_{dcsource}$ is input DC source voltage.

3.1.2 Voltage stress of the DC-DC converter semiconductors

From the above (16-19) made equations the voltage stress of the power switches is written as:

$$V_{S1} = \frac{V_{OUT}}{(6-(4*D))}*(1-D) \tag{20}$$

$$V_{S2} = V_{out}*\frac{3-(2*D)-(3*D^2)}{3*(3-(2*D))} \tag{21}$$

(20) and (21) equations show that maximum stress voltage of the S_1 power switch depending on D duty value is varying in $[\frac{1}{7}*V_{out};\ \frac{1}{5}*V_{out}]$ interval and the S_2 power switch maximum stress voltage is placed in $[\frac{2}{5}*V_{out};\ \frac{1}{3}*V_{out}]$ interval.

3.1.3 Control method of the DC-DC converter

To maintain output DC voltage in the reference voltage (380 VDC) range and to control input current, a digital double PI regulator is used as shown in Fig. 5. Duty value is being compared with the triangle carrier and thus PWM signals are made. S_2 switch PWM signal is made by 180° shifting the triangle carrier waveform.

3.2 Five Level Inverter Operation and Analysis

Fig. 2(b) shows the five level inverter circuit of the proposed topology. There are five switches and just one diode in this figure. MOSFETs M_1, M_2, M_3, M_4, represents H-type structure. Adding M_5 and D_5 to

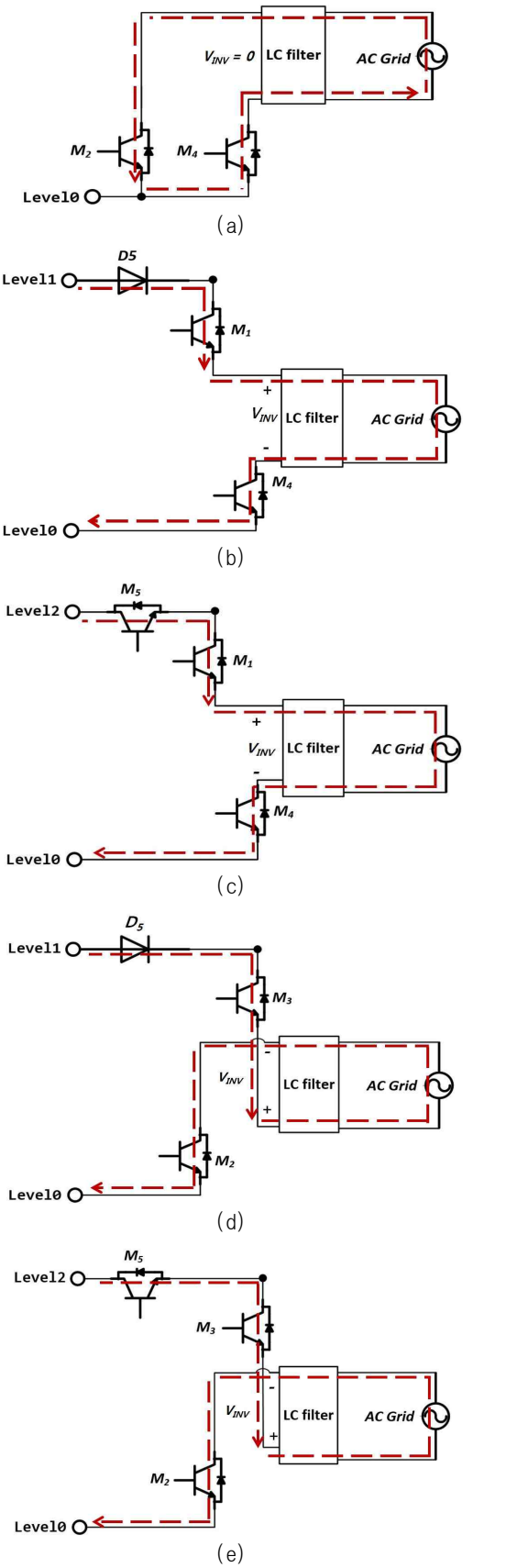

Fig. 6. Operating stages of the five-level inverter of the proposed topology. (a) I stage, (b) II stage, (c) III stage, (d) IV stage, (e) V stage.

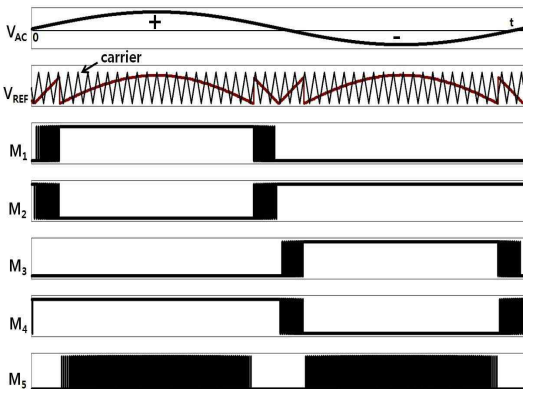

Fig. 7. Switching pattern of the five level inverter of the proposed topology.

this structure let to produce five level AC voltage. Operation mode of the inverter consist on five independent switching states that generate the required five level voltage which are shown in Table I, Fig. 6 and in Fig. 7. The switching function of the switches is defined as follow:

$$S_x = \begin{cases} 1 & S_x \ is \ on \\ 0 & S_x \ is \ off \end{cases} \quad x = 1,2,3,4,5 \qquad (22)$$

The five operating stage waveforms of the five-level inverter are given in Fig. 6 and described in details as follow:

① Zero output level (stage I): In this stage the switches M_2 and M_4 are in ON state. Diode D_5 is forward-biased. The other switches are in OFF state. During these two stages, an zero-output voltage is applied to LC filter.

② Positive $\frac{1}{3} * V_{out}$ voltage level (stage II): The switches M_1 and M_4 are in ON state. Diode D_5 is forward-biased. The other switches are in OFF state. During the stage, $\frac{1}{3} * V_{out}$ equal voltage is applied to LC filter.

③ Positive V_{out} voltage level (stage III): Switches M_1, M_4 and M_5 are in ON state. Diode D_5 is forward-biased. The other switches are in OFF state. During the stage, V_{out} equal voltage is applied to LCfilter.

④ Negative $\frac{1}{3} * V_{out}$ voltage level (stage IV): The switches M_2 and M_3 are in ON state. The other switches are in OFF state. In this stage, $-\frac{1}{3} * V_{out}$ equal voltage is applied to LC filter.

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE PROPOSED TOPOLOGY

Parameter	Values
Input Voltage DC	36-64 V
Output Voltage AC	230 Vrms
Power	400 W
Switching frequency	30 Khz
Efficiency	90-93.2 %

TABLE III
COMPONENTS SPECIFICATION OF THE PROPOSED TOPOLOGY

Devices	Model	Specifications
MOSFET (S1)	IPB020N10N5	100V/176A
MOSFET (S2)	IRFP4668PBF	200V/130A
Diodes	DPG10I200PA/IXYS	200V/10A
Diode D5	SBR40U300CTB	300V/40A
MOSFET M1.M2,M3,M4,M5	C2M0025120D/CREE	1200V/90A
Inductors L1 L2	TDK	600uH
Capacitor Cup1	NXA/SAMYOUNG	820uF/100VDC
Capacitors(other)	B43630F2827M000/TDK	820uF/250VDC
AC filter inductor	TDK	2mH
AC filter capacitor	Panasonic	1uF

⑤ Negative V_{out} voltage level (stage V): The switches M_2, M_5 and M_4 are in ON state. Diode D_5 is forward-biased. The other switches are in OFF state. $-V_{out}$ equal voltage is applied to LC filter.

4. Components Selection

4.1 DC-DC Converter Components Selection

The inductors of the DC-DC converter part of the proposed topology is designed according to (18) and (19). C_1, C_{up1} and output capacitor values are selected based on the next formulas:

$$C_{1\min} = \frac{(6-4*D)*P_{out}}{\triangle V_{out} * V_{out} * f_{sw}} \qquad (23)$$

$$C_{outmin} = \frac{(1-D)*P_{out}}{\triangle V_{out} * V_{out} * f_{sw}} \qquad (24)$$

According to (20) and (21) formulas, S_1 and S_2 switch of the DC-DC converter are selected with 100V and 200V breaking voltage respectively.

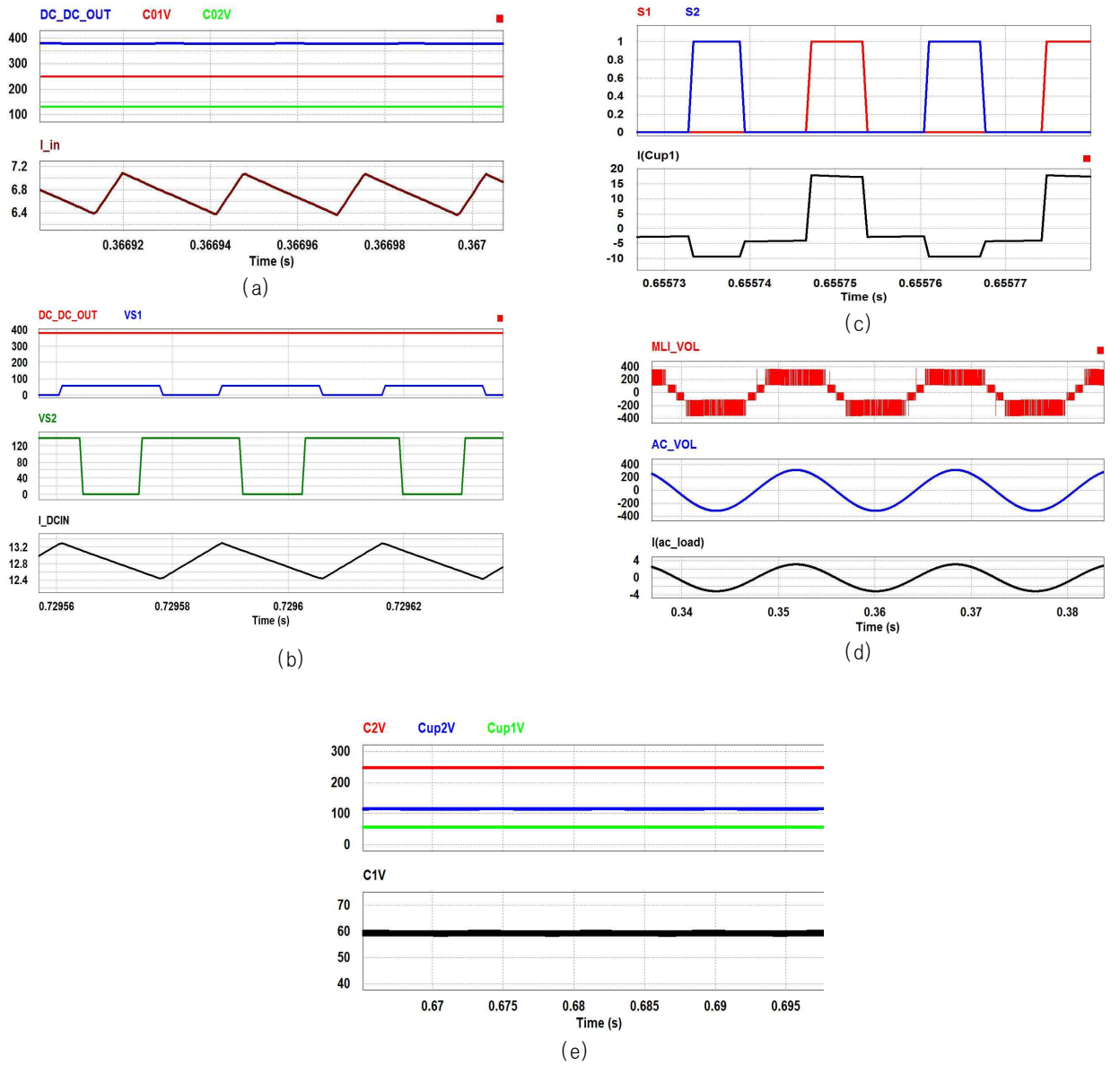

Fig. 8. Simulation results of the proposed topology. From top to bottom: (a) DC Link voltage (blue), C_{o1} capacitor voltage (red), C_{o2} capacitor voltage (green), input current (brown), (b) DC output voltage (red), S_1 switch drain-source voltage (blue), S_2 switch drain-source voltage (green), input current (black), (c) S_1 switch gate-source voltage (red), S_2 switch gate-source voltage (blue), C_{up1} capacitor current (black), (d) Five level inverter output voltage (red), AC voltage (blue) and AC current (black), (e) C_2 (red), C_{up2} (blue). C_{up1} (green), and C_1 (black) capacitors voltage.

4.2 Five Level Inverter Components Selection

In the five level inverter side of the proposed topology LC filter values are designed according to above formula

$$C_{AC} = VAR^{*}\frac{P_{out}}{2\pi^{*}f_{sw}{}^{*}(V_{ACout})^{2}} \tag{25}$$

$$L_{AC} = \frac{V_{LOAD}}{4^{*}f_{sw}{}^{*}\triangle i_{pp}} \tag{26}$$

where VAR is 2% of the AC voltage and $\triangle i_{pp}$ is AC current ripple percentage. It is selected as 15% of AC current in this experiment Due to low $R_{DS(ON)}$ and better switching and conducting characteristics, SiC type Power MOSFET are selected as five level inverter switches.

5. Simulation and Experiment Results

To verify the operating performance of the proposed topology. simulation studies are conducted by PSIM 9.1 software tool. Table Ⅱ and Table Ⅲ list the simulation

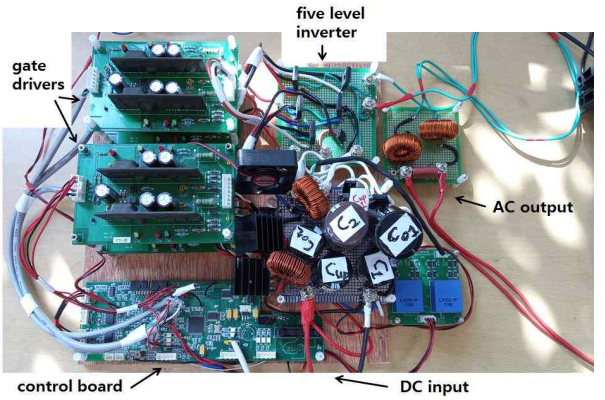

Fig. 9. Experiment prototype of the proposed topology.

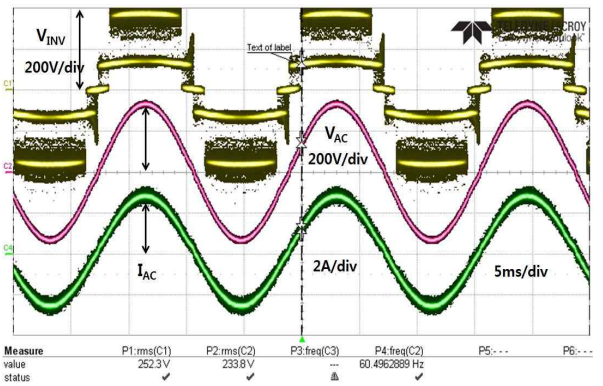

Fig. 10. Experiment results of the proposed topology. From top to bottom: Five level inverter output voltage (yellow), AC voltage (red), and AC current (green).

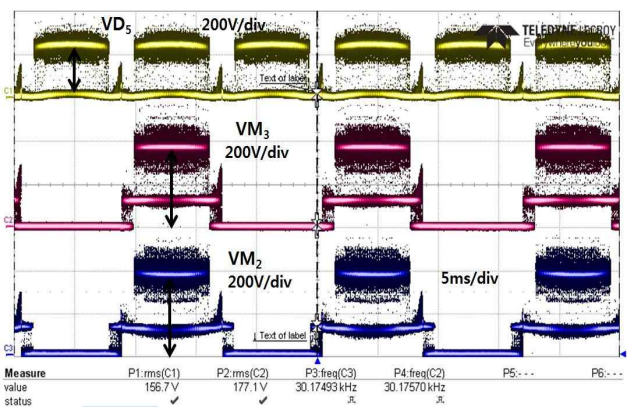

Fig. 11. Experiment results of the proposed topology. From top to bottom: D_5 diode voltage (yellow), M_3 switch drain-source voltage (red), M_2 switch drain-source voltage (blue).

and experiment parameters of the proposed topology. Fig. 8(a) shows simulation results when the input DC source is 36V. It is seen that C_{o1} capacitor and C_{o2} capacitor voltages are stepped up to 250V and 130V, respectively. DC link voltage is 380V and it is formed by adding the C_{o1} and C_{o2} capacitors voltage values.

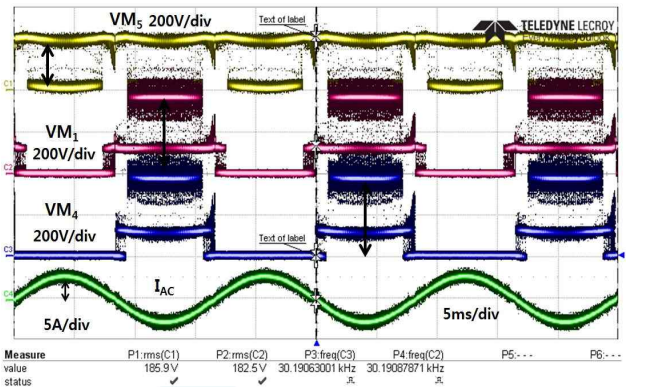

Fig. 12. Experiment results of the proposed topology. From top to bottom: M_5 switch drain-source voltage (yellow), M_1 switch drain-source voltage (red), M_4 switch drain-source voltage (blue) and AC load current (green).

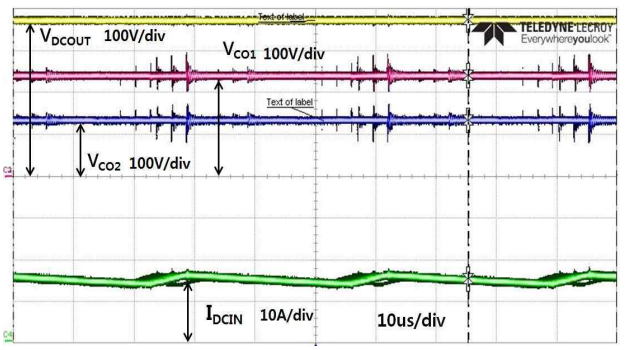

Fig. 13. Experiment results of the proposed topology. From top to bottom: DC Link voltage (yellow), C_{o1} capacitor voltage (red), C_{o2} capacitor voltage (blue), DC source input current (green).

L_1 inductor current is changing linearly depending on S_1 switch operation as shown in Fig. 8(b). The hardware of the proposed topology is assembled as shown in Fig. 9 and experiments were carried out. DSP TMS320F28069 based double closed loop controller is implemented to maintain DC output in the DC reference value of the DC-DC converter. Applying the setting parameters, proposed topology is well experimented. Resistor is the used as an AC load. Fig. 10 Fig. 11 and Fig. 12 show the experiment results under unity power factor. From Fig. 10 it is seen that five level inverter output, AC voltage and AC current have the same phase. Driving PWM signals of S_1 and S_2 switches have a 180° phase difference.

L_1 inductor is being charged and discharged according to S_1 switch operation. DC-DC converter of the proposed topology creates multi output levels: 380V, 250V, 130V and 0 V, which are seen in Fig. 13. Fig. 14 shows that C_{up1} capacitor has not inrush

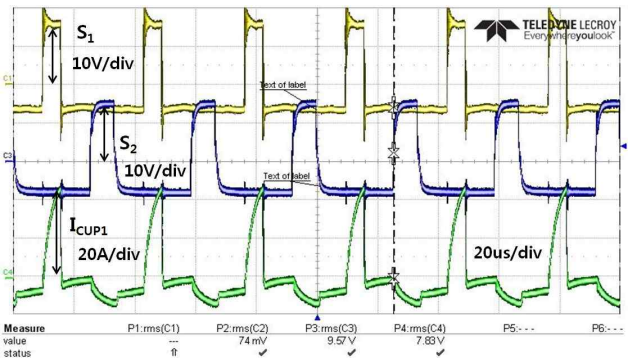

Fig. 14. Experiment results of the proposed topology. From top to bottom: S_1 switch gate-source voltage (yellow), S_2 switch gate-source voltage (blue), C_{up1} capacitor current (green).

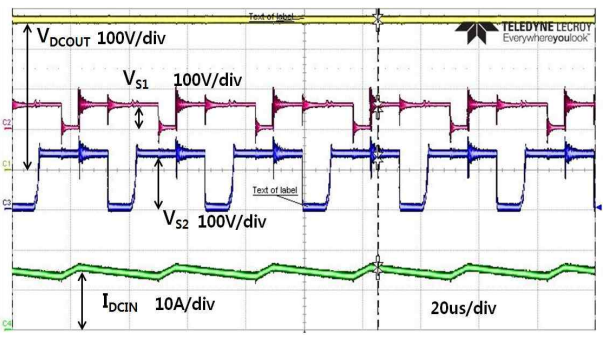

Fig. 15. Experiment results of the proposed topology. From top to bottom: DC output voltage (yellow), S_1 switch drain-source voltage (red), S_2 switch drain-source voltage (blue), DC source input current (green).

current. From Fig. 15 it is seen that S_1 and S_2 switches have decreased draun-source voltages. It let to use low voltage and low $R_{DS(ON)}$ switches because of that the system efficiency is increased which is seen from Fig. 16. The system maximum efficiency is 93.1% when the input voltage is 64V and load power is 300W. Moreover, the minimum efficiency is 90.1% which is at 400W load and 42V input voltage conditions.

6. Conclusions

In this paper a new Single Phase Five Level Inverter for Off-Grid Applications constructed with A Newly Created Multilevel DC-DC step-up converter is proposed. As compared with the conventional two stage inverters, it requires less number of switches for a single phase five level AC voltage. The operating principles, switching states and patterns are presented in detail. The proposed topology has many

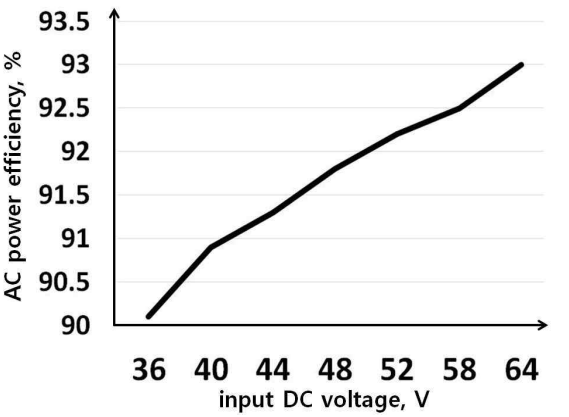

Fig. 16. AC power efficiency-input DC voltage curve.

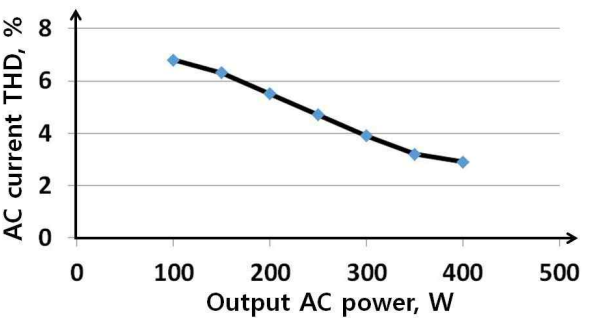

Fig. 17. AC current THD-output AC power curve.

advantages like that low stress voltage, simple modulation control and lower current THD which is shown in Fig. 17. Experimental prototype based on a 400W hardware have been carried out to demonstrate the performance of the proposed topology.

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