산업융합연구 제18권 제2호 pp. 69-75, 2020
ISSN 2635-8875 / e-ISSN 2672-0124
https://doi.org/10.22678/JIC.2020.18.2.069

A Cache Hit Ratio based Power Consumption Model for Wireless Mesh Networks

Seung Hyun Jeon[1*], Yong-jun Seo[2]
[1]Researcher, School of Electrical Engineering, Korea Advanced Institute of Science and Technology
[2]Student, School of Electrical Engineering, Korea Advanced Institute of Science and Technology

무선 메쉬 네트워크를 위한 캐시 적중률 기반 파워 소모 모델

전승현[1*], 서용준[2]
[1]한국과학기술원 전기및전자공학부 박사후 연구원, [2]한국과학기술원 전기 및 전자공학부 학생

Abstract Industrial IoT has much interested in wireless mesh networks (WMNs) due to cost effectiveness and coverage. According to the advance in caching technology, WMNs have been researched to overcome the throughput degradation of multihop environment. However, there is few researches of cache power consumption models for WMNs. In particular, a wired line based cache power consumption model in content-centric networks is not still proper to WMNs. In this paper, we split the amount of cache power from the idle power consumption of CPU, and then the cache hit ratio proportional power consumption model (CHR-model) is proposed. The proposed CHR-model provides more accurate power consumption in WMNs, compared with the conventional cache power efficiency based consumption model (CPE-model). The proposed CHR-model can provide a reference model to improve energy-efficient cache operation for Industrial IoT.

Key Words : Industrial IoT, Wireless Mesh Networks (WMNs), Cache Hit Ratio, Cache Size, Power Consumption Model

요 약 산업용 IoT는 비용 효율적이고 넓은 커버리지를 제공하는 무선 메쉬 네트워크에 관심이 많았다. 하지만, 무선 메쉬 네트워크는 멀티홉 환경의 심각한 성능 절하를 겪는다. 이를 극복하기 위해 메쉬 라우터에 캐시를 장착하는 연구가 많았으나 캐시 파워 소모 모델 연구는 적었다. 최근 캐시 파워 효율 기반 모델은 캐시까지 콘텐츠 전달 파워를 모두 측정했기 때문에 무선 메쉬 네트워크에서 쓰기에 부적절합니다. 본 논문은 CPU의 동작속도가 캐시 크기에 비례한다는 사실을 이용하여 캐시 적중률 기반 파워 소모 모델을 제안하고, 기존 캐시 파워 효율 기반 소모 모델과 비교하여 정확하게 측정되었다. 제안된 캐시 적중률 기반 파워 소모 모델은 산업용 IoT에서 무선 메쉬 네트워크를 구성할 시 에너지 효율적인 캐시 운용을 위한 참조 모델로 활용되길 기대합니다.

키워드 : 산업용 IoT, 무선 메쉬 네트워크, 캐시 적중률, 캐시 크기, 파워 소모 모델

1. Introduction

According to spreading the development of hardware and protocols for industrial Internet of things (IoTs) such as Bluetooth, LoRa and IEEE 802.11, interest for wireless mesh networks (WMNs) has been increased due to cost effectiveness, reliability, and coverage[1]. For example, a Bluetooth device integrated with master as well as slave functions has supported WMNs[2]. Nevertheless, due to severe problem of

*Corresponding Author : Seung Hyun Jeon(creemur@kaist.ac.kr)
Received April 5, 2020 Revised April 14, 2020
Accepted April 20, 2020 Published April 30, 2020

throughput degradation in multihop environment, WMNs have been still deployed as small and middle scale of networks[3]. Recently, caching technique that stores content in mesh routers (MRs) near mobile users can improve the throughput. However, using many caching resources causes to increase the power consumption of cache due to CPU usage. Thus, cache can increase the power consumption of WMNs. Despite the advance of CPU technologies and increasing capacity of the cache, there is still lack of researches for cache power consumption.

Authors analyzed cache power consumption in content-centric networks (CCNs)[4]. However, the power consumption model based on cache power efficiency (CPE-model), which considers cache transmission power per bit (Watt/bit) based on a cache level, is not suitable for WMNs because power consumption delivering and storing content into cache is considered without the limitation of the MR's maximum power consumption. The another power consumption model did not consider the cache in WMNs[5]. The representative traffic proportional power consumption models in ITU-T Recommendations Y.3022 (measuring energy in networks) were not standardized for cache[6]. Nonetheless, the power consumption of cache in CPU is proportional to a size of cache[7-9]. That is, cache power can be extracted from idle power as CPU, and then be measured again. Thus, a new power consumption model is required to design energy-efficient operations for industrial IoT.

In this paper, we propose a novel power consumption model suitable in WMNs, reflecting a traffic model of multihop environment. The proposed cache power consumption model based on cache hit ratio (CHR-model), which does not include delivered power for stored cache and consider only the power consumption for hit content, is designed in proportional to the size of cache within the maximum power per MR. Numerical results show that the total power consumption measured by our proposed CHR-model is measured more accurately than the existing CPE-model.

2. Problem Formulation

2.1 System Model

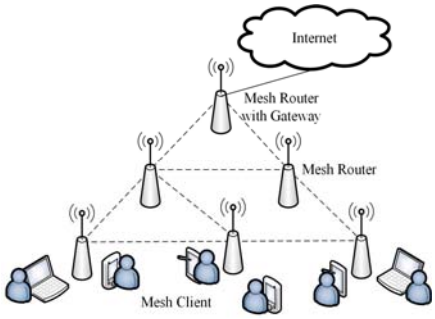

Fig. 1. General architecture of WMNs

WMNs consist of devices with three roles via general architecture of Fig. 1[10]: a MR with a gateway, MRs, and mesh clients (i.e., mobile users). First, the MR with the gateway links into wired networks for Internet connection. MRs link each other wirelessly. Finally, mobile users can connect to the Internet via adjacent MRs. If the count of hops from the MR with the gateway increases, mobile users may feel significant throughput degradation.

Accordingly, Fig. 2 shows a block diagram for WMNs, which is composed of cache-enabled MRs[2]. Our network model is designed as linear multihop environment[11]. Here, we consider the content request into cache of the MR with the gateway. However, since the existing CPE-model measures power for content delivered into the cache from a content delivery network in CCNs, all MRs with cache store content, and can measure cache power according to CPE. In a proposed CHR-model, cache power consumption of the MR that a cache hit occurs is only measured.

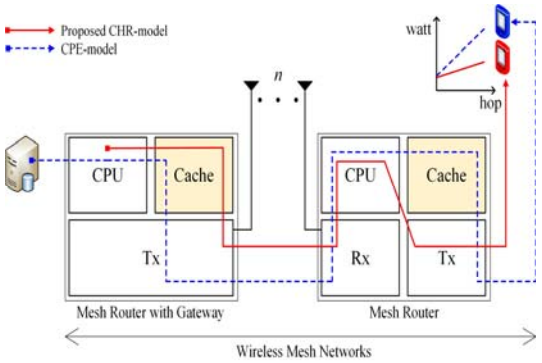

Fig. 2. A block diagram of a proposed CHR-model for WMNs

2.2 Traffic Model

We assume that a traffic model is exponentially distributed according to[12,13], which result in

$$r_h = r_h \lambda e^{-\lambda h}, \quad (1)$$

where is λ distribution parameter, h is the number of hops from the gateway that h = 0, and r_0 is the data rate at the gateway. n is the number of MRs in Fig. 2. Let R : $\{r_0, r_1, r_2, \ldots, r_{n-1}\}$ be the set of data rate from the gateway of 0^{th} hop to the $n-1^{th}$ hop away. The data rate is used in the form of traffic load ρ by dividing by the link capacity C_{MR} at the MR.

Since ζ as total overhead above an IP layer is defined as $\frac{\gamma}{\beta+\gamma}$, ζr_h is the maximum throughput in the IP layer[14]. Here, β is total overhead above a MAC layer and γ is an IP layer datagram size. Cache traffic is considered as an IP packet[15].

2.3 Path Loss Model

We use a following indoor path loss model from[16].

$$L_{total} = L(d_0) + N_{PL} \log_{10} \frac{d}{d_0} + L_f(n), \quad (2)$$

where N_{PL} is distance power loss coefficient, f is frequency (MHz), d is separation distance (m) between the base station and portable terminal (where d > 1m), d_0 is reference distance (m), $L(d_0)$ is path loss at d_0 (dB), for a reference distance d_0 at 1m, and assuming free-space propagation $L(d_0) = 20\log_{10} f - 28$ where f is in MHz, L_f is floor penetration loss factor (dB), and n is number of floors between access point and portable terminal ($n \geq 0$), L_f = 0 dB for n = 0. Thus, our path loss model is defined as

$$L_{total} = 39.6 + 28 \log_{10} d, \quad (3)$$

where the number of floors n is 0, frequency f is 2.4 GHz, and distance power loss coefficient N_{PL} is 28 for indoor residential buildings.

2.4 Received and Transmitted Power

From Shannon's law[17], we can derive the required received power P^{RX} for data rate r_h as following:

$$P^{RX}(r_h) = 10 \log_{10}(2^{(r_h / C_{MR})/B} - 1) + N, \quad (4)$$

where B is bandwidth and N is noise. Thus, the transmitted power P^{TX} for data rate r_h is the sum of received power and path loss as follows:

$$P^{TX}(r_h) = P^{RX}(r_h) + L_{total}. \quad (5)$$

2.5 General Power Consumption Model for WMNs

The total power consumption[18] of WMNs is defined as

$$P_{WMN}(r_h) = P_{idle,0} + P_{MR}^{TX}(r_0) + \sum_{h=1}^{n-1} \left\{ \frac{2P_{idle,h} + P_{MR,h}^{TX}(r_h) + P_{MR,h}^{RX}(r_h)}{2} \right\}. \quad (6)$$

2.6 Proposed Cache Power Consumption

Through the observation that CPU frequency f is in proportion to the size of cache[8,9], the proposed cache power consumption is defined as the CPU power consumption of the h^{th} MR for data rate r_h:

$$P_{CPU,h}(r_h) = \begin{cases} P_{idle,h} + P_{cache,h}(r_h) & when\ hit\ ratio\ is\ 1 \\ P_{idle,h} & when\ hit\ ratio\ is\ 0. \end{cases} \quad (7)$$

When a cache hit occurs, it is defined as the sum of idle power and cache power at the h[th] hop. However, when a cache miss occurs, it is defined as only idle power at the h[th] hop. Cache power consumption per bit at the h[th] hop with data rate r_h reflecting traffic passing through the cache is defined as,

$$P_{cache,h}(r_h) = \alpha C_{eff} V_{DD}^2 S_{cache} \delta \rho \beta_{hit,h} d_{req,h} = \left(\frac{\alpha C_{eff} V_{DD}^2 S_{cache} \delta \beta_{hit,h} d_{req,h}}{C_{MR}} \right) r_h, \quad (8)$$

where $\beta_{hit,h}$ is cache hit in the h[th] hop's MR, $d_{req,h}$ is download request in the h[th] hop's MR, and S_{cache} is the size of allocated cache. Both $\beta_{hit,h}$ and $d_{req,h}$ in the h[th] hop's MR are equal to 1 if a cache hit occurs. Otherwise, all are set as 0. Also, δ is a scale factor related to the CPU frequency and the size of cache. Here, α is activity factor ranging from 0 to 1, C_{eff} is effective capacitance, and V_{DD} is supply voltage[9]. Since cache power consumption is reflected according to the data rate at which the cache is actually used, the proposed model increases power consumption as you use more CPU cache. If a requested content is not found in the cache, the cache power consumption is not measured.

2.7 Proposed CHR-Model

In this paper, according to the location on requesting content download into the cache c, cache power consumption can be classified into the following three types: $h < c$, $h = c$, and $h > c$. Here, a range of c equals to the value of h. The power consumption in the h[th] MR $P_{MR,h}(r_h)$ consists of four parts in Fig. 2: idle power consumption $P_{idle,h}$, cache power consumption $P_{cache,h}(r_h)$, received power consumption $P_{RX,h}(r_h)$, and transmitted the power consumption $P_{TX,h}(r_h)$. Considering the caching position c, $P_{MR,h}(r_h)$ is defined as

$$P_{MR,h}(r_h) = \begin{cases} P_{idle,h} & h < c \\ P_{idle,h} + P_{cache,h}(r_h) + P_{TX,h}(r_h) & h = c \\ \dfrac{2P_{idle,h} + P_{RX,h}(r_h) + P_{TX,h}(r_h)}{2} & h > c. \end{cases} \quad (9)$$

Thus, the total power consumption in WMNs is defined as

$$P_{WMN}(r_h) = \sum_{k=0}^{h} P_{MR,h}(r_h). \quad (10)$$

3. Numerical Results

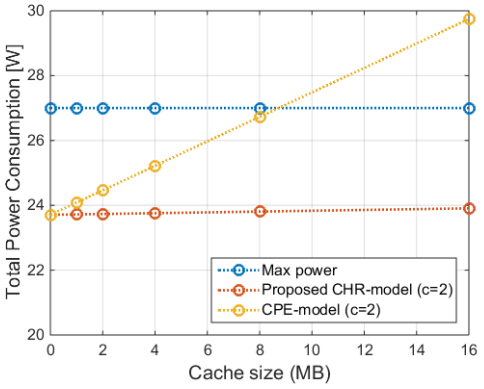

Fig. 3. Total power consumption for increasing the size of cache in WMNs

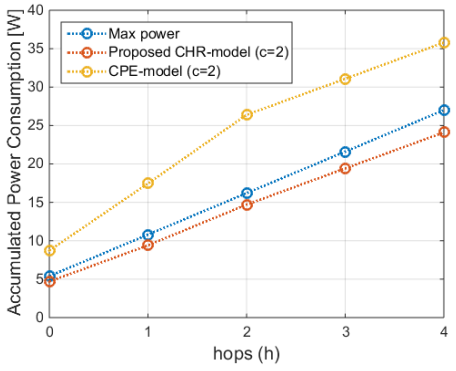

Fig. 4. Accumulated power consumption for increasing hops in WMNs

In this section, we present numerical analysis for the proposed CHR-model and the conventional

CPE-model[4], together with the max power. We consider a TP-Link (TL-WR940N) model as a WiFi MR based on version 2 of datasets[19,20]. A CPU of the TL-WR940N model uses Atheros AR9341 and CPU clock speed provides 535 MHz. Also, static random access memory is used as general CPU cache ranging from level 1 to 3[21]. Here, we assume max power per MR is set as 5.4 Watt[19], idle power of CPU is set as 4.7 Watt, and cache of the 2nd hop's MR from the gateway is requested. That is, $c = 2$ and $\beta_{hit,h} = 1$. In CPE-model, cache power efficiency is defined as 1.5 x 10^{-8} Watt/bit[4]. Also, considering CPU profile[9], we assume that a is 1, C_{eff} is 3 picofarads (pF), V_{DD} is 2.62 V, and δ is 800. Besides, the data rate at the MR with the gateway r_0 is set as 54 Mbps, $\lambda = 1.5$, and the link capacity per MR C_{MR} is set as 600 Mbps.

Fig. 3 shows the total power consumption for increasing the size of cache in WMNs. First, according to the max power of the MR, the total power consumption results as 27 Watt regardless of increasing the size of cache. The proposed CHR-model shows that within the range of the max power, cache power consumption increases proportional to the size of cache. This means because the power consumption from the request into the cache is limited to the maximum bound of MR's power consumption in WMNs. However, the existing CPE-model shows that since the cache power consumption is proportional to the size based on CCNs without any limitation, the maximum power consumption of WMNs is exceeded in case that the size of the cache is over 8 MB.

Fig. 4 shows the accumulated power consumption for increasing hops from the gateway of WMNs. The size of cache is assumed as 32 MB and the location of the requested cache is the 2nd MR. In case of the max power of the MR, all MR's power consumption is summed. Here, the existing CPE-model shows that since content is stored till the location of requested cache in CCNs, the cache power consumption is aggregated from the gateway to the 2nd hop's MR. However, the proposed CHR-model only measures the amount of cache power consumption requested into the 2nd hop's MR.

In our proposed CHR-model, we consider the limitation of the max power of the MR and whether cache hit occurs or not, and then delivered content in the cache is irrelevant to the power consumption.

4. Conclusion

We have presented a CHR-model that considered multihop transmission in WMNs. We have founded CPU frequency is proportional to the size of the cache. Based on the traffic proportional power consumption model of ITU-T standards, we can measure more accurate power consumption than the conventional CPE-model within the bound of maximum power consumption, despite increasing the size of the cache.

REFERENCES

[1] A. Cilfone, L. Davoli, L. Belli & G. Ferrari. (2019). Wireless Mesh Networking: An IoT-Oriented Perspective Survey on Relevant Technologies. *Future Internet, 11(4),* 99.
DOI : 10.3390/fi11040099

[2] L. Leonardi, G. Patti& L. L. Bello. (2018). Multi-hop real-time communications over bluetooth low energy industrial wireless mesh networks. *IEEE Access, 6,* 26505-26519.
DOI : 10.1109/ACCESS.2018.2834479

[3] S. H. Jeon. (2019). User Centric Cache Allocation Schemes in Infrastructure Wireless Mesh Networks. *Journal of Industrial Convergence, 17(4),* 131-137.
DOI : 10.22678/JIC.2019.17.4.131

[4] N. Choi, K. Guan, D. C. Kilper & G. Atkinson.. (2012, June). In-network caching effect on optimal energy consumption in content-centric networking. *In 2012*

IEEE international conference on communications (ICC) (pp. 2889-2894). Ottawa : IEEE.

[5] U. Ashraf. (2016). Energy-aware gateway placement in green wireless mesh networks. *IEEE Communications Letters, 21(1),* 156-159. DOI : 10.1109/LCOMM.2016.2618378

[6] I. REC. (2013). Y. 3022. *Measuring energy in networks,*" Aug.

[7] D. Nicolaescu, A. Veidenbaum & A. Nicolau. (2003, August). Reducing data cache energy consumption via cached load/store queue. I*n Proceedings of the 2003 international symposium on Low power electronics and design (ISLPED)* (pp. 252-257). Seoul : IEEE.

[8] R. Schone, D. Hackenberg & D. Molka. (2012). *Memory Performance at Reduced CPU Clock Speeds: An Analysis of Current x86_64 Processors.* In Presented as part of the 2012 Workshop on Power-Aware Computing and Systems. Hollywood : USENIX.

[9] White Paper. (2004). Enhanced Intel SpeedStep technology for the Intel Pentium M processor. Intel (Online).http://download.intel.com/design/network/papers/30117401.pdf

[10] I. F. Akyildiz & X. Wang. (2005). A survey on wireless mesh networks. *IEEE Communications magazine, 43(9),* S23-S30. DOI : 10.1109/MCOM.2005.1509968

[11] S. Arai, K. Suto & H. Nishiyama. (2014, June). An energy efficient upload transmission method in storage-embedded wireless mesh networks. *In 2014 IEEE International Conference on Communications (ICC)* (pp. 2785-2790). Sydney : IEEE.

[12] R. K. Sheshadri & D. Koutsonikolas. (2013, April). Comparison of routing metrics in 802.11 n wireless mesh networks. *In 2013 Proceedings IEEE INFOCOM* (pp. 1869-1877). Turin : IEEE.

[13] M. Gerla, R. Bagrodia, L. Zhang, K. Tang & L. Wang. (1999, June). TCP over wireless multi-hop protocols: simulation and experiments. *In 1999 IEEE International Conference on Communications (Cat. No. 99CH36311)* (Vol. 2, pp. 1089-1094). Vancouver : IEEE.

[14] J. Jun, P. Peddabachagari & M. Sichitiu. (2003, April). Theoretical maximum throughput of IEEE 802.11 and its applications. *In Second IEEE International Symposium on Network Computing and Applications, 2003. NCA 2003.* (pp. 249-256). Cambridge : IEEE.

[15] H. Y. Kim, S. Rixner & V. S. Pai. (2005). Network interface data caching. *IEEE Transactions on Computers, 54(11),* 1394-1408. DOI : 10.1109/TC.2005.185

[16] P. Series. (2015). Propagation data and prediction methods for the planning of indoor radiocommunication systems and radio local area networks in the frequency range 300 MHz to 100 GHz. *Recommendation ITU-R,* 1238-8.

[17] C. E. Shannon. (1948). A mathematical theory of communication. *Bell system technical journal, 27(3),* 379-423. DOI : 10.1002/j.1538-7305.1948.tb01338.x

[18] P. Serrano, A. Garcia-Saavedra, G. Bianchi, A. Banchs & A. Azcorra. (2014). Per-frame energy consumption in 802.11 devices and its implication on modeling and design. *IEEE/ACM Transactions on networking, 23(4),* 1243-1256. DOI : 10.1109/TNET.2014.2322262

[19] WiFi-Routers | TL-WR940N specifications. *TP-Link(Online).* https://www.tp-link.com

[20] Techdata: TP-Link TL-WR940N v2. *OpenWrt(Online).* https://openwrt.org

[21] S. D. Burd. (2010). *Systems architecture.* Boston : Cengage Learning.

전승현(Seung Hyun Jeon) [정회원]

· Feb., 2017 : KAIST, School of Electrical Engineering (Ph.D.)
· Mar., 2017 Present : Researcher of School of Electrical Engineering at KAIST

· Research Interests : Distributed Network, Energy Consumption of Networks
· E-Mail : creemur@kaist.ac.kr

서용준(Yong-jun Seo) [학생회원]

· Jan, 2010 : KAIST, School of electrical engineering (M.S.)
· Feb., 2010 ~ Present : Student of School of Electrical Engineering at KAIST

· Research Interests : Distributed Network, Energy Consumption of Networks
· E-Mail : yongjun86@kaist.ac.kr