International Journal of Internet, Broadcasting and Communication Vol.12 No.2 30-36 (2020)
http://dx.doi.org/10.7236/IJIBC.2020.12.2.30

IJIBC 20-2-5

A Trapping Behavior of GaN on Diamond HEMTs for Next Generation 5G Base Station and SSPA Radar Application

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Abstract

We demonstrated a successful fabrication of 4 ” Gallium Nitride (GaN)/Diamond High Electron Mobility Transistors (HEMTs) incorporated with Inner Slot Via Hole process. We made in manufacturing technology of 4” GaN/Diamond HEMT wafers in a compound semiconductor foundry since reported [1].

Wafer thickness uniformity and wafer flatness of starting GaN/Diamond wafers have improved greatly, which contributed to improved processing yield. By optimizing Laser drilling techniques, we successfully demonstrated a through-substrate-via process, which is last hurdle in GaN/Diamond manufacturing technology. To fully exploit Diamond’s superior thermal property for GaN HEMT devices, we include Aluminum Nitride (AlN) barrier in epitaxial layer structure, in addition to conventional Aluminum Gallium Nitride (AlGaN) barrier layer. The current collapse revealed very stable up to Vds = 90 V. The trapping behaviors were measured Emission Microscope (EMMI). The traps are located in interface between Silicon Nitride (SiN) passivation layer and GaN cap layer.

Keywords: *GaN/Diamond, HEMTs, Slot Via Hole, Current Collapse, EMMI*

1. INTRODUCTION

III-Nitride High Electron Mobility Transistors (HEMTs) technology for Radio Frequency (RF) application has been of critical importance for commercial and military applications, 50 V Continuous Wave (CW)

Manuscript Received: February. 21, 2020 / Revised: February. 25, 2020 / Accepted: March. 2, 2020
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applications with greater than 10 W/mm saturated output power density are fairly common. A discrete transistor with higher than 100 V S-band 200 W has been demonstrated recently [2].

However, the long-term reliable operation of GaN at high power has been facing unique challenges originating from the simultaneously high electric field and high temperature within a small volume of a HEMTs [3]. With the ever-increasing operating voltage and power, heat dissipation became the key technological barrier hindering future progress of GaN-based RF transistors.

Mitigating self-heating using a Chemical Vapor Deposition (CVD) Diamond cap has resulted in about 20% lower device temperature at an expense of additional process complexity in order to integrate the heat spreading close to the 2DEG channel [4]. On the other front, advances in CVD Diamond technology make synthetic diamond an ideal substrate for GaN devices due to its excellent thermal conductivity (up to 20 W/cmK). In the past few years, with the improvement in microwave CVD Diamond synthesis process, researchers in Raytheon and TriQuint successfully demonstrated enhanced thermal and RF performance on GaN/Diamond HEMTs, reducing the operating junction temperature by 40-45% and tripling the areal RF power density compared to that of GaN/ Silicon Carbide (SiC) [5, 6]. Similarly, GaN/Diamond technology had produced an excellent electro-thermal performance by integrating GaN/Si with CVD Diamond grown on the N-polar backside [7]. Such advances in thermal management have demonstrated that GaN/Si HEMTs have the potential to operate reliably at a very high power density (> 10 W/mm). This characteristics of the best thermal dissipation can be successfully adopt at higher frequency area for operation such as W band [8]. But most of the work was R&D based activity for GaN HEMTs as well as GaN/Diamond HEMTs. The propose of this work is to develop a production level process using fully automated 4 ” foundry fabrication facility (Fab) and to improve RF characteristics of GaN/HEMT bare die as well as a packaged device. In this paper, the development status of high power GaN/Diamond HEMTs results will be addressed, and characteristics of On-wafer Load pull measurement of GaN/Diamond Transistor will be discussed.

2. FABRICATION AND MEASUREMENT

A. 4 ” GaN/Diamond epitaxial wafer

A manufacturing process procedure, exclusive technology holded by RFHIC, for GaN/Diamond epitaxial wafer are shown in Figure 1. The process for epitaxial wafer manufacturing is as follows: Si substrate and transition layer included buffer layer are removed, 35 nm thick intermediate layer is deposited onto exposed GaN epitaxial layer and 120 μm thick CVD Diamond layer is deposited onto the intermediate layer and finally temporary carrier is removed.

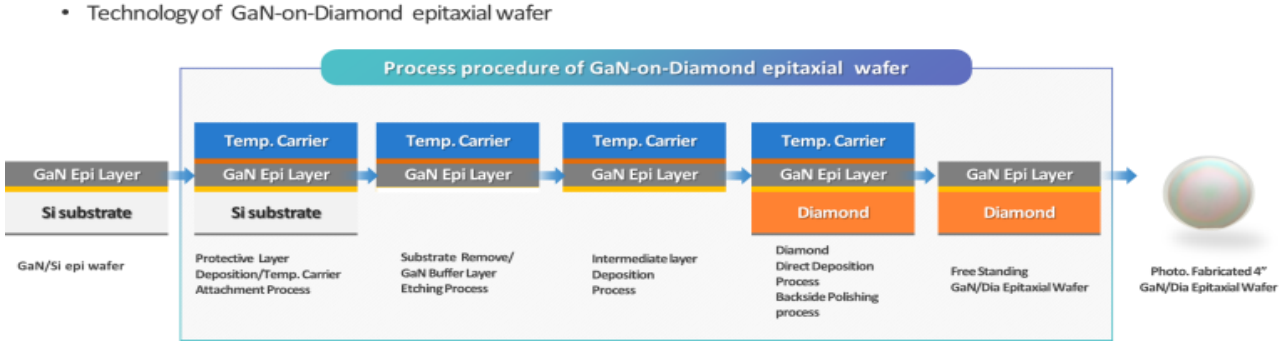


Figure 1. Manufacturing process procedure of GaN/Diamond epitaxial wafer

A TBR of GaN/Diamond epitaxial wafer measured using Thermo-Reflectance measurement method. In

Figure 2, map of TBR for 120 µm thick 4 ” GaN/Diamond epitaxial wafer is shown. The within wafer TBR uniformity is of the order of ±10%, with wafer to wafer TBR average uniformity of the measurement of less than ±15%, for all process lot.

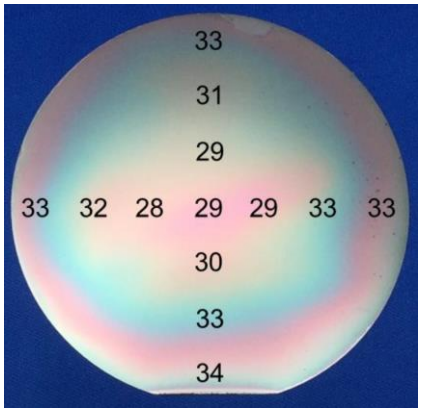


Figure 2. Map of TBR (Unit : m2K/GW) for 120 µm thick 4 ” GaN/Diamond epitaxial wafer

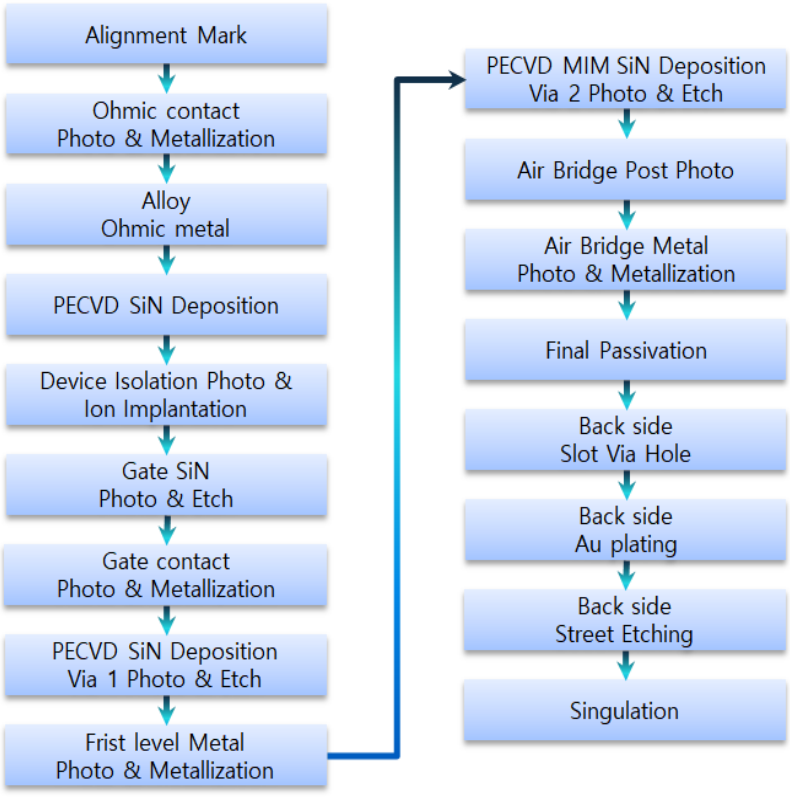


Figure 3. Standard GaN/Diamond HEMTs process Flow

B. 0.5 µm *GaN/Diamond HEMTs*

A 4 ” GaN/Diamond HEMT epitaxial wafer was produced by RFHIC and processed at a foundry Fab using standard existing 4 ” toolset as in GaN/SiC and GaN/Si production.

The typical 4 ” GaN/Diamond epitaxial wafer has a thickness from 110 µm to 130 µm. Specially developed wafer bonding process effectively controlled BOW and Warpage during the wafer process. A stiff

carrier with strong bonding media is necessary to let these tools accept 4 ” GaN/Diamond epitaxial wafers. Especially, at gate lithography (0.5 µm) process using Stepper, wafer bowing and poor thickness uniformity presented extraordinary challenges.

Using a standard GaN/SiC HEMTs process procedure, 0.5 µm GaN/Diamond HEMTs was fabricated with high temperature ohmic alloying, SiN deposition, implant isolation defining the active layer, gate formation involving a gate SiN etch and gate metal deposition, and anneal. Then 2nd SiN layer is deposited to passivate the gates. M1 interconnect, 3rd SiN layer, air bridge, and final passivation are followed to complete GaN/Diamond HEMTs wafer surface. Figure 3 illustrates the simplified process flow. A 0.5 µm GaN/Diamond HEMT basically followed these standardized production level process route incorporated with Inner Slot Via Hole process. In Figure 4, 4 ” GaN/Diamond HEMTs wafer is shown a front side process and a back side process completion in standard 4 " foundry Fab.

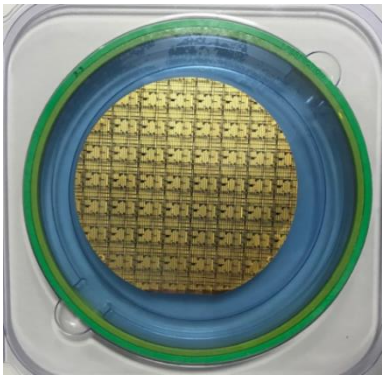


Figure 4. 4 ” 0.5 µm GaN/Diamond HEMTs wafer

A damage-free Inner Slot Via Hole process recipe was successfully developed for GaN/Diamond HEMTs using a Laser Drilling process. This unique process was made on 80 µm
Source pad incorporated with round shape 20 µm dia. hole.

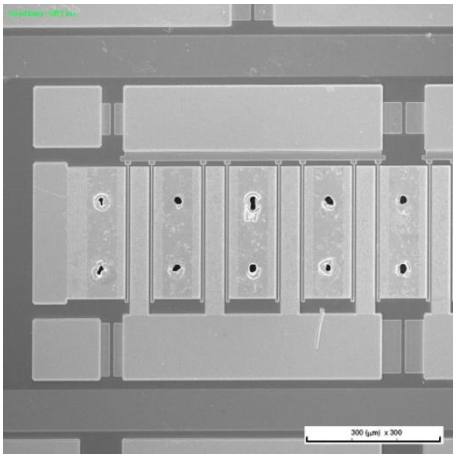


Figure 5. Inner Slot Via Hole shape on Source pad

As shown Figure 5, Inner Slot Via Hole was controlled by taper characteristics during Laser Drilling process in order to increase Au plating process yield.

C. Current Collapse measurement

A current collapse is very important because the output power density at RF frequency is limited by this effect. Several mechanisms have been proposed as source for the current collapse such as gate biasing induced non-uniform strain, charging up of a second virtual gate [9], and hot electron injection and trapping in the buffer [10]. Different approaches have proposed to eliminate the current collapse such as passivation with Si3N4 film, and surface charge control with GaN cap layer. In Figure 6, measurement condition of current collapse is shown.

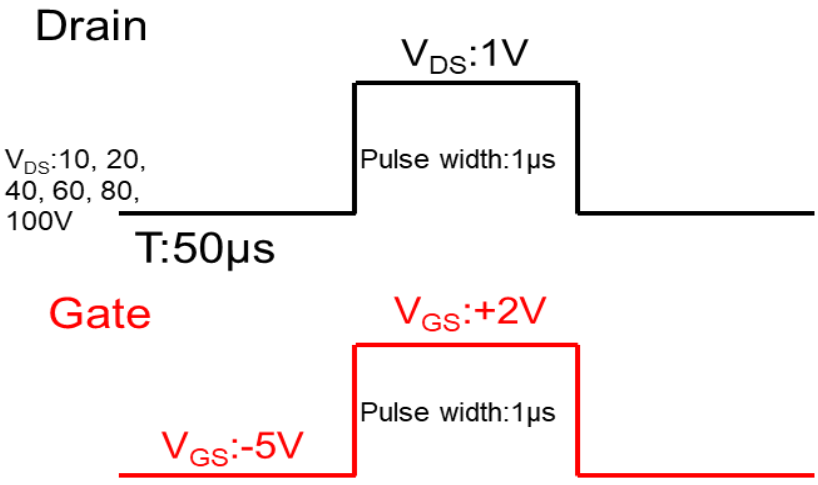


Figure 6. Measurement condition of current collapse for three-terminal 0.5 μm GaN/Diamond HEMTs

D. EMMI (Emission Microscope) measurement

Surface trap is another main factor to decrease performance under the RF frequency condition. Hot spot due to surface trap can be verified which area has surface trap. EMMI is capable of detecting light wavelength between 350 nm – 1100 nm that is used for detecting leakage current resulting from surface trap.

3. MEARUEMENT RESULT

The On-wafer Load pull measurement results of 4 ” GaN/Diamond HEMT are announced that 0.6 mm GaN/Diamond HEMTs revealed RF power saturated at 41.3 dBm, corresponding to a world record of 22.5 W/mm in power density [11].

At high power operation of 0.5 μm GaN/Diamond HEMTs at 2 GHz, drain efficiency was decreased down to 55 % rapidly due to trapping effect when drain bias applied 80 V.

We found that test results of current collapse are gradually increased up to Vds = 90 V. However, current collapse has different slope when 0.5 μm GaN/Diamond HEMTs was operated at Vds = 100 V.

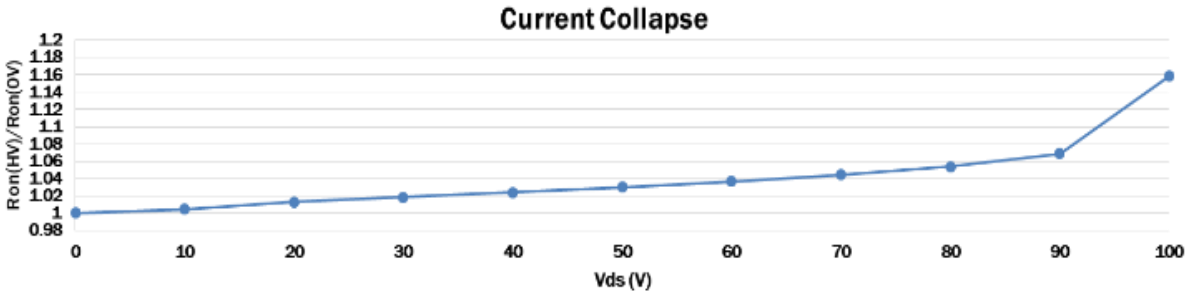
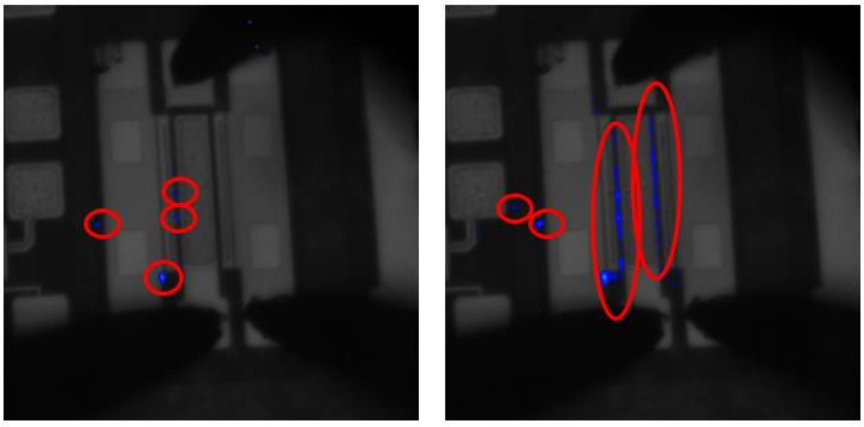


Figure 7. Current Collapse measurement results of 0.5 µm

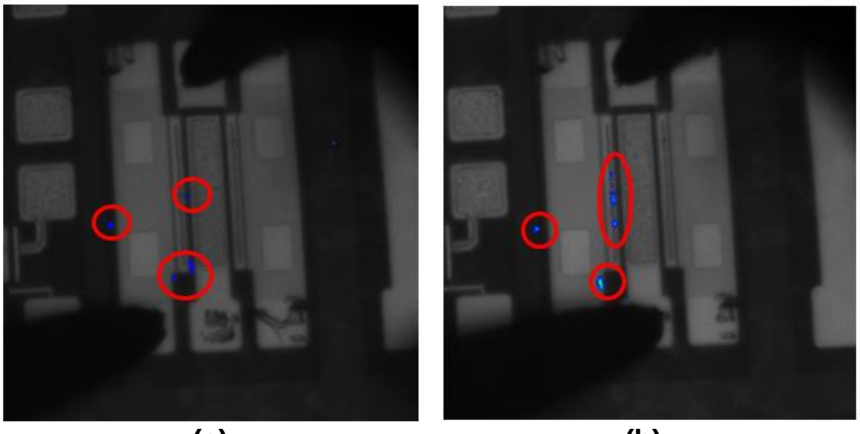
Figure 7 shows the current collapse in the measurement range from Vds = 0 V to Vds = 100 V. GaN/Diamond HEMTs at Vds = 0 V – 100 V.

EMMI was used to evaluate the trap location of the 0.5 µm GaN/Diamond HEMTs. Figure 8 shows the EMMI results of the 0.5 µm GaN/Diamond HEMTs at Vds = 40 V / Vgs = -8 V , Vds = 50 V / Vgs = -8 V, respectively. GaN/Diamond HEMTs at (a) Vds = 40 V / Vgs = -8 V, (b) Vds = 50 V / Vgs = -8 V.



(a) **(b)**

Figure 8. EMMI images of 0.5 µm gate length 2 X 300 µm



(a) **(b)**

Figure 9. EMMI images of 0.5 µm gate length 2X300 µm

Figure 9 shows the EMMI images at Vgs = 50 V and Vdg = 60 V, respectively. GaN/Diamond HEMTs at (a) Vgs = 50 V, (b) Vdg = 60 V.

EMMI images are revealed that traps are located in interface between SiN passivation layer and GaN cap layer. Bulk traps located in GaN buffer layer can be possibly minimize using developed flip process. Current collapse was induced from their traps located in interface between SiN passivation layer and GaN cap layer when drain bias was increased up to 100 V.

4. CONCLUSION

RFHIC & LIG NEX1 continue to make significant progress in GaN/Diamond HEMTs manufacturing technology, including production level process development. On 0.5 μm GaN/Diamond HEMTs, we verified that trap was located in interface between SiN passivation layer and GaN cap layer. We obtained that current collapse can be gradually increasing up to Vds = 90V, however, current collapse was changed their behavior at Vds = 100 V due to increasing surface leakage current. EMMI revealed correlation results that leakage current was located in surface. We believe that surface leakage current of GaN/Diamond HEMTs can be induced from flip process in order to make a GaN/Diamond epitaxial wafer. It can be possibly realize to make next generation GaN/Diamond epitaxial wafer to minimize surface leakage current using additional surface passivation layer incorporated.

To our knowledge, GaN/Diamond HEMT is going to make a better performance in terms of efficiency at RF operation when surface passivation process can be eliminate surface traps.

REFERENCES

[1] Mo Wu, Won Sang Lee et al, “Fabrication of 4-inch GaN/Diamond HEMT in Compound Semiconductor Foundry.” 2018 International Conference on Compound Semiconductor Manufacturing Technology, May 2018.

[2] G. Formicone, J. Cluster, and J. Berger, “First Demonstration of GaN-SiC RF Technology Operating Above 100 V in S-band”, 2017 International Conference on Compound Semiconductor Manufacturing Technology, May 2017.

[3] D.J. Meyer et al, IEEE Electr. Dev. Lett., vol. 35, pp. 1013-1015, 2014.

[4] M.J. Tadjer et al, IEEE Electr. Dev. Lett., vol. 33, pp. 23-25, 2012.

[5] D. Altman, M. Tyhach, J. McClymonds, S. Kim, S. Graham, J. Cho, K. Goodson, D. Francis, F. Faili, F. Ejeckam, and S. Bernstein, “Analysis and Characterization of Thermal Transport in GaN HEMTs on Diamond Substrates, I-THERM 2014 Conference in Orlando, FL.

[6] J. Pomeroy, M. Benardoni, A. Sarua, A. Manoi, D.C. Dumka, D.M. Fanning and M. Kuball, “Achieving the Best Thermal Performance for GaN-on-Diamond” 35th IEEE Compound Semiconductor IC Symposium (CSICS) Oct. 13-16, 2013.

[7] D.C. Dumka et al., Proc. CSICS, 2013. DOI: http://doi.org/10. 1109/CSICS. 2013. 6659225.

[8] Sun-il Kim, “Design and Fabrication of SSPA module in Ku band for Satellite Terminals.” Journal of Institute of Internet, Broadcasting and Communication (IIBC) Vol. 16, No. 4, pp. 59-64, Aug. 31, 2016. DOI: http://dx. doi.org/10.7236/JIIBC.2016.16.4.59

[9] R. Vetury, N. Q. Zhang, et al., “The impact of surface state on the DC and RF characteristics of AlGaN/GaN HFETs.” IEEE Trans. Electron Devices, vol. 48, pp.560-566. Mar. 2001.

[10] S. Binari, K. Ikossi, et al., “Trapping effects and microwave power performance in AlGaN/GaN HEMTs,” IEEE Trans. Electron Devices, vol 48, pp.465-471, Mar. 2001.

[11] Won Sang Lee et al, “A GaN/Diamond HEMTs with 23 W/mm for Next Generation High Power RF Application,” 2019 International Microwave Symposium, June 2019.