Bidirectional DC-DC Converter Based on Quasi-Sepic for Battery Charging System

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〈Abstract〉

In order to satisfy the voltage levels of the low voltage battery side and high voltage DC bus, a high voltage gain with bidirectional operation is required. In this system, the cost effectiveness of the design is a critical factor; therefore, the system should be designed using a small number of components. This paper propose a novel bidirectional converter composed with a quasi-sepic and switched-indictor network. The proposed converter consists a small number of components with a high voltage gain ratio. Detailed analysis are made with respect to the operating mode, number of components, voltage and current ripple and efficiency. To verify performance of the proposed converter, simulation was performed is this paper. The simulation results are shown to verify the feasibility and performance of the proposed bidirectional converter.

Keywords : energy storage system (ESS), Quasi-Sepic converter, Transformerless dc-dc converter, High sep-up converter

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1. Introduce

Energy sorage system(ESS) with DC-DC converters operating in bidirectional is indispensable in microgrids, electric vehicles (EVs), and transportation system based on renewable energy [1,2]. Bidirectional DC-DC converters are essential for the transfer and conversion of the electrical energy of the storage units, which operate the charge and discharge processes. In general, the realization of highly efficient converters with large conversion ratios and high power densities is a significant challenge in the power electronic fields.

According to the conventional bidirectional converters with transformer [3]-[5], this type of converter benefits from a simple structure and easy to operate. However, the leakage indictance loss due to the high-frequency transformer results in a low converter efficiency. In [6]-[8], DC-DC converters operating in bidirectional with high conversion ratio were proposed. Practically, there have more power switches in these converters which led to increasing the conduction losses and the cost efficiency, lead to decrease the efficiency.

To overcome these problems, converters based on the integration of the boost converter with the Cuk, SEPIC, and buck-boost converters were presented in [9-11]. Which attained a high voltage gain ratio and low stresses across the power switches. However, the converters operate only in unidirectional mode, furthermore, the voltage and current stresses on the switches were not analysis in detail. Therefore, a novel DC-DC converter with quasi-sepic and switched inductor network are proposed in this paper.

In order to analyze the proposed converter, detailed analysis are processed with respected to the operating mode, number of components, voltage and current ripple and efficiency. The voltage ripple of the proposed converter is relatively low, which increase design flexibility for the passive components. The simulation results are shown to verify the feasibility and performance of the proposed bidirectional converter.

2. Bidirectional DC-DC converter with wide voltage conversion ratio

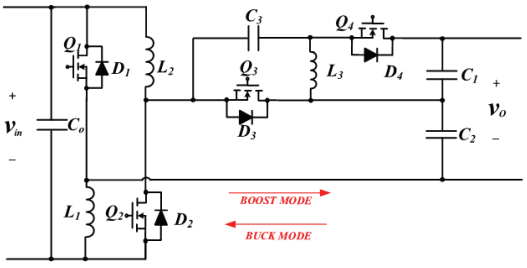


Fig. 1 Proposed converter

Figure 1 shows the schematic diagram of the proposed converter. The proposed converter consist of four power switches Q_1-Q_4; capacitors C_0-C_3, in addition, there are three in ductors L_1, L_2 and L_3 in the

converter. The proposed converter was analyzed based on the assumption that the converter operate in continuous conduction mode (CCM), and that all the components are analyzed in ideal condition.

2.1 Construction of the proposed converter.

The presented converter is presented in Figure 1. The steady-state analyses with respect to the switching states of the converter are shown as follows:

When the converter operates in the boost mode, the power flows from the battery side to the dc bus side. In this mode, the gate signal of Q_1 and Q_2 are complementary to Q_3 and Q_4. The main theoretical waveform of the proposed converter in CCM are presented in Figure 3, and the topological states are described in Figure 2.

[t0-t1]: When the circuit operates in this case. Switches Q_1 and Q_2 are ON, and switches Q_3 and Q_4 are turned OFF, as described in Figure 2 (a), during this time, the L_1 and L_2 are charged by the input voltage V_{in}, L_3 and C_2 are charged through C_2, C_1 and C_2 are discharged through the load resistance. The equation can be derived:

$$\begin{cases} U_{L1} = U_{low} \\ U_{L2} = U_{low} \\ U_{L3} = U_{C2} - U_{C3} \\ U_{C1} + U_{C2} = U_{high} \end{cases} \quad (1)$$

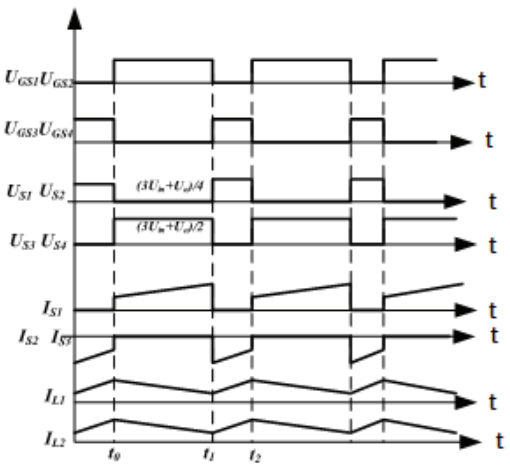
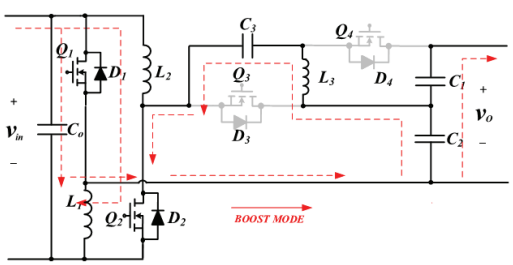
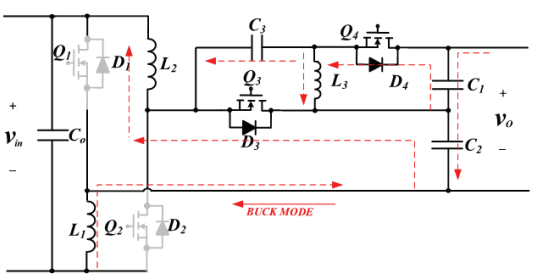


Fig. 3 Main waveforms of boost mode.

$$\begin{cases} i_{L3} = -i_{C2} \\ i_{C3} = i_{L3} \\ i_{C1} = -i_{high} \end{cases} \quad (2)$$



(a)



(b)

Fig. 2 Topological states of the converter in boost mode (a) [t0-t1] (b) [t1-t2]

where U_{L1}, U_{L2}, U_{L3} represent the voltages on the inductance. U_{C1}, U_{C2}, and U_{C3} are the voltage on the capacitors. U_{high} and U_{low} are shown as the voltage on the DC bus side and voltage side. I_{high} and I_{low} are shown as the current on the DC bus side and battery side. These symbols are applicable to all of the converter in this paper.

[t1-t2]: When the circuit operates in this case. Switches Q_1 and Q_2 are OFF, and switches Q_3 and Q_4 are turned ON, as described in Figure 2 (b), L_1 and L_2 are discharged through Q_3 and C_2, L_3 is discharged through Q_4, output voltage is boosting through C_1 and C_2. The formulas below were derived for this state.

$$\begin{cases} U_{L2}+U_{L1}=U_{low}-U_{C2} \\ U_{L3}=-U_3=-U_1 \\ U_{C1}+U_{C2}=U_{high} \end{cases} \tag{3}$$

$$\begin{cases} i_{L1}+i_{C3}-i_{L2}=i_{C2} \\ i_{C3}+i_{L2}-i_{C1}=i_{high} \end{cases} \tag{4}$$

By employing the ampere-second balance law to the inductance on the basic of (1) and (3), the voltage conversion ratio can be calculated as

$$M=\frac{1+3d_{Boost}}{1-d_{Boost}} \tag{5}$$

By employing the ampere-second balance law to the capacitors on the basic of (2) and (4), the average value of the inductor currents can be derived as

$$\begin{cases} I_{L1}=I_{L2}=\dfrac{1+3d_{Boost}}{1-d_{Boost}}I_{high} \\ I_{L2}=I_{high} \end{cases} \tag{6}$$

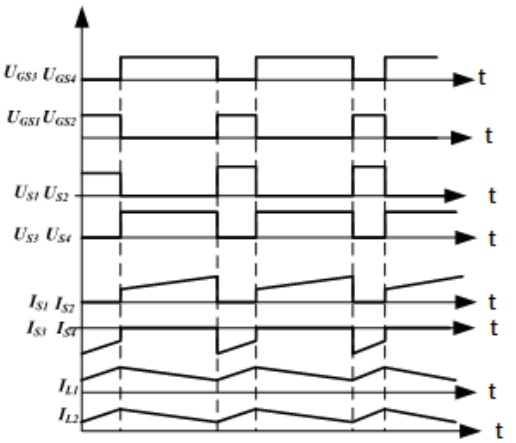


Fig. 4 Main waveforms of buck mode.

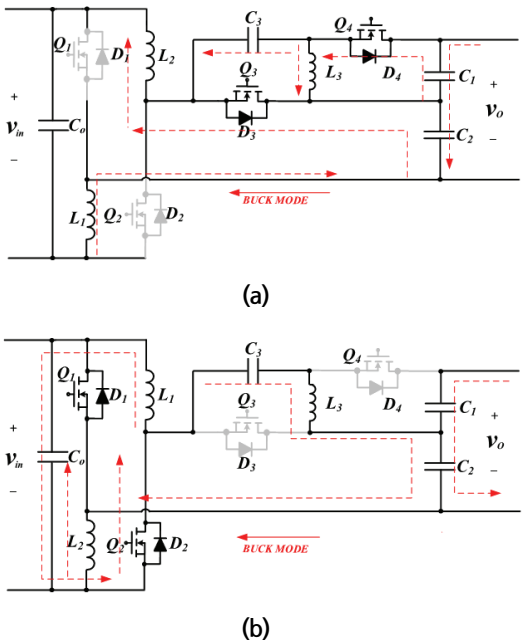


Fig. 5 Topological states of the converter in buck mode (a) [t0-t1] (b) [t1-t2]

When the proposed converter is applied to the buck mode, this is reverse to the boost mode, in which the gate signal of Q_1 and Q_2 is complementary with Q_3 and Q_4.. The characteristic waveform of the presented converter in CCM are described in Figure 4, and the topological stages are depicted in Figure 5.

[t0-t1]: When the circuit operates in this case. Switches Q_1 and Q_2 are ON, and switches Q_3 and Q_4 are turned OFF, as described in Figure 5 (a).L_1 and L_2 are charging by C_2, then L_3 is charged by C_1 and C_3. The equation can be derived:

$$\begin{cases} U_{L1} = U_{L2} = (U_{C2} - U_{low})/2 \\ U_{L3} = U_{C3} = U_{C1} \\ U_{C1} + U_{C2} = U_{high} \end{cases} \tag{7}$$

$$\begin{cases} i_{C1} = i_{L1} + i_{L2} + i_{C3} - i_{L3} \\ i_{high} = i_{L3} - i_{C2} \end{cases} \tag{8}$$

[t1-t2]: In the inductance charging mode, switching state is opposed to previous operation. In this state, C_3 and L_3 are in series connection to charge C_2. Moreover, L_1 and L_2 also discharging to C_0 through Q_1 and Q_2 on the basis of Figure 5(b). The equation can be derived:

$$\begin{cases} U_{L1} = U_{L2} = -U_{low} \\ U_{L3} = U_{C3} - U_{C2} \\ U_{C1} + U_{C2} = U_{high} \end{cases} \tag{9}$$

$$\begin{cases} i_{L3} = i_{L3} \\ i_{L1} = i_{L2} = i_{C2} \\ i_{C1} = i_{high} \end{cases} \tag{10}$$

Taking into account the volt-second balance law on L_1 and L_2 according to (8) and (10), the buck conversion Mbuck of the proposed converter in CCM can be obtained as

$$M_{Buck} = \frac{d_{Buck}}{4 - 3d_{Buck}} \tag{11}$$

Moreover, it is concluded that the capacitor voltage can be deduced as

$$\begin{cases} U_{C1} = U_{C3} = \dfrac{U_{low}}{4 - 3d_{Buck}} \\ U_{C2} = \dfrac{(1 - d_{Buck})\,U_{low}}{d_{Buck}} = \dfrac{(1 - d_{Buck})\,U_{high}}{4 - 3d_{Boost}} \end{cases} \tag{12}$$

Using the ampere-second balance law of capacitors with (9) and (11), the average inductor current I_{L1} and I_{L2} of inductances L_1 and L_2 can be obtained as

$$\begin{cases} I_{L1} = I_{L1} = I_{low} \\ I_{L3} = \dfrac{d_{Buck}}{4 - 3d_{Buck}} I_{low} \end{cases} \tag{13}$$

2.2 Comparisons with conventional converter

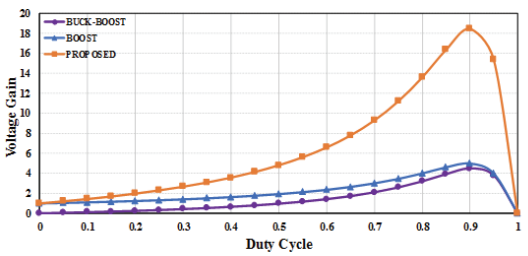


Fig. 6 Voltage gain ratio comparison between proposed converters and conventional converters with parasitic resistance

In general, the losses of the inductor, capacitor, and switch cause the parasitic effects on the converter. In these components, the inductor parasitic resistance has the greatest influence on the converter voltage conversion ratio. Therefore, when considering the influence of the inductance parasitic resistance, the voltage gain ratio of the conventional converter and the proposed converters can be expressed as follows

$$M_{Boost} = \frac{1}{1-D}\left(\frac{1}{1+\frac{r1}{(1-D)^2 R}}\right) \quad (14)$$

$$M_{Buck-Boost} = \frac{D}{1-D}\left(\frac{1}{1+\frac{r1}{(1-D)^2 R}}\right)$$

$$M_{P-converter} = \frac{1+3D}{1-D}\left(\frac{1}{1+\frac{r1}{(1-D)^2 R}}\right)$$

which D is the duty cycle, and r_l represent as the inductor parasitic resistance, R is the load resistance.

These three equations are derived by applying the volt-second balance law to inductors, if R/r_l is set to 0.01, the voltage gain ratio can be obtained under different duty cycle.

The comparison between the voltage conversion ratio and duty cycles of the proposed converter are shown in Figure 6. It can be seen that when considering the influence of parasitic components, voltage gain ratio sharply decrease at large duty cycle. However, under the same duty cycle, the voltage gain ratio of the proposed converters is higher than conventional converters. Therefore, under large duty cycle, the proposed converter has a better setp-up voltage performance than the conventional converters.

2.3 Voltage and current stresses on the switches

Voltage stress across the power switches: in accordance with the above analysis, as shown in Figure 4 and Figure 6. In addition, by employing the Kirchhoff voltage law (KVL) to the switches, it can be derived as

$$\begin{cases} U_{Q1-Boost} = U_{Q2-Boost} = \frac{U_{low}}{1-d_{Boost}} = \frac{U_{high}}{1+3d_{Boost}} \\ U_{Q3-Boost} = U_{Q4-Boost} = \frac{2U_{low}}{1-d_{Boost}} = \frac{2U_{high}}{1+3d_{Boost}} \end{cases} \quad (15)$$

$$\begin{cases} U_{Q1-Buck} = U_{Q2-Buck} = \frac{U_{high}}{4-3d_{Buck}} \\ U_{Q3-Buck} = U_{Q4-Buck} = \frac{2U_{high}}{4-3d_{Buck}} \end{cases} \quad (16)$$

By using above analysis and the Kirchoff voltage law (KVL) to the switches, the voltage stress on the switches can be obtained as

$$\begin{cases} I_{Q1-Boost} = I_{Q2-Boost} = \frac{I_{high}}{1-d_{Boost}} \\ U_{Q3-Boost} = U_{Q4-Boost} = \frac{1}{1-d_{Boost}} I_{high} \end{cases} \quad (17)$$

$$\begin{cases} I_{Q1-Buck} = I_{Q2-Buck} = \frac{I_{low}}{4-3d_{Buck}} \\ I_{Q3-Buck} = I_{Q4-Buck} = \frac{I_{low}}{4-3d_{Boost}} \end{cases} \quad (18)$$

2.4 Selection of inductors and capacitors

According to the current ripple of the inductances, the value of inductance can be calculated.

$$\begin{cases} I_{L1} = I_{L1} = \dfrac{1+3d_{Boost}}{1-d_{Boost}} I_{high} \\ I_{L2} = I_{high} \end{cases} \tag{19}$$

$$\begin{cases} L_1 = L_2 = \dfrac{(1-D)\, V_{low}^2\, DT}{r_i\%\,(1+3D)P} \\ L_3 = \dfrac{V_{low}^2\, DT}{r_i\%\, P} \end{cases} \tag{20}$$

The capacitors are designed according to the capacitor voltage ripple.

$$\begin{cases} i_{L3} = -i_{C2} = i_{Q2} = \dfrac{1}{1-d_{Boost}} i_{high} \\ i_{L3} = i_{C3} = i_{Q2} = \dfrac{1}{1-d_{Boost}} i_{high} \\ i_{C1} = -i_{high} \end{cases} \tag{21}$$

According to the current relationship of the capacitance, it can be derived that

$$\begin{cases} C_1 \dfrac{\triangle_{C1}}{DT} = -\dfrac{P_O}{V_O} \\ C_2 \dfrac{\triangle_{C1}}{DT} = -\dfrac{P_O}{(1-d_{Boost})\, V_O} \\ C_3 \dfrac{\triangle_{C1}}{DT} = -\dfrac{P_O}{(1-d_{Boost})\, V_O} \end{cases} \tag{22}$$

The value of capacitance can be attained that

$$\begin{aligned} C_1 &= -\frac{P_O DT}{r_v\%\, V_o} \\ C_2 &= -\frac{P_O DT}{r_v\%\, V_o (1-d_{Boost})} \\ C_2 &= -\frac{P_O DT}{r_v\%\, V_o (1-d_{Boost})} \end{aligned} \tag{23}$$

3. Simulation results

To verify the theoretical analysis of the proposed converter, a 200-W prototype was simulated in PSIM. The parameters of the test prototype are presented in Table1. A double loop proportional-integral (PI) control, (inner current control loop and outer voltage control loop) as shown in Figure 7.

PSIM simulation results in boost mode is shown in Figure 8, when the duty cycle is equal to 0.6, the input voltage is 50V, and

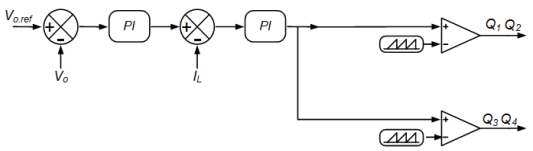


Fig. 7. Bidirectional power flow control strategy of proposed converter

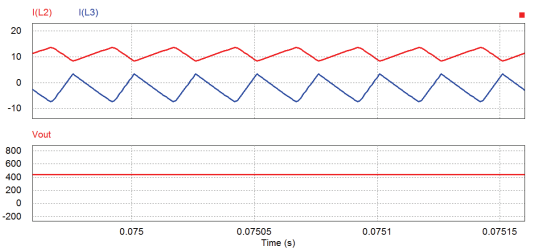


Fig. 8 Simulation results of the inductors and output voltage in Boost mode

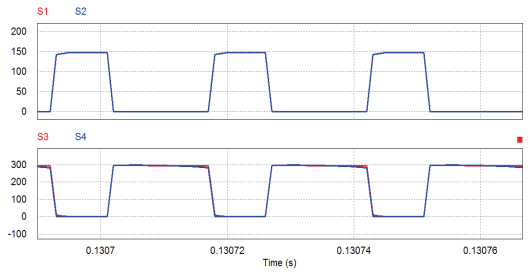


Fig. 9 Simulation results of the voltage across Q1-Q4 in boost mode

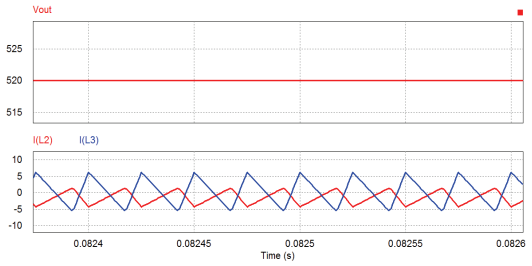


Fig. 10 Simulation results of the inductors and output voltage in Buck mode

the output voltage is equal to 400V, which is satisfy the theoretical analysis.

The voltage stress waveforms of Q_1-Q_4 in boost mode are presented in Figure 9. The voltage stresses on Q_1-Q_2 were 85V, which indicates the voltage stresses on Q_1-Q_2 are satisfy the equation (15), and the voltage stresses on Q_3-Q_4 were 240V, which also satisfy the equation (15).

PSIM simulation results in boost mode is shown in Figure 9, when the duty cycle is equal to 0.6, the input voltage is 65V, and the output voltage is equal to 520V, which is satisfy the theoretical analysis.

The voltage stress waveforms of Q_1-Q_4 in buck mode are presented in Figure 10. The voltage stresses on Q_1-Q_2 were 85V, which indicates the voltage stresses on Q_1-Q_2 are satisfy the equation (15), and the voltage stresses on Q_3-Q_4 were 240V, which also satisfy the equation (15).

Characteristic of the proposed converter is shown in Table2, the duty cycle represent the PWM signal operate in Boost mode.

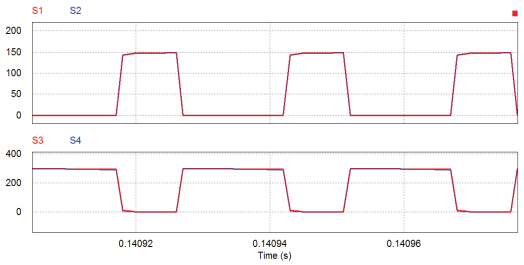


Fig. 11 Simulation results of the voltage across Q1-Q4 in buck mode

Table 1. Parameters of the proposed converter

Parameters	Symbol	Value
Battery voltage	Vl_{ow}	40-130[V]
Output voltage	V_{high}	250[V]
Inductor	L_1 L_2	102uH
Inductor	L_3	150uH
Capicitor	C_3	5uF
Output power	P_o	200W

4. Conclusion

In this study, a novel bidirectional DC-DC converter without transformer and with high voltage gain was developed. The set of converter benefit from a high voltage

Table 2. Characteristic of the proposed converter

Input current	Discontinous
Switch voltage stress (Q1 Q2)	$V_{high}/(1+3D)$
Switch voltage stress (Q3 Q4)	$2V_{high}/(1+3D)$
Voltage gain ratio	(1+3D)/(1-D)
Num, of switches	4
Num, of inductors	3

conversion ratio in the boost and buck modes. Detailed analysis were made with respect to the opearting mode, number of components, current and voltage stresses on the switches. Finally, the experiment results were presented to verify the feasibility of the proposed converter. The results confirm that the converter provide a good trade-off between the voltage gain ratio, voltage and current stresses, and the components count.

References

[1] Yilmaz, M.; Krein, P. T. Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles. *IEEE Trans. Power. Electron.* 2013, 28, 2151–2169.

[2] Han, Y.; Chen, W.; Li, Q. Energy Management Strategy Based on Multiple Operating States fora Photovoltaic/Full Cell/Energy Storage DC Microgrid. *Energies* 2017, 10, 136.

[3] Inoue, S.; Akagi, H.S. A bidirectional isolated dc–dc converter as a core circuit of the next-generation medium-voltage power conversion system. *IEEE Trans. Power Electron.* 2007, 22, 535-542.

[4] Liu, C.; Chau, K.T.; Wu, D.; Gao, S. Opportunities and challenges of vehicle-to-home, vehicle-to-vehicle, and vehicle-to-grid technologies. *Proc. IEEE*, 2013, 101, 2409–2427.

[5] Jin, K.; Yang, M.; Ruan, X.; Xu, M. Three-level bidirectional converter for fuel-cell/ battery hybrid power system. *IEEE Trans. Ind. Electron*. 2010, 57, 1976-1986.

[6] Fang, X.; Ji, X. Bidirectional power flow Z-source dc-dc converter. IEEE Vehicle Power and Propulsion Conference (VPPC), Harbin, Hei Longjiang, China, 3-5 Sept 2008; pp. 1-5.

[7] J. Y. Shin, J. S. Song, "Time Synchronized Cluster(TSC) for Power Conservation in Ad Hoc Networks", Korea Institute Of Communication Science, pp. 560-563, Nov. 2003.

[8] Li, Cong.; Herrera, Luis. Design and implementation of a bidirectional isolated Cuk converter for low-voltage and high-current automotive DC source applications. *IEEE Trans. Veh. Technol.* 2014, 63, 2567-2577.

[9] Liang, T.J.; Lee, J.H. Novel-high-conversion-ratio high efficiency isolated bidirectional DC-DC converter. *IEEE Trans. Ind. Electron.* 2015, 62, 4492-4503.

[10] Zhang, Y.; Liu, Q.; Li, J.; Sumner, M. A Common Ground Switched-Quasi-Z-Source Bidirectional DC–DC Converter With Wide-Voltage-Gain Range for EVs With Hybrid Energy Sources. *IEEE Trans. Ind. Electron.* 2018, 65, 5188-5200.

[11] Abutbul, O.; Gherlitz, A.; Berkovich, Y.; Ioinovici, A. Step-up switching-mode converter with high voltage gain using a switched capacitor circuit. *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.* 2003, 50, 1098-1102.

(Manuscript received March 5, 2020;
revised March 20, 2020; accepted March 30, 2020)