Review Paper

J. Korean Inst. Electr. Electron. Mater. Eng.
Vol. 33, No. 2, pp. 88-92 March 2020
DOI: https://doi.org/10.4313/JKEM.2020.33.2.88
ISSN 1226-7945(Print), 2288-3258(Online)

Self Heating Effects in Sub-nm Scale FinFETs

Khushabu Agrawal[1], Vilas Patil[2], Geonju Yoon[1], Jinsu Park[1], Jaemin Kim[1], Sangwoo Pae[3], Jinseok Kim[3], Eun-Chel Cho[1], and Yi Junsin[1]

[1] Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea
[2] Materials and Devices Laboratory of Nanoelectronics, North Maharashtra University, Jalgaon M.S. 425001, India
[3] Technology Quality & Reliability Foundry Division, Samsung Electronics Co., LTD., Suwon 16674, Korea

(Received September 3, 2019; Revised November 20, 2019; Accepted November 29, 2019)

Abstract: Thermal effects in bulk and SOI FinFETs are briefly reviewed herein. Different techniques to measure these thermal effects are studied in detail. Self-heating effects show a strong dependency on geometrical parameters of the device, thereby affecting the reliability and performance of FinFETs. Mobility degradation leads to 7% higher current in bulk FinFETs than in SOI FinFETs. The lower thermal conductivity of SiO_2 and higher current densities due to a reduction in device dimensions are the potential reasons behind this degradation. A comparison of both bulk and SOI FinFETs shows that the thermal effects are more dominant in bulk FinFETs as they dissipate more heat because of their lower lattice temperature. However, these thermal effects can be minimized by integrating 2D materials along with high thermal conductive dielectrics into the FinFET device structure.

Keywords: FinFETs, Self heating effects, Thermal resistance, Lattice temperature

1. INTRODUCTION

Moving from Planar to multigate FinFETs in the sub 20 nm technology region, the narrow conduction path between channel and substrate due to miniaturization results in the heating of the devices termed as the self-heating effect (SHE) which have become a crucial issue now a day [1]. This SHE shows different behaviour for Bulk and Silicon on insulator (SOI) FinFETs and can be studied through several device parameters like drain to source current (I_{ds}), thermal resistance (R_{th}), carrier mobility (μ), saturation velocity (η) and threshold voltage (V_{th}) [2]. Within these parameters, the mobility strongly depends on the temperature which can ultimately lead to the drain current reduction and affect the device reliability and device performance therefore, it became essential to study this thermal effects and try to found out possible solutions to overcome it. There are several mechanisms represented by research groups working in this area to study these thermal effects which includes: 1) four point gate resistance method where, the measurement parameter is the device temperature (ΔT) have great impact on the drive current and reliability 2) the AC conductance method relates to the thermal resistance (R_{th}) 3) the pulse method related to trap mechanism, etc [3]. Among these methods, the AC conductance method has been used widely to study the thermal effects in bulk and SOI FinFETs.

In this paper, we reviews the self heating effects in bulk and SOI FinFETs, the overview of different techniques used to investigate these thermal effects has been carried out mainly. Furthermore, the thermal effect on several parameters in n type and p type bulk and SOI FinFETs

✉ Eun-Chel Cho; echo0211@skku.edu
Yi Junsin; junsin@skku.edu

Copyright ©2020 KIEEME. All rights reserved.
This is an Open-Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/3.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

has been discussed in more detail. The section two of this paper describes the techniques while, results are discussed in section three. The fourth section summarizes the paper.

2. RESEARCH METHOD

2.1 Different mechanisms for SHE measurements

The self heating in the FinFET increases the △T and decreases the drive current (I_d) due to charge carrier induced lattice vibrations and therefore directly proportional to the drive current density and the thermal resistance R_{th} [3]. However, this R_{th} is strongly dependant on geometrical parameters of devices like gate length, a number of parallel fins dependence, fin width, etc. which can be plotted as a function of R_{th} as shown in Fig. 1.

The AC conductance mechanism is SHE measurement technique which uses drain to source conductance termed as g_{ds} at an accurate frequency and by integrating g_{ds} we can calculate the I_{ds}-V_{ds} [2]. Eq. (1-3) helps to extract the SHE effect on different device characteristics.

Another potential method to evaluate SHE in FETs is the four terminal gate resistance (R_g) technique [4]. In this technique the device temperature ΔT is evaluated by the temperature dependancy of the gate resistance. Figure 2 shows the gate resistance change as a function of chip temperature with different gate electrodes and

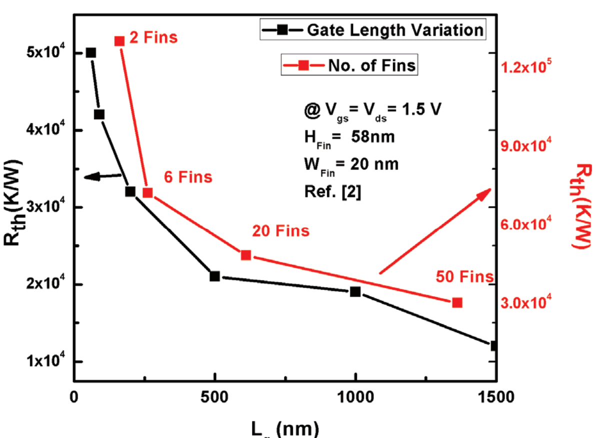

Fig. 1. R_{th} dependency on gate length variation and no. of fins [2].

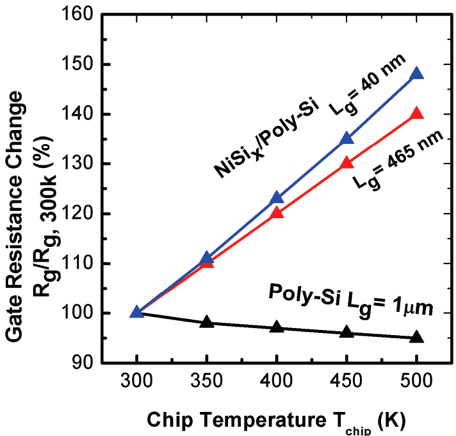

Fig. 2. Device temperature dependence as a function of gate resistance with different gate material configuration and gate length [4].

gate length plotted by using 4 point probe method with conventional I_d-V_d measurements.

Eq. (1) extracts the effective mobility degradation where μ_{eff} represents effective mobility at temperature T, μ_{effo} is the effective mobility at ambient temperature and T and T_o are the channel temperature and ambient temperature of the device. The degradation in mobility directly affects the drain current characteristics.

$$\mu_{eff} = \mu_{eff0}\left(\frac{T}{T_0}\right)^{-2} \tag{1}$$

$$\eta = \frac{I_{dsw/o} - I_{dsw}}{I_{dsw/o}} \times 100\% \tag{2}$$

$$R_{th} = \frac{I_{dsw/o} - I_{dsw}}{I_{ds} \cdot V_{ds} \cdot \frac{\delta I_{ds}}{\delta T}} \tag{3}$$

Eq. (2) gives the value of saturation output current with (I_{dsw}) and without ($I_{dsw/o}$) SHE impacts. Eq. (3) represents the thermal resistance value extraction where $\delta I_{ds}/\delta T$ is the saturation output current as a function of output temperature. The value of $\delta I_{ds}/\delta T$ can be obtained from the linear fitting of the hot chuck current measurement [2].

Further, the increase in temperature is determined by power and thermal resistance as shown in the following eq. (4).

$$\Delta T = R_{th} \times P = R_{th} \times (I_{ds} \cdot V_{ds}) \quad (4)$$

This thermal resistance is directly proportional to the rising temperature ΔT at constant power P and therefore, the R_{th} is considered as the standard asset for the measurement of SHE.

3. RESULTS AND DISCUSSIONS

3.1 R_{th} effect in bulk and SOI

In general, the multigate transistor with lower gate lengths suffer with the self-heating effect as it accumulates the heat at certain constant power when the thermal conductivity of SiO_2 is lower than that of Si and current densities are higher. SHE effects can be measured by using the R_{th} calculation which has a definite effect on the geometrical parameters of the devices. Table 1 shows the thermal conductivities of some materials which are actively in use for FinFETs [5].

H. Jiang et al. [2] studied the SHE effects in multi fins SOI FinFETs and investigated the effect of SHE with respect to number of fins, gate length scaling and reduction in width, where they have utilized AC conductance mechanism to study the SHE effects in SOI FinFETs, and shown that the thermal resistance is increased with the increase in number of fins and decrease with gate length. B. Gonzalez et al. [6] have compared the thermal effects in the SOI and Bulk FinFETs, where they found the mobility degradation due to SHE leads to further current enhancement. It is noticed that bulk FinFETs show a 7% higher current than that of the SOI FinFETs. Venkateswarlu et al. [7] simulated the multi-fin FinFET and optimized the device transfer characteristics for the 14 nm technology. The results show the strong influence of the thermal resistance and ambient temperature on device self-heating effects. The increase of R_{th} degrades the device on the current by 4.7% and also suggested that the thermal resistance can be reduced by increasing the source-drain contact areas. Further, the use of dielectric material and spacer having high thermal conductivity can help to reduce the overall ambient temperature and thermal resistance of the device by 23%.

Table 1. Thermal conductivities of some semiconducting materials [5].

Material	Thermal conductivity in $W.m^{-1}K^{-1}$ value
Si (Bulk)	148
Ge (Bulk)	16
$Si_{0.7}Ge_{0.3}$	8
SiO_2	14
Si (10 nm)	13

Another effective way has been reported by [8] to measure the channel local temperature induced due to SHE within 14 nm n and p type SOI FinFETs. In this work, the authors utilized lateral profiling technique, in which random telegraph noise (RTN) is generated to measure the local channel temperature with low level signal $|\tau_e|$. Figure 3 shows the plot of $Ln|\tau_e|$ as a function of Boltzmann constant K_BT. The linear slope of this graph is used to calculate the activation energy of the trapped carriers which causes actual heat in the channel and replicates that pFinFET exhibits more higher temperature at the drain side due to SHE than that of nFinFET. The SHE causes the 4% more degradation in drain current of pFinFET that of nFinFET.

The time resolved emission (TRE) measurements were employed to investigate the SHE in the SOI FinFETs [9]. The change in off state leakage current due to SHE was used as the main asset to investigate SHE. The

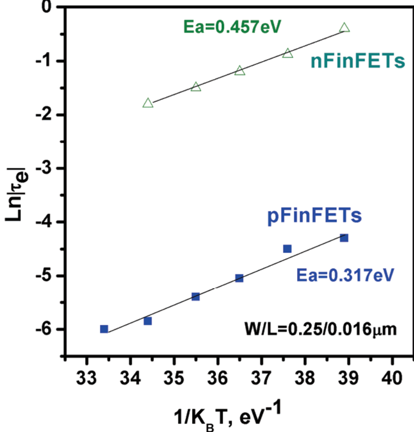

Fig. 3. A graph of $Ln|\tau_e|$ versus inverse of K_BT. The slope linear fit gives the value of activation energy of an electrons in RTN trap.

periodic voltage pulse were applied to gate to measure the respective drain current. At the end of this pulse, the FinFET device under test reaches to its peak temperature ΔT that strongly depends on the dissipated power and the pulse time (t). Figure 4 shows the calibration curve for different device temperature measurement as a function of drain current.

The I_{ds} value reported so far for Bulk and SOI FinFETs are ~9×10^{-5} A [5] (@ V_{gs}=1V) and 2.31×10^{-3} A [10] (@ V_{gs}=1.1 V), respectively which is high in the case of SOI FinFETs. Figure 5 shows the thermal resistance values reported so far for bulk and SOI FinFETs [1,2,5].

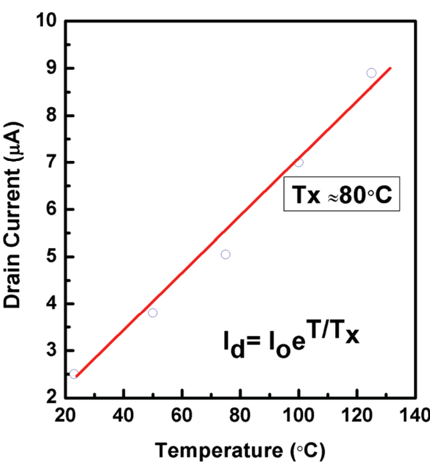

Fig. 4. Drain current as the function of device temperature T, where Tx is the characteristic constant.

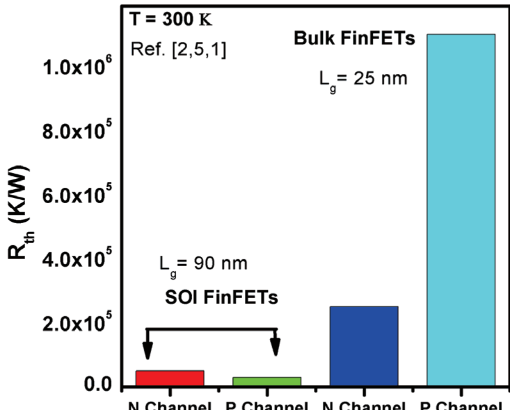

Fig. 5. R_{th} comparison for bulk and SOI FinFETs.

3.2 Integration of graphene Ccn reduce SHE in the FinFETs?

The lower thermal conductivity of the buried oxide is somewhere the main reason for the self heating of the device. Further, the central fins accumulate 50% more heat as compare to the lateral fins reported earlier [11]. The use of higher thermal conductivity material can be employed to reduce the SHE in nanoscale FinFETs. Use of 2D materials opened the doors for the new device structures to drive future electronics industry. The graphene is the 2-dimensional material having very high mobility and also the thermal conductivity (~1,800 W $m^{-1}K^{-1}$ at 325 k) in comparison with Si [12]. In this context, the FinFET with single fin, where graphene is used as the gate electrode has been patented by global foundries Inc. 2014 [13]. Further, it is also reported that, the thermal conductivity of the 2D material like graphene is independent of the thickness [14]. Pan et al. [15] has studied the SHE in the graphene transistors with different dielectric layers wherein, the high thermal conductive AlN with graphene can be used to suppress the thermal effects in the future devices. The A. Moore [16] has given very nice review on the thermal management of futuristic devices, wherein, the use of higher thermal conductive material like 2D h-BN having similar properties to diamond with Al_2O_3 gate dielectric can help to alleviate the local hot spots and improve the device performance and reliability. Figure 6 shows an example of the 2D material based device.

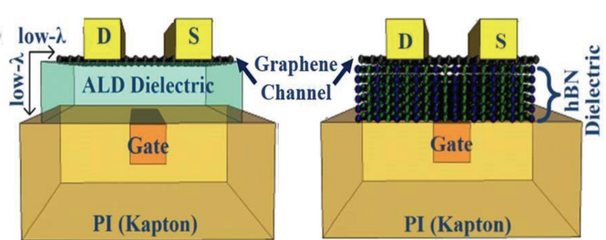

Fig. 6. Cross sectional view of flexible FET with graphene, h-BN as a channel and Al_2O_3 as gate dielectric. Reproduced with permission from elsevier reference [16].

4. CONCLUSION

Complex geometry and lack of heat release path between channel and substrate lead to self-heating effect which ultimately degrades the device performance. There are different mechanisms to study these effects. The respective potential of each technique with there assets like R_{th}, ΔT, I_d to study the SHE has been discussed. The R_{th} value appear differently for the bulk and SOI FinFETs. The one of reason behind this self heating of device is the lower thermal conductivity of the SiO_2. Therefore, the higher thermal conductive material like graphene as a channel and high thermal conductive dielectric can be employed to suppress these SHE. The study reviewed in this article may useful for the futuristic nanoscale FinFETs beyond 14 nm.

ORCID

Eun-Chel Cho https://orcid.org/0000-0002-4808-9388
Junsin Yi https://orcid.org/0000-0002-6196-0035

ACKNOWLEDGEMENT

The authors acknowledge with thanks to Samsung Electronics Co. LTD., Korea, for their support and suggestions.

REFERENCES

[1] S. W. Yoo, H. Kim, M. Kang, and H. Shin, *J. Semicond. Technol. Sci.*, **16**, 204 (2016). [DOI: https://doi.org/10.5573/JSTS.2016.16.2.204]

[2] H. Jiang, N. Xu, B. Chen, L. Zeng, Y. He, G. Du, X. Liu, and X. Zhan, *Semicond. Sci. Technol.*, **29**, 115021 (2014). [DOI: https://doi.org/10.1088/0268-1242/29/11/115021]

[3] E. Bury, B. Kaczer, P. Roussel, R. Ritzenthaler, K. Raleva, D. Vasileska, and G. Groeseneken, *Proc. 2014 IEEE International Reliability Physics Symposium* (IEEE, Waikoloa, USA, 2014) p. 14. [DOI: https://doi.org/10.1109/IRPS.2014.6861186]

[4] T. Takashi, T. Matsuki, T. Shinada, Y. Inoue, and K. Uchida, *IEEE J. Electron Devices Soc.*, **4**, 365 (2016). [DOI: https://doi.org/10.1109/JEDS.2016.2568261]

[5] M. I. Khan, A. R. Buzdar, and F. Lin, *Proc. 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)* (IEEE, Guilin, China, 2014) p. 7021443. [DOI: https://doi.org/10.1109/ICSICT.2014.7021443]

[6] B. González, J. B. Roldán, B. Iñiguez, A. Lázaro, and A. Cerdeira, *Microelectron. J.*, **46**, 320 (2015). [DOI: https://doi.org/10.1016/j.mejo.2015.02.003]

[7] S. Venkateswarlu, A. Sudarsanan, S. G. Singh, and K. Nayak, *IEEE Trans. Electron Devices*, **65**, 2721 [DOI: https://doi.org/10.1109/TED.2018.2834979]

[8] E. R. Hsieh, M. R Jiang, J. L. Lin, S. S. Chung, T. P. Chen, S. A. Huang, T. J. Chen, and O. Cheng, *IEEE J. Electron Devices Soc.*, **6**, 866 (2018). [DOI: https://doi.org/10.1109/JEDS.2018.2859276]

[9] F. Stellari, K. A. Jenkins, A. J. Weger, B. Linder, and P. Song, *Proc. 2015 IEEE International Reliability Physics Symposium* (IEEE, Monterey, USA 2015). [DOI: https://doi.org/10.1109/IRPS.2015.7112672]

[10] I. Hossain, A. Anwar, M. Z. Baten, and Q.D.M. Khosru, *Proc. International Conference on Electrical & Computer Engineering (ICECE 2010)* (IEEE, Dhaka, Bangladesh, 2010) p. 400. [DOI: https://doi.org/10.1109/icelce.2010.5700713]

[11] K. Derbyshire, *Will Self-Heating Stop FinFETs*, https://semiengineering.com/will-self-heating-stop-finfets/ (2017).

[12] J. U. Lee, D. Yoon, H. Kim, S. W. Lee, and H. Cheong, *Phys. Rev. B*, **83**, 081419 (2011). [DOI: https://doi.org/10.1103/PhysRevB.83.081419]

[13] US Patent: Z. Krivokapic and B. Sahu, FinFET Device with a Graphene Gate Electrode and Method of Forming Same, 2014/OO15O15 A1, (2014).

[14] X. Wu, V. Varshney, J. Lee, Y. Pang, A. K. Roy, and T. Luo, *Chem. Phys. Lett.*, **669**, 233 (2017). [DOI: https://doi.org/10.1016/j.cplett.2016.12.054]

[15] T. S. Pan, M. Gao, Z. L. Huang, Y. Zhang, X. Feng, and Y. Lin, *Nanoscale*, **7**, 13561 (2015). [DOI: https://doi.org/10.1039/c5nr02750k]

[16] A. L. Moore and L. Shi, *Mater. Today*, **17**, 163 (2014). [DOI: https://doi.org/10.1016/j.mattod.2014.04.003]