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A New Multi Level High Gain Boost DC-DC Converter with Wide Input Voltage Range and Reduced Stress Voltage Capability

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Abstract

The use of high-gain-voltage step-up converters for distributed power generation systems is being popularized because of the need for new energy generation and power conversion technologies. In this study, a new constructed high-gain-boost DC - DC converter was proposed to coordinate low voltage output DC sources, such as PV or fuel cell systems, with high DC bus (380 V) lines. Compared with traditional boost DC - DC converters, the proposed converter can create higher gain and has wider input voltage range and lower voltage stress for power semiconductors and passive elements. Moreover, the proposed topology produces multilevel DC voltage output, which is the main advantage of the proposed topology. Steady-state analysis in continuous conduction mode of the proposed converter is discussed in detail. The practicability of the proposed DC - DC converter is presented by experimental results with a 300 W prototype converter.

Key words: High gain boost DC-DC converter, High efficiency, Multilevel DC-DC converter, Switched capacitor, Reduced stress voltage

1. Introduction

Recently, with the development of green energy producing technology, the use of renewable sources such that PV arrays, fuel cells, etc. have been increasing rapidly. Since the output voltage level of the renewable sources is very low, two stage power conversion is required to generate high DC bus (380V) shown in Fig. 1. In the first stage low level DC voltage is increased to a high level DC voltage (380V) by power converter with a high gain conversion and high efficiency. In the second stage high DC voltage can be used for DC or AC voltage application.

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The traditional boost converters have not high gain capability to make high DC voltage as they require high duty cycle, which resulted in high power loss and reduced life cycle. To get a high gain and high efficient power converter, there are developed many converters, such that isolated, non-isolated and also floated output step-up converters[1]-[4]. The isolated circuits have some disadvantages, that they require a large number of components to make high DC voltage in two stage. And also the isolated boost converters demand briefly parameters design which will be difficult. Non-isolated converters step up low voltage in many techniques, such that switched-inductor (SL) based, switched-capacitor (SC) and mixed types[5]-[7]. The topologies certainly have high gain capability, but on the other hand have some disadvantages, such that large number of components, high voltage stress, high input current ripple and complexity of the circuit. Such disadvantages lead to high cost and decreases device life cycle.

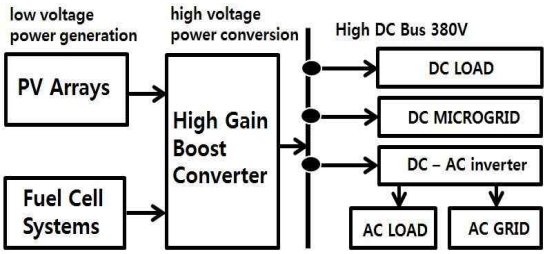

Fig. 1. Block diagram of a typical power generation system.

In order to obtain high gain, high efficient and low voltage stress topologies, Voltage Multiplier, Voltage lift, Multilevel output and X-shaped Z-source network converters were developed[8]-[12]. Such converters has high gain, high flexibility and $\frac{1}{2}V_{out}$ stress voltage. However, some components suffer from V_{out} equal voltage and high current stress. And also the duty value of such converters approaches to unity which will lead to high power losses. Because of such disadvantages there is a need to create some boost converter which can obtain high gain capability with lowered number of active and passive elements and decreased duty cycle.

The goal of this paper is to create high gain, high efficient, long life cycle and wide input voltage range boost dc-dc converter by

① decreasing all components voltage stress from V_{out} to $\frac{1}{3}V_{out}$ value;

② decreasing duty D cycle;

③ creating multilevel output DC voltage.

This paper will be described in the following sequence. Section 2 presents the proposed converter topology, operating principles and some analysis. Simulation results are in Section 3. Comparisons to other boost converters is discussed in Section 4. Active and passive components selection will be described in Section 5. In Section 6 experimental results will be described. Finally, in Section 7 a few conclusions will be described.

2. The Proposed Converter Topology and Some Operating Analysis

2.1 Circuit of the proposed converter

The proposed converter topology is made by two MOSFETs S_1 and S_2, inductor L, capacitors C_{UP}, C_{o1}, C_{o2}, C_1, C_2, diodes D_1, D_2, D_3 and D_{out} as pictured in Fig. 2. The output capacitors C_{o1} and C_{o2} are connected

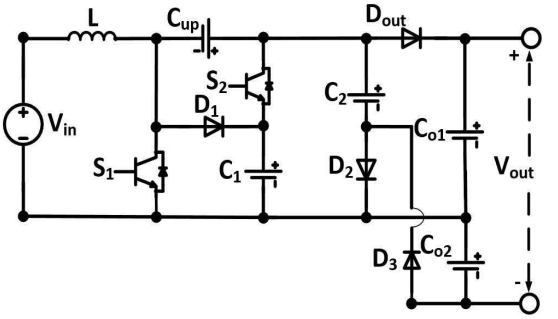

Fig. 2. Proposed high gain multi level boost converter.

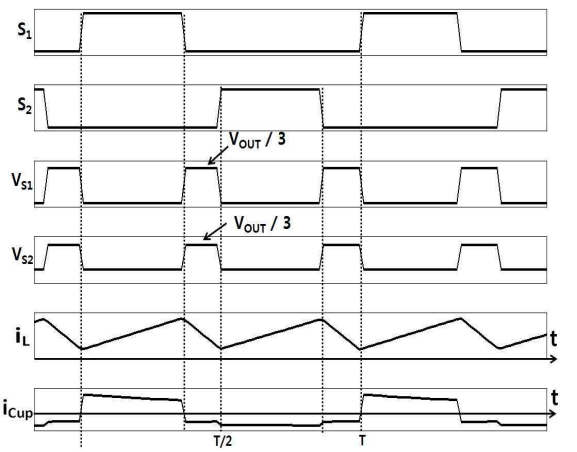

Fig. 3. Main waveforms of the proposed converter for CCM operation.

in series. C_{o1} capacitor have common ground with the input DC source, but C_{o2} capacitor has different ground. This connection let to create multilevel output capability and thus decreases voltage stress for active and passive components. Capacitor C_{UP} is connected in switched-capacitor technique. The main waveforms of the proposed topology are presented in Fig. 3. As shown in the Fig. 3. S_1 and S_2switches drain-source voltages V_{S1} and V_{S2} are equal to third value of output DC voltage, the inductor current is twice charged and discharged during one switching period. And there is no inrush current in C_{UP} capacitor.

In order to explain the steady state operation of the proposed converter, some assumptions are made as below :

① The effects of ON state resistance ($R_{DS(ON)}$) of the switches, forward voltage drop (V_f) of the diodes and equivalent series resistance (ESR) of the inductor and electrolitic capacitors are neglected ;

② The summarized capacitance of the two output capacitor are enough to maintain constant output DC voltage.

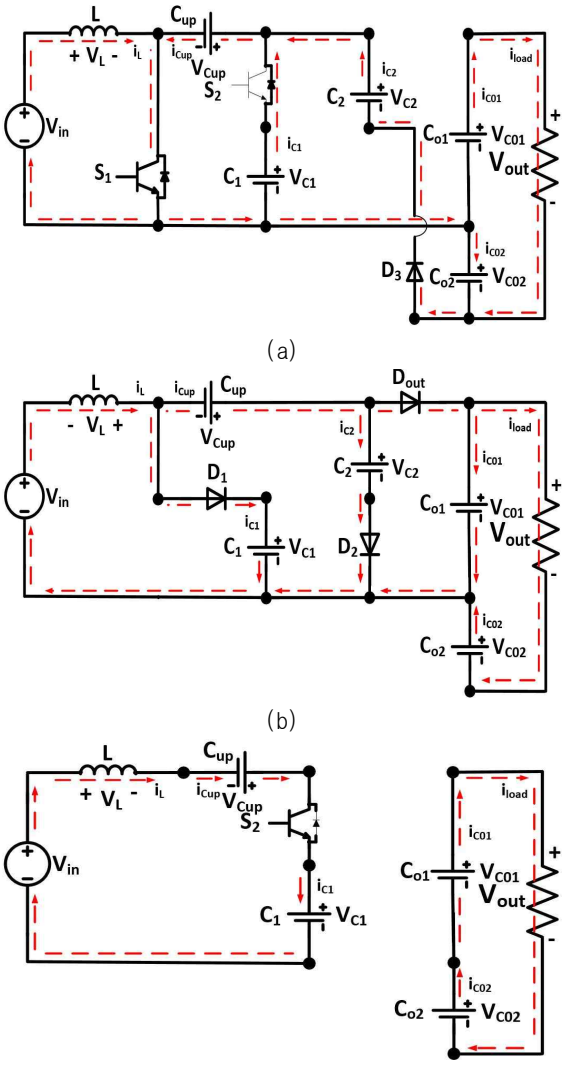

Fig. 4. Energy flowing schemes of switching states: (a) "S1S2" = [10], (b) "S1S2" = [00], (c) "S1S2" = [01].

③ It is possible to get high step-up gain capability, even output power of the load is extremely high.

2.2. Operating principle of the proposed converter

In this part operating principle of the proposed converter in continuous conduction mode (CCM) is discussed. Two switches (S_1 and S_2) are operated in the same duty value, but their gate driving signals has 180^0 phase difference. There are three different switching states "S_1S_2" = [10, 00, 01], where "0" means switch have OFF state and "1" means ON state for two switches with the same duty value. Switching sequence is "10 - 00 - 01 - 00 - 10". As seen from the Fig. 3, S_1 and S_2 are operating only when $D<0.5$. It means that the duty cycle of the proposed converter is limited in $[0<D<0.5]$ interval. Energy flowing paths of each switching states of the proposed topology are shown in Fig. 4 and also in Fig. 5, Fig. 6, Fig. 7 simulation results are shown.

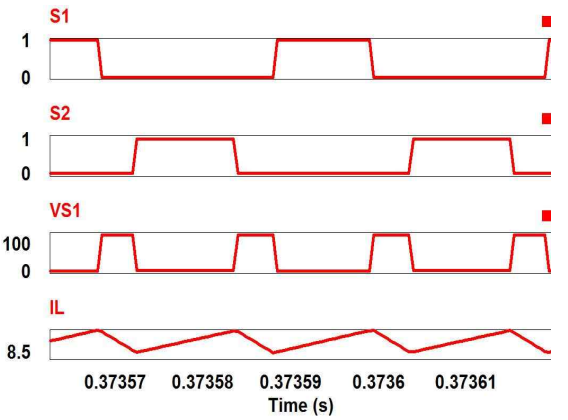

Fig. 5. Simulation results of the proposed converter. From top to bottom: gate signals for the S_1 and S_2 switches, drain-source voltage- V_{S1} of the S_1 switch and i_L- inductor current.

In switching state "S_1S_2" = [10] S_1 is in ON state and oppositely S_2 is in OFF state. In this switching state which can be seen in Fig. 4(a) inductor L is charged with linearly rising i_L current from input DC source and capacitor C_{UP} is charged by C_1 and C_2 capacitor. And also C_2 and C_{o1} capacitors are discharged. The load is supplied by summarizing C_{o1}, C_2 and C_{up} capacitors voltages. Therefore, in this switching state the following equations are made:

$$V_L = V_{dcsource} = L^* \frac{dI_L}{dT} \tag{1}$$

$$V_{C_2} = V_{C_{UP}} + V_{C_{02}} \tag{2}$$

$$V_{LOAD} = V_{C_{01}} + V_{C_2} - V_{C_{UP}} \tag{3}$$

$$i_{LOAD} = i_{C_{o1}} + i_{C_2} - i_{C_{up}} \tag{4}$$

where

$V_{C_{UP}}$ is C_{UP} capacitor voltage;

i_L is inductor current;

$V_{dcsource}$ is input DC source voltage;

V_{C_1} is C_1 capacitor voltage;

V_{C_2} is C_2 capacitor voltage;

$V_{C_{01}}$ is C_{o1} capacitor voltage;

$V_{C_{02}}$ is C_{o2} capacitor voltage;

V_{LOAD} is the load voltage.

In the next "S_1S_2" = 00 switching state both of the switches are in OFF state, which energy flowing

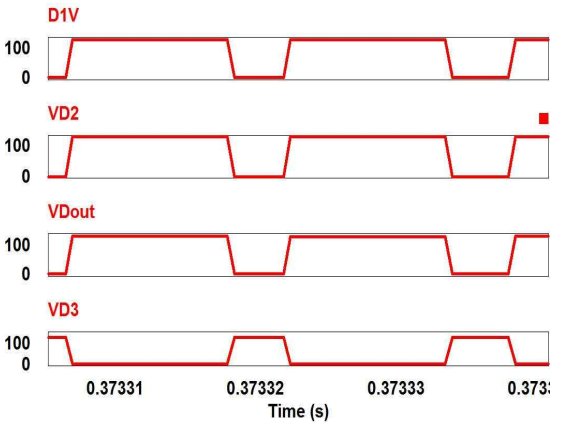

Fig. 6. Simulation results of the proposed converter. From top to bottom: D_1, D_2, D_{out} and D_3 diodes stress voltages.

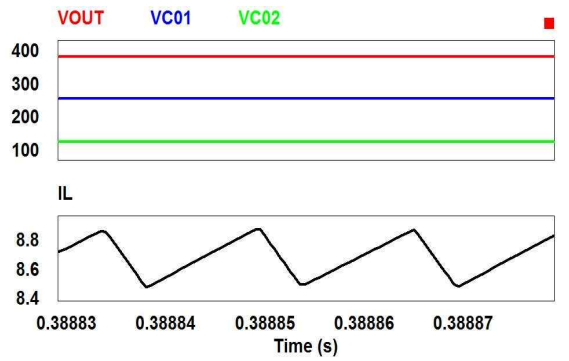

Fig. 7. Simulation results of the proposed converter. From top to bottom: output DC voltage- V_{OUT}(red), C_{o1}capacitor voltage- V_{Co1}(blue), C_{o2}capacitor voltage- V_{Co2}(green) and inductor current - i_L(black).

path is pictured in Fig. 4(b). C_{UP} and C_{o2} capacitors are discharged, the other C_1 , C_2 and C_{o1} capacitors are charged. Diode D_3 is turned off. The current of the inductor I_L is linearly decreased. In this switching state the load voltage is formed by summarizing input DC source, inductor, C_{UP} and C_{02} capacitors voltages. The following equations are made in "S_1S_2" = 00 switching state :

$$V_{C_1} = V_{dcsource} - V_L \tag{5}$$

$$V_{C_2} = V_{dcsource} - V_L - V_{C_{UP}} \tag{6}$$

$$i_L = i_{C_1} + i_{C_2} + i_{C_{o1}} + i_{LOAD} \tag{7}$$

$$V_{LOAD} = V_{dcsource} - V_L - V_{C_{up}} - V_{C_{o2}} \tag{8}$$

In next "S_1S_2" = 01 switching state S_1 is in OFF state and S_2 is in ON state as shown in Fig. 4(c). D_{out} diode is turned off and the load is supplied in accordance to the next equation :

$$i_{LOAD} = i_{C_{o1}} + i_{C_{o2}} \tag{9}$$

$$V_{LOAD} = V_{C_{o1}} + V_{C_{o2}} \tag{10}$$

In this switching state the load voltage is formed by summarizing C_{o1} and C_{02} capacitors voltages, the inductor is charged by input DC source. i_L inductor current is linearly increased.

2.3 Operating analysis of the proposed converter

2.3.1 Voltage gain and duty cycle

From the above made equations (1-10) and applying volt-second balance of inductor during steady-state operation, the proposed converter main equations can be expressed as

$$V_{out} = \frac{3 * V_{dcsource}}{(1-2*D)} \tag{11}$$

$$G = \frac{3}{(1-2*D)} \tag{12}$$

$$i_L = \frac{3}{(1-2*D)} * i_{load} \tag{13}$$

$$\triangle I_L = \frac{(1-2*D)* V_{dcsource}}{L * f_{sw}} \tag{14}$$

where V_{out} is out DC voltage, G is voltage gain, i_L is average inductor current, $\triangle I_L$ is inductor current ripple and $V_{dcsource}$ is input DC source voltage of the proposed converter.

(12) equation shows that D duty value of the proposed converter should be within $[0 < D < 0.5]$ interval. In traditional step-up converters, when high gain is required, the duty cycle should be in $[0 < D < 1.0]$ interval. Using large duty cycles lead to high conduction and high switching losses. So, the proposed topology can earn high gain with a small duty cycle which can decrease conduction losses on the power semiconductors.

2.3.2 Voltage stress of the semiconductors

From (12), (13) and (14) equation, the maximum voltage stress of the semiconductors can be written as

$$V_{S1\max} = V_{C_1} = \frac{1}{3} * V_{out} \tag{15}$$

$$V_{S2\max} = V_{out} - V_{C_1} - V_{C_{o2}} = \frac{1}{3} * V_{out} \tag{16}$$

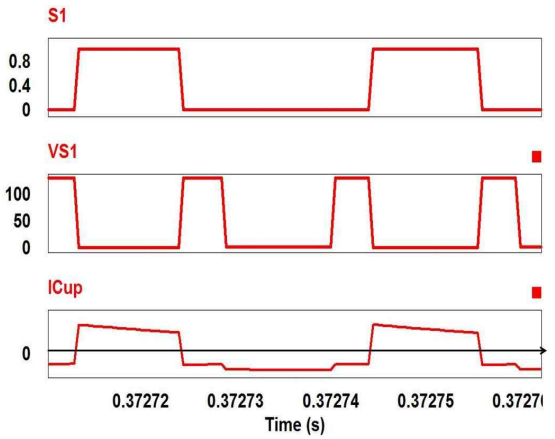

Fig. 8. Simulation results of the proposed converter. From top to bottom: S_1 switch gate signal, S_1 switch drain-source voltage- V_{S1}, $i_{C_{UP}}$-capacitor C_{UP} current.

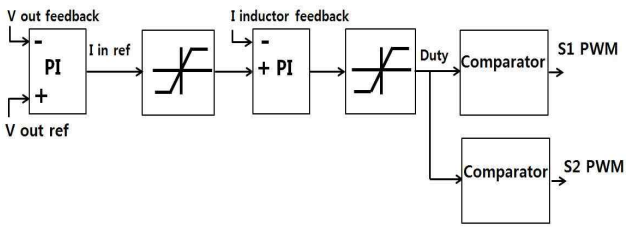

Fig. 9. Output DC voltage control scheme of the proposed topology.

$$V_{diode} = V_{S2\max} = \frac{1}{3} V_{out} \tag{17}$$

where $V_{S1\max}$, $V_{S2\max}$, are S_1 and S_2 switches maximum voltages and V_{diode} is diodes maximum voltages. Simulation waveforms of the diodes stress voltage are pictured in Fig. 6. It can be concluded that voltage stress all of the semiconductors is equal to third of the output voltage.

2.3.3 Output voltage control

As shown in Fig. 9, a double PI regulator is used to maintain output DC voltage in the reference voltage value range and to control input current. Duty value is being compared with the triangle waveform and thus PWM signals are made. Note that S_2 switch PWM signal is made by phase shifting the triangle carrier waveform.

3. Simulation Results

To confirm the operating validity of the proposed topology, PWIM simulation was performed. The proposed boost dc-dc converter with 300W output is designed and simulated by PSIM9.1 software tool. The simulation and experimental specifications of the proposed topology are described in Table II and Table III.

As shown from the Fig. 5, S_1 switch V_{S1} drain-source voltage maximum value is equal to the third value of the output DC voltage. Inductor charged and discharged twice during one switching period. In the next Fig. 7 it is seen that V_{out} output DC voltage is formed by summing C_{o1} and C_{02} capacitor voltages.

4. Comparison with Other High Gain Converters

4.1 Voltage gain

In nowadays there are many boost converters with high voltage gain, high efficiency, decreased duty cycle and decreased number of components. In order to compare the proposed topology with other step-up converters Table I is presented. As shown from the Table I, the proposed topology has higher voltage gain. And also the proposed topology requires the lowest duty cycle for the same voltage gain than converters in [5]-[11].

4.2 Active and passive components voltage stress and inductor current ripple

The voltage stresses of all power semiconductors in [5], [6], [10], [11] converters are between $\frac{1}{2} V_{out}$ and $\frac{2}{3} V_{out}$. Converter in [7] has $\frac{1}{3} V_{out}$ equal voltage stress, but it includes large number of components and operates in large duty cycle $0 < D < 1.0$ as well as the other converters. In the proposed converter C_{o1} capacitor has $\frac{2}{3} V_{out}$ equal voltage stress, but the other passive and active components have $\frac{1}{3} V_{out}$ equal voltage stress. Moreover, inductor current frequency of the proposed converter is double the switching frequency which can reduce the input current ripple.

4.3 The number of active and passive components

Compares to converters in [7] and [10], the proposed topology uses less number of the components. Compares to converters in [7] and [10], the proposed topology uses less number of the components. Converter in [5] uses one less active

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS

Converters	Active elements (switch, diodes)	Passive elements (Cap, inductor)	Experimented power, W	Voltage gain	Voltage stress for switches
in [5]	5	7	40	$\frac{2}{1-D}$	$\frac{1}{2}*V_{out}$
in [6]	5	5	130	$\frac{D^2-3D+3}{(1-D)^2}$	$\frac{2}{3}*V_{out}$
in [7]	8	6	1000	$\frac{3}{1-D}$	$\frac{1}{3}*V_{out}$
in [10]	8	8	200	$\frac{4}{1-D}$	$V_{out}-V_{dcsource}$
in [11]	5	3	100	$\frac{1+D_1}{1-D_1-D_2}$	$\frac{1}{2}*V_{out}$
proposed	6	6	300	$\frac{3}{1-2*D}$	$\frac{1}{3}*V_{out}$

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE PROPOSED CONVERTER

Parameter	Values
Input Voltage	36-72 V
Output Voltage	382 V
Power	300 W
Switching frequency	20 Khz
Efficiency	90 - 95 %

TABLE III
ACTIVE AND PASSIVE ELEMENTS SPECIFICATION OF THE PROPOSED CONVERTER

Devices	Model	Specifications
MOSFET (S1, S2)	IRFP4668PBF	200V/130A
Diodes	DPG10I200PA/ IXYS	200V/10A
Capacitor	B43630F2827M000/TDK	820uF/250VDC
Capacitor	SAMYOUNG	470uF/250VDC
Inductor	TDK	720uH

component, but it has one more passive component and experimented power is very low. Converter in [6] has one less active and one less passive component, but the duty cycle of the converter is very large. Converter in [11] has the decreased components, but as converter in [6] has high duty cycle. Therefore, the size and the weight of the proposed converter are lower than the other topologies.

5. Active and Passive Components Selection

5.1 Switches selection

Due to the proposed converter has decreased voltage stress for switches, all of the semiconductors are selected with maximum 200V breaking voltage capability. $R_{DS(ON)}$ for Power MOSFET is selected lower than 10mOhm in order to decrease switching and conduction losses.

5.2 Passive components selection

The inductance of the proposed converter is selected by considering the input current ripple as 1 A and according to (18)

$$L=\frac{(1-2*D)*V_{dcsource}}{\triangle I_L*f_{sw}} \tag{18}$$

So. the minimum inductance value should be 600 μH. The capacitance should be selected as

$$C_{\min}=\frac{(1-2*D)*P_{out}}{\triangle V_{out}*V_{out}*f_{sw}} \tag{19}$$

Setting $\triangle V_o$ out DC voltage ripple to 50mV and out DC voltage to 382 V, the minimum capacitance is calculated as $C_{\min}=256\mu F$. In this case to avoid a large out voltage ripple when the load power suddenly changes, the out capacitance is selected as $C_{out}=820\mu F$ per capacitor.

6. Experimental Results and Analyses

To verify output performance of the proposed converter, 300 W experiment prototype of the proposed converter was built as pictured in Fig. 10 and experiments were carried out. Two power switches IRFP4668PbF and four diode DPG10I200PA

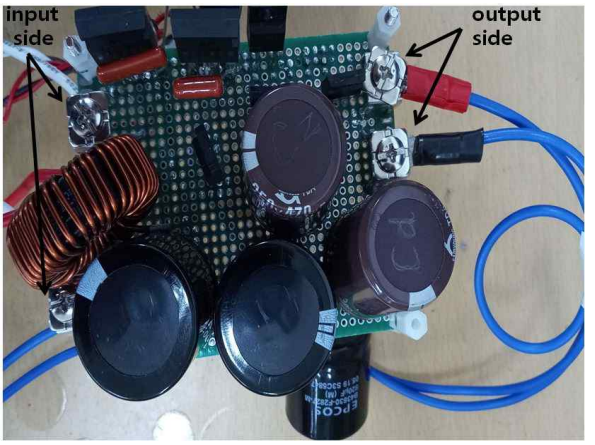

Fig. 10. Hardware prototype of the proposed converter.

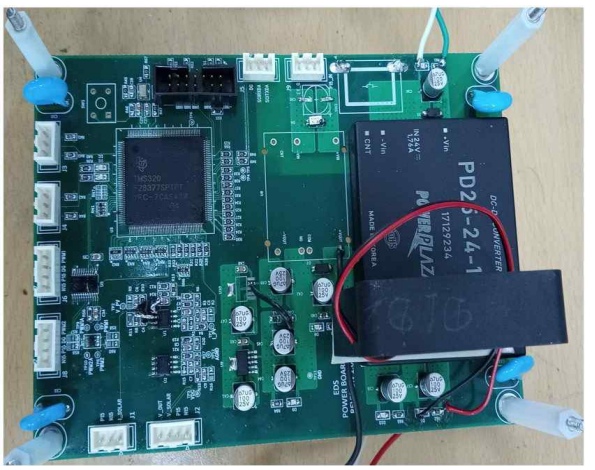

Fig. 11. Control system of the proposed converter based on TMS320F28377S.

were used. The proposed converter is fed by KEYSIGHT N8762A power supply. Closed-loop control method as described in Fig. 9 is implemented by using DSP TMS320F28377S as pictured in Fig. 11. Resistor is used as the load. Experiment results are demonstrated in Fig. 12 - Fig. 16. Experiment and components parameters are shown in Table II and Table III. Applying the double closed-loop control method, the proposed topology normally operates under input DC voltage from 36 V to 72 V, out DC voltage $V_{out} = 382\,V$ and out power $P_{out} = 300\,W$. Operating experiment waveform of the inductor L is the same as the simulation waveform: its charging and discharging frequency is double the switching frequency which is seen in Fig. 13. and Fig. 15.

When the proposed converter operates at the rated $P_{out} = 300\,W$ power, its voltage stress of the power semiconductors are the third of V_{out} value which are seen from the Fig. 13, Fig. 14, Fig. 15.

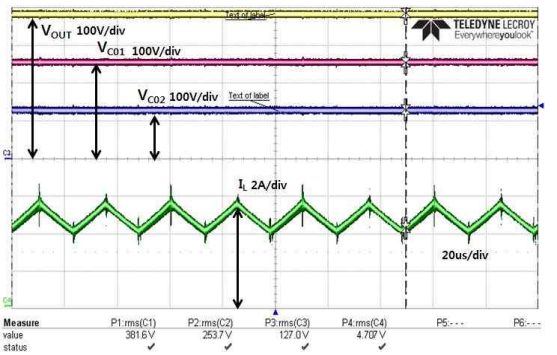

Fig. 12. Experiment results of the proposed topology. From top to bottom: output DC voltage - V_{OUT} (yellow), C_{o1} capacitor voltage - V_{Co1} (red), C_{o2}capacitor voltage - V_{Co2} (blue) and inductor current - i_L (green).

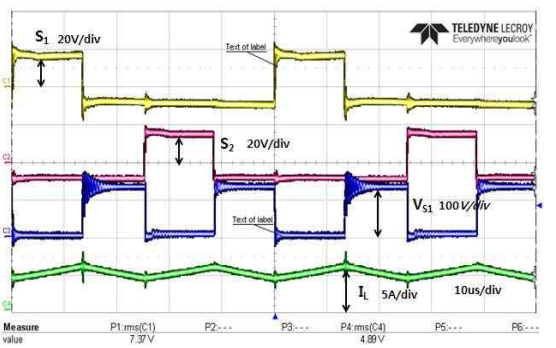

Fig. 13 Experiment results of the proposed topology. From top to bottom: gate signals for the S_1 (yellow) and S_2 (red) switches, drain-source voltage V_{S1} (blue) of the S_1 switch and i_L-inductor current (green).

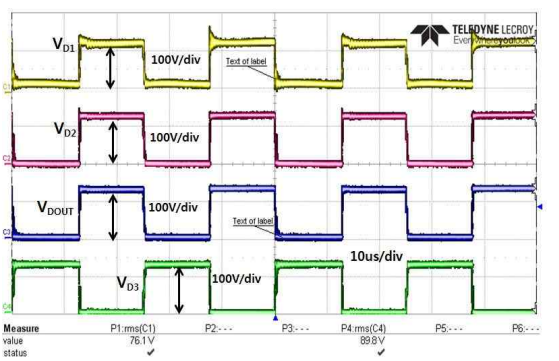

Fig. 14. Experiment results of the proposed topology. From top to bottom: $V_{D1}, V_{D2}, V_{Dout}, V_{D3}$ - D_1 (yellow), D_2 (red), D_{out} (blue) and D_3 (green) diodes stress voltages.

Fig. 12 shows V_{out}, C_{o1}, C_{o1} capacitors voltage waveforms where V_{out} = 382V, C_{01} capacitor holds $\frac{2}{3}V_{out}$ equal and C_{02} capacitor holds $\frac{1}{3}V_{out}$ equal voltage value, which confirm that the proposed topology has multi level ouput capability. Some differences between the simulation results and the experimental

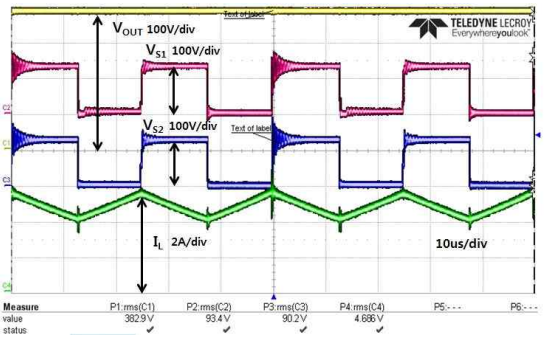

Fig. 15. Experiment results of the proposed topology. From top to bottom: output DC voltage – V_{OUT} (yellow), drain-source voltage– V_{S1} (red) of the S_1 switch, drain-source voltage– V_{S2} (blue) of the S_2 switch and i_L – inductor current (green).

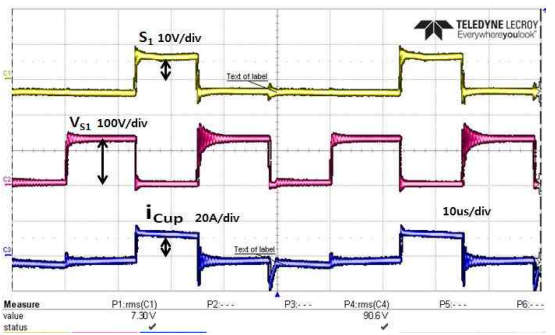

Fig. 16. Experiment results of the proposed topology. From top to bottom: S_1 switch gate-source voltage (yellow), S_1 switch drain-source voltage– V_{S1} (red) and C_{UP} capacitor current–$i_{C_{UP}}$ (blue).

waveforms are resulted due to the existence of ESR of the passive components and $R_{DS(ON)}$ of the MOSFETs.

The output voltage stays invariable in reference voltage value of 382 V when input voltage changes from 36 V to 72 V. It means that the proposed topology can achieve voltage gain from 5.3 to 10.6. Relatively to changes in input voltage, the duty cycle of the proposed converter changes from 0.23 to 0.372 which avoid extreme duty cycle changes. Waveform of diodes voltages is presented in Fig. 14. As it is seen the maximum value of the voltage does not extend the $\frac{1}{3}V_{out}$= 127.3V value. The C_{UP} capacitor current waveform is shown in the Fig. 16. As shown from the waveform the C_{UP} capacitor charges when S_1 switch is in ON state and discharges when S_1 switch is in OFF state. The most important fact that the C_{UP} capacitor has no inrush current.

Experiments also were conducted to measure efficiency of the proposed converter at different input

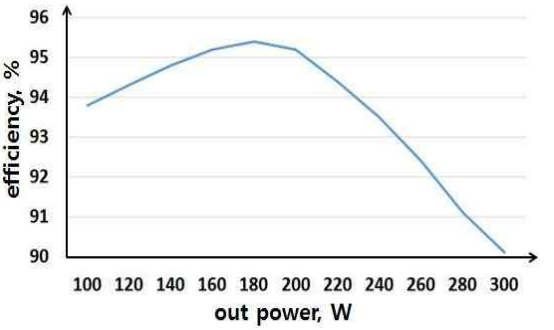

Fig. 17. Efficiency–out power curve when $V_{dcsource}$ = 36V.

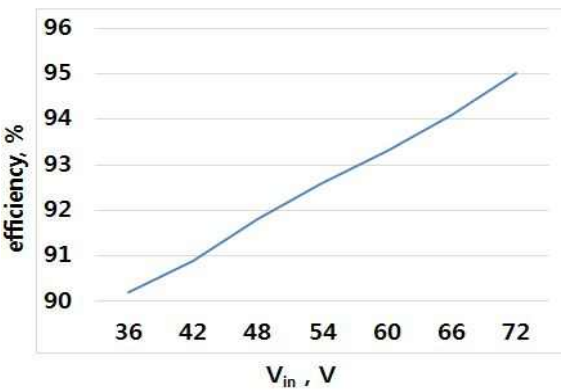

Fig. 18. Efficiency – input voltage curve when P_{OUT} = 300W.

voltages and at different output power. Efficiency – out power curve waveform is presented in Fig. 17. Differences between the simulation and the experimental efficiency is around 1%. The maximum efficiency is 95.1% when input voltage is 72V and the rated power is 300W. The minimum efficiency is 90% at 36V input and at 300W out power. Efficiency decreasing reason is due to the increasing power losses caused by the input current. From the Fig. 18 it is seen that by decreasing input voltage the efficiency value is also decreased.

7. Conclusions

In this paper a new multi level high gain boost DC-DC converter with wide input voltage range and reduced stress voltage capability is proposed. The main advantages of the proposed topology are as follows: $\frac{1}{3}V_{out}$ equal voltage stress, multi level voltage output capability and low conduction losses on the semiconductors. And also small duty cycle in $[0 < D < 0.5]$ interval can be used for achieving high voltage gain when the input voltage varies between 36V to 72V. Furthermore, the inductor of the proposed

converter is charged and discharged twice during one switching period. As a result, input current ripple is decreased. A lot of experimental results proved that the proposed converter could be used as high gain DC-DC power conversion system to coordinate low voltage PV or fuel cell stacks with high 380V DC buses.

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