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- 오류정정 -

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	8. R. Darveaux, K. Banerji, A. Mawer, and E. Mammo, “Reliability of Plastic Ball Grid Array Assembly”, Ball Grid Array Technology, McGraw-Hill, New York (1995).

요청사항	9. J. H. Lau, J. L. Prince, W. Nakayama, and C. P. Wong, “Electronic Packaging: Design, Materials, Process, and Reliability”, McGraw-Hill, New York (1997). 10. E. Lin, D. Chang, D. S. Jiang, Y. P. Wang, and C. S. Hsiao, “Advantage and challenge of coreless Flip chip BGA Microsystems”, International Microsystems, Packaging, Assembly and Circuits Technology (IMPACT), Taipei, Taiwan, 346, IEEE (2007). 11. C. Chiu, K. C. Chang, J. Wang, and C. H. Lee, “Challenges of thin core PCB Flip Chip package on advanced Si Nodes”, Proc. 57th Electronic Components and Technology Conference (ECTC), 22 (2007). 12. S. H. Cho, T. E. Chang, J. Lee, and H. P. Park, “New dummy design and stiffener on warpage reduction in Ball Grid Array Printed Circuit Board”, Microelectronics Reliab., 50, 242 (2010). 13. J. H. Lau, and S.-W.R, Lee, “Effects of Build-Up Printed Circuit Board Thickness in the Solder Joint Reliability of a Wafer Level Chip Scale Package(WLCSP)”, Trans. Comp. Packag. Technol., 25(1), 3 (2002). 14. W. Sun, W. H. Zhu, C. K. Wang, A. Y. S. Sun, and H. B. Tan, “Warpage Simulation and DOE Analysis with Application in Package-on-Package Development”, Proc. 9th EuroSimE 2008 - International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems (ESIME), Freiburg im Breisgau, Germany, 244, IEEE (2008). 15. Y. L. Tzeng, N. Kao, E. Chen, J. Y. Lai, Y. P. Wang, and C. S. Hsiao, “Warpage and Stress Characteristic Analyses on Package-on-Package (PoP) Structure”, Proc. 9th Electronics Packaging Technology Conference (EPTC), Singapore, 482, IEEE (2007). 16. W. Sun, W. H. Zhu, K. S. Le, and H. B. Tan, “Simulation Study on the Warpage Behavior and Board-level Temperature Cycling Reliability of PoP Potentially for High-speed Memory Packaging”, International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), Shanghai, 978, IEEE (2008). 17. S. H. Cho, H. I. Jung, and O. C. Bae, “Numerical Analysis on the Design Variables and Thickness Deviation Effects on Warpage of Substrate for FCCSP”, J. Microelectron. Packag. Soc., 19(3), 57 (2012). 18. S. H. Cho, D. H. Kim, Y. G. Oh, J. T. Lee, and S. S. Cha“A Study on the Parameters of Design for Warpage reduction of Passive components Embedded Substrate for PoP”, J. Microelectron. Packag. Soc., 22(1), 75 (2015). 19. M. S. C. Marc, “Manual Volume A: Theory and User Information”, 210 (2015).
정 정	(pp.31) 참고문헌 7번-18번까지로 표기 수정 7. R. Darveaux, K. Banerji, A. Mawer, and E. Mammo, “Reliability of Plastic Ball Grid Array Assembly”, Ball Grid Array Technology, McGraw-Hill, New York (1995). 8. J. H. Lau, J. L. Prince, W. Nakayama, and C. P. Wong, “Electronic Packaging: Design, Materials, Process, and Reliability”, McGraw-Hill, New York (1997). 9. E. Lin, D. Chang, D. S. Jiang, Y. P. Wang, and C. S. Hsiao, “Advantage and challenge of coreless Flip chip BGA Microsystems”, International Microsystems, Packaging, Assembly and Circuits Technology (IMPACT), Taipei, Taiwan, 346, IEEE (2007). 10. C. Chiu, K. C. Chang, J. Wang, and C. H. Lee, “Challenges of thin core PCB Flip Chip package on advanced Si Nodes”, Proc. 57th Electronic Components and Technology Conference (ECTC), 22 (2007). 11. S. H. Cho, T. E. Chang, J. Lee, and H. P. Park, “New dummy design and stiffener on warpage reduction in Ball Grid Array Printed Circuit Board”, Microelectronics Reliab., 50, 242 (2010). 12. J. H. Lau, and S.-W.R, Lee, “Effects of Build-Up Printed Circuit Board Thickness in the Solder Joint Reliability of a Wafer Level Chip Scale Package(WLCSP)”, Trans. Comp. Packag. Technol., 25(1), 3 (2002). 13. W. Sun, W. H. Zhu, C. K. Wang, A. Y. S. Sun, and H. B. Tan, “Warpage Simulation and DOE Analysis with Application in Package-on-Package Development”, Proc. 9th EuroSimE 2008 - International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Micro-Systems (ESIME), Freiburg im Breisgau, Germany, 244, IEEE (2008). 14. Y. L. Tzeng, N. Kao, E. Chen, J. Y. Lai, Y. P. Wang, and C. S. Hsiao, “Warpage and Stress Characteristic Analyses on Package-on-Package (PoP) Structure”, Proc. 9th Electronics Packaging Technology Conference (EPTC), Singapore, 482, IEEE (2007). 15. W. Sun, W. H. Zhu, K. S. Le, and H. B. Tan, “Simulation Study on the Warpage Behavior and Board-level Temperature Cycling Reliability of PoP Potentially for High-speed Memory Packaging”, International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), Shanghai, 978, IEEE (2008).

정 정	16. S. H. Cho, H. I. Jung, and O. C. Bae, “Numerical Analysis on the Design Variables and Thickness Deviation Effects on Warpage of Substrate for FCCSP”, J. Microelectron. Packag. Soc., 19(3), 57 (2012). 17. S. H. Cho, D. H. Kim, Y. G. Oh, J. T. Lee, and S. S. Cha, “A Study on the Parameters of Design for Warpage reduction of Passive components Embedded Substrate for PoP”, J. Microelectron. Packag. Soc., 22(1), 75 (2015). 18. M. S. C. Marc, “Manual Volume A: Theory and User Information”, 210 (2015).
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	9. A. L. Moore, and L. Shi, “Emerging Challenges and Materials for Thermal Management of Electronics”, Mater Today., 17(4), 163 (2014).
정 정	(pp.37) 참고문헌 9번 수정
	9. A. A. Balandin, "Thermal Properties of Graphene and Nanostructured Carbon Materials", Nat. Mater., 10, 569 (2011).
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	6. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, 22(4), 91 (2015).
정 정	(pp.45) 참고문헌 6번 저널명 삽입
	6. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, J. Microelectron. Packag. Soc., 22(4), 91 (2015).
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	20. S. W. Jung, J. S. Choi, J. B. Koo, C. W. Park, B. S. Na, J. Y. Oh, S. S. Lee, and H. Y. Chu, “Stretchable Organic Thin-Film Transistors Fabricated on Elastomer Substrates Using Polyimide Stiff-Island Structures”, ECS Solid State Lett., 4(1), P1 (2015).
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	20. H. Hocheng and C. M. Chen, “Design, Fabrication and Failure Analysis of Stretchable Electrical Routings”, Sensors, 14, 11855 (2014).
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	7. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, 22(4), 91 (2015).
정 정	(pp.53) 참고문헌 7번 저널명 삽입
	7. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, J. Microelectron. Packag. Soc., 22(4), 91 (2015).
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	22. D. Park, K. S. Han, and T. S. Oh, Comparison of “Flip-Chip Bonding Characteristics on Rigid, Flexible, and Stretchable Substrates: Part II. Flip-Chip Bonding on Compliant Substrates”, Mater. Trans., 58(8), 1217 (2017).
정 정	(pp.53) 참고문헌 22번 쌍 따옴표 위치 수정
	22. D. Park, K. S. Han, and T. S. Oh, “Comparison of Flip-Chip Bonding Characteristics on Rigid, Flexible, and Stretchable Substrates: Part II. Flip-Chip Bonding on Compliant Substrates”, Mater. Trans., 58(8), 1217 (2017).

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요청부분	(pp.62) 참고문헌 6번 저널명 누락
	6. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, 22(4), 91 (2015).
정 정	(pp.62) 참고문헌 6번 저널명 삽입
	6. H. A. Oh, D. Park, K. S. Hahn, and T. S. Oh, “Elastic Modulus of Locally Stiffness-Variant Polydimethylsiloxane Substrates for Stretchable Electronic Packaging Applications”, J. Microelectron. Packag. Soc., 22(4), 91 (2015).
요청부분	(pp.62) 참고문헌 17번 쌍 따옴표 위치 오류
	17. J. C. Lotters, W. Olthuis, P. H. Veltink, and P. Bergveld, The Mechanical Properties of the Rubber Elastic Polymer Polydimethylsilicone for Sensor Applications“, J. Micromech.Microeng., 7, 145 (1997).
정 정	(pp.62) 참고문헌 17번 쌍 따옴표 위치 수정
	17. J. C. Lotters, W. Olthuis, P. H. Veltink, and P. Bergveld, “The Mechanical Properties of the Rubber Elastic Polymer Polydimethylsilicone for Sensor Applications”, J. Micromech. Microeng., 7, 145 (1997).
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	24. S. W. Jung, J. S. Choi, J. B. Koo, C. W. Park, B. S. Na, J. Y. Oh, S. S. Lee, and H. Y. Chu, “Stretchable Organic Thin-Film Transistors Fabricated on Elastomer Substrates Using Polyimide Stiff-Island Structures”, ECS Solid State Lett., 4(1), P1 (2015).
정 정	(pp.62) 참고문헌 24번 변경
	24. H. Hocheng and C. M. Chen, “Design, Fabrication and Failure Analysis of Stretchable Electrical Routings”, Sensors, 14, 11855 (2014).
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	26. D. Park, K. S. Han, and T. S. Oh, Comparison of “Flip-Chip Bonding Characteristics on Rigid, Flexible, and Stretchable Substrates: Part II. Flip-Chip Bonding on Compliant Substrates”, Mater. Trans., 58(8), 1217 (2017).
정 정	(pp.62) 참고문헌 26번 쌍 따옴표 위치 수정
	26. D. Park, K. S. Han, and T. S. Oh, “Comparison of Flip-Chip Bonding Characteristics on Rigid, Flexible, and StretchableSubstrates: Part II. Flip-Chip Bonding on Compliant Substrates”, Mater. Trans., 58(8), 1217 (2017).
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	Effect of Temperature and Compressive stress on the Dielectric and Piezoelectric Properties of PIN-PMN-PT Single Crystal
정 정	(pp.63) 영문 제목 대문자 수정
	Effect of Temperature and Compressive Stress on the Dielectric and Piezoelectric Properties of PIN-PMN-PT Single Crystal
요청부분	(pp.63) 1저자 소속 표기 기호 누락
	Jae Gwang Lim
정 정	(pp.63) 1저자 소속 표기 기호 삽입
	Jae Gwang Lim[1]
요청부분	(pp.63) 본문 문장 오류
	0.9 이상의 전기기계결합계수, 1,000 이상의 기계적 품질계수, 1,200 pC/N 이상의 압전계수를 나타내므로
정 정	(pp.63) 본문 문장 수정
	0.9 이상의 전기기계결합계수와 1,200 pC/N 이상의 압전계수를 나타내므로

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	연구에 사용된 조성은 PIN이 첨가된 PIN-PMN-PT 조성이다.
정 정	(pp.64) 본문 문장 수정
	연구에 사용된 조성은 In_2O_3가 첨가된 PIN-PMN-PT 조성이다.
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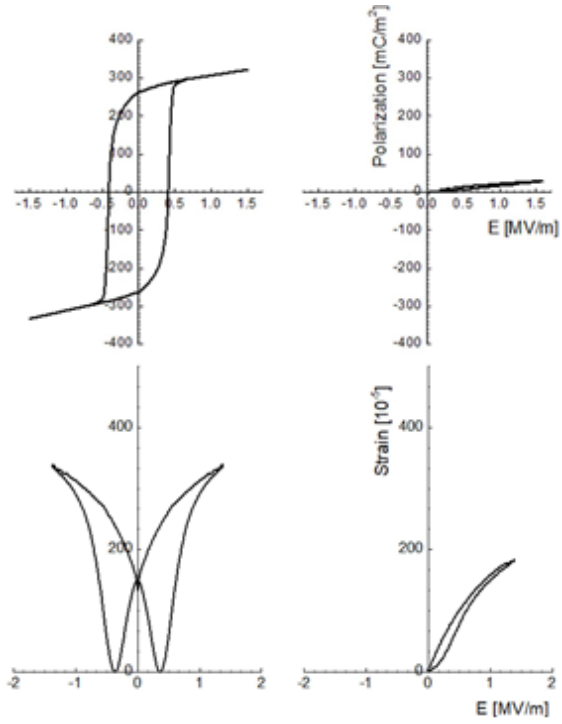
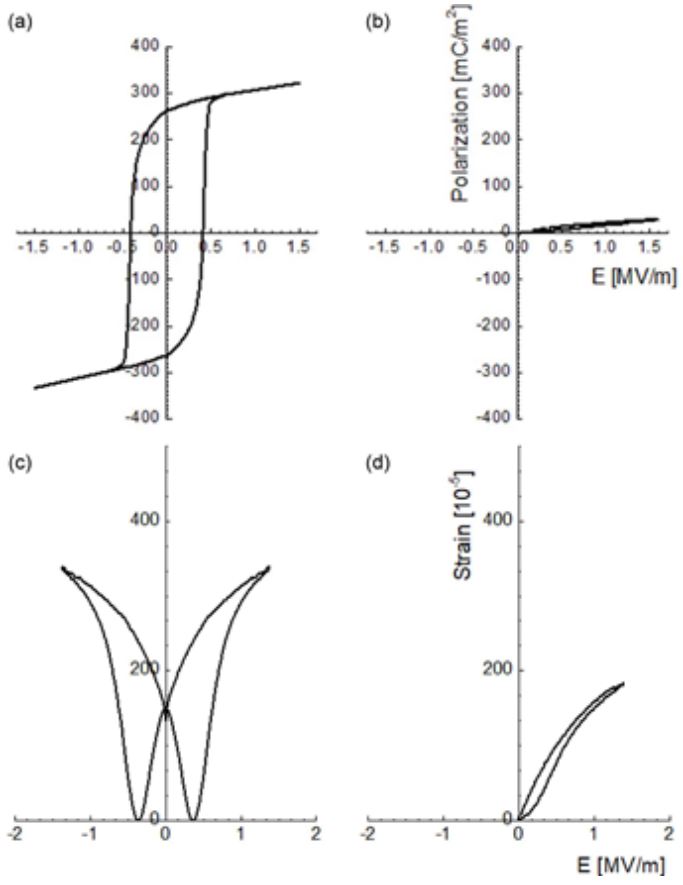
	
정 정	(pp.65) Fig. 3 구분 기호 삽입
	

요청부분	(pp.66) Table 1. 기호 누락
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정 정	(pp.66) Table 1. 기호 삽입
	Table 1. Change of d_{33} [pC/m] in PMN-PIN-PT with temperature and compressive stress change
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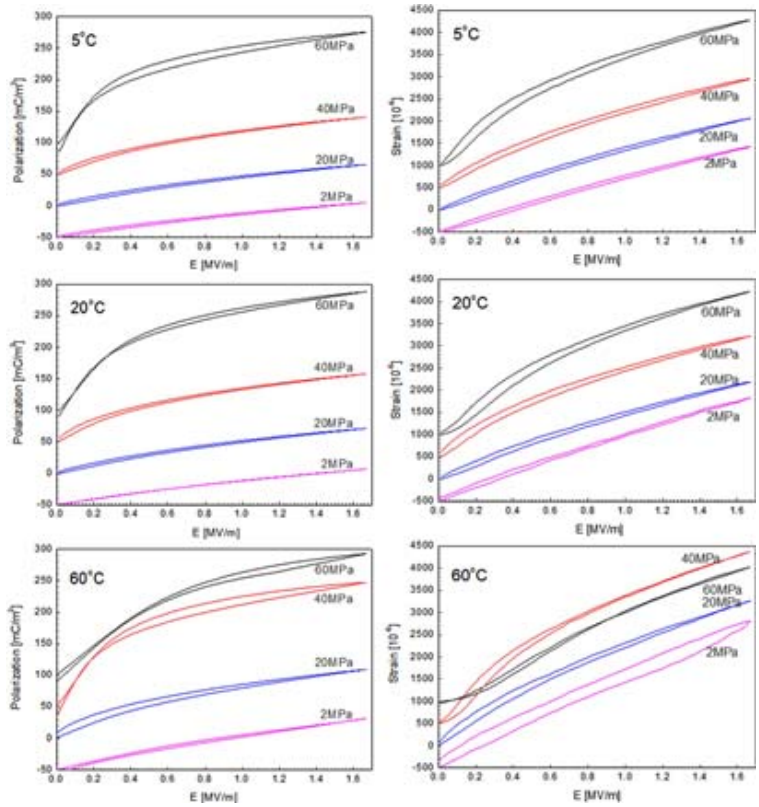
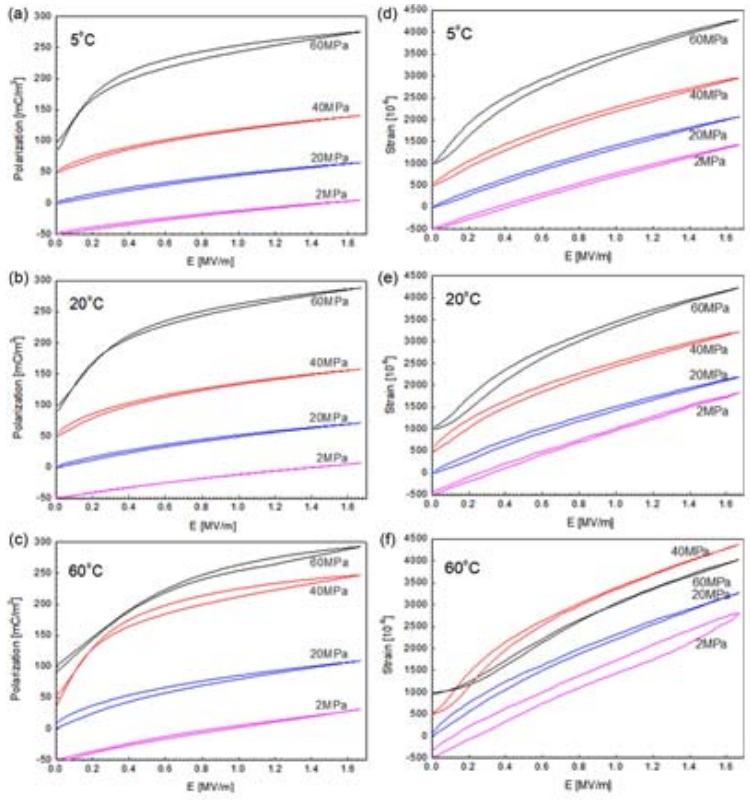
	
정 정	(pp.67) Fig. 4 구분 기호 삽입
	

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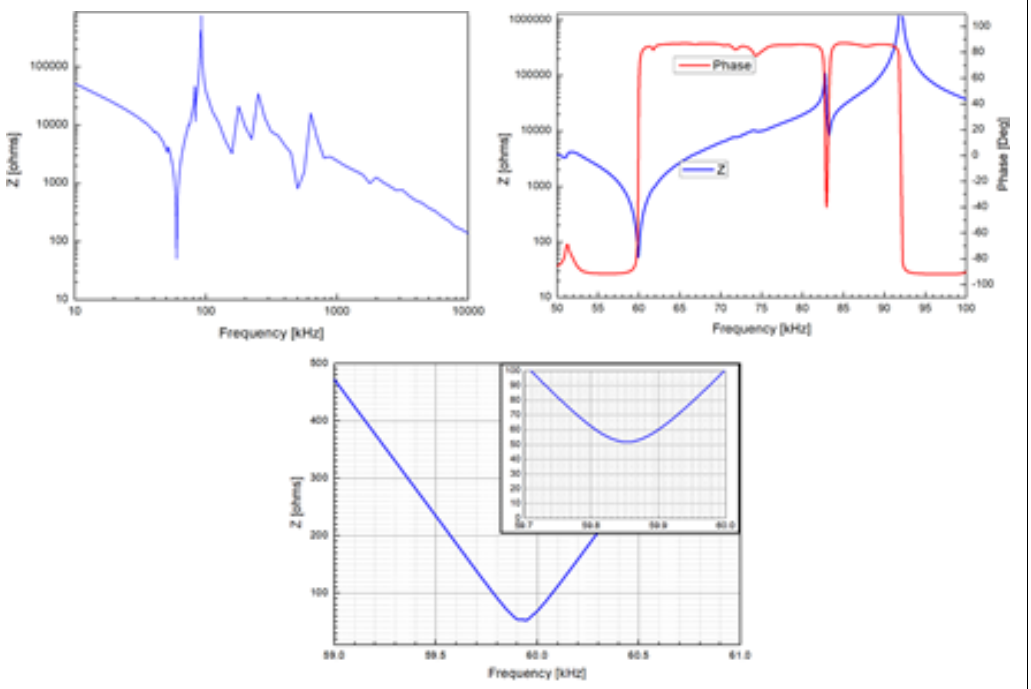
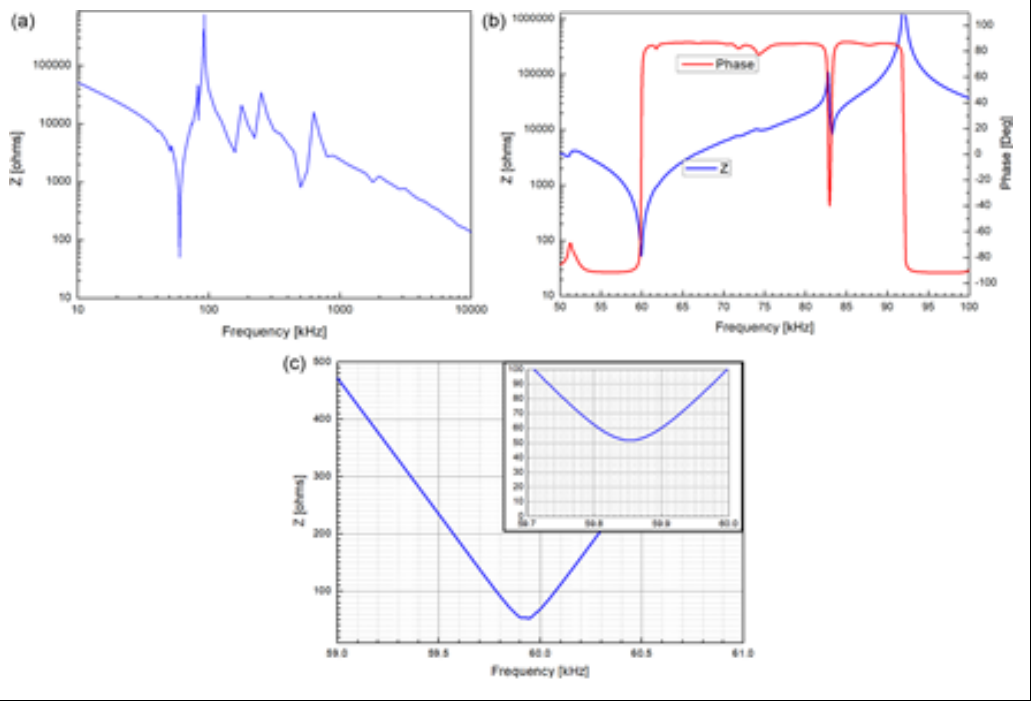
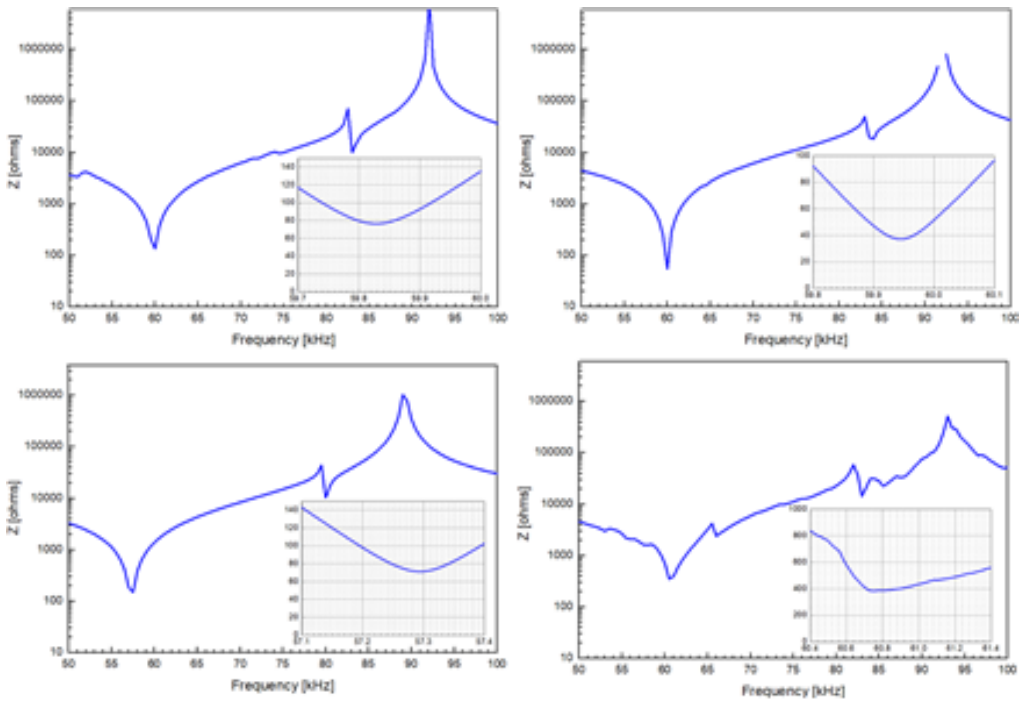
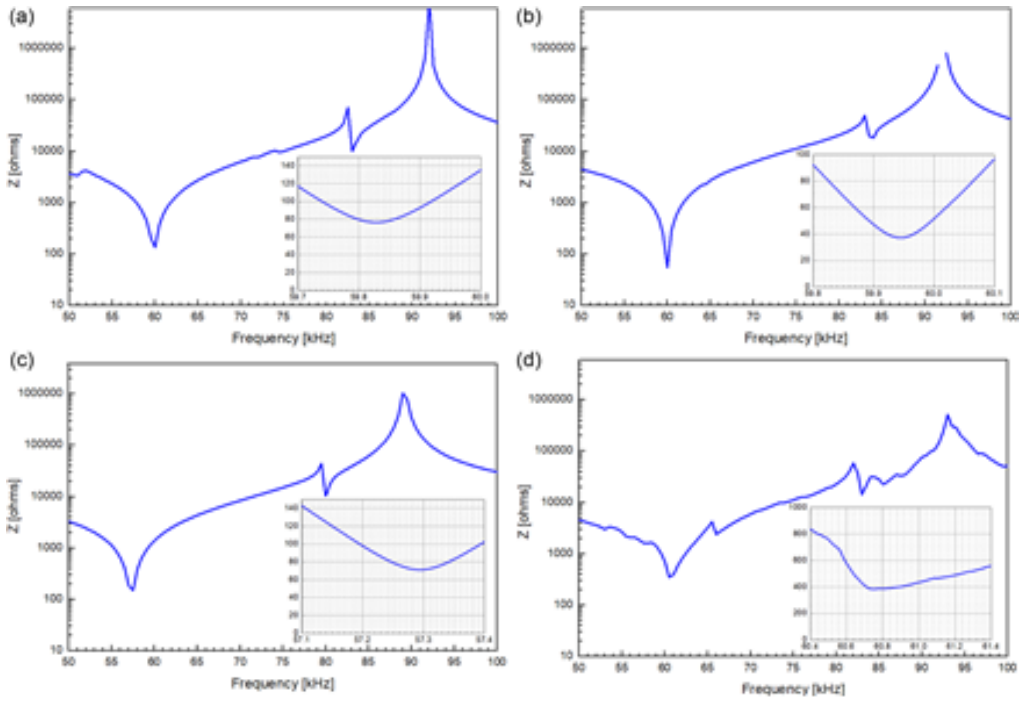
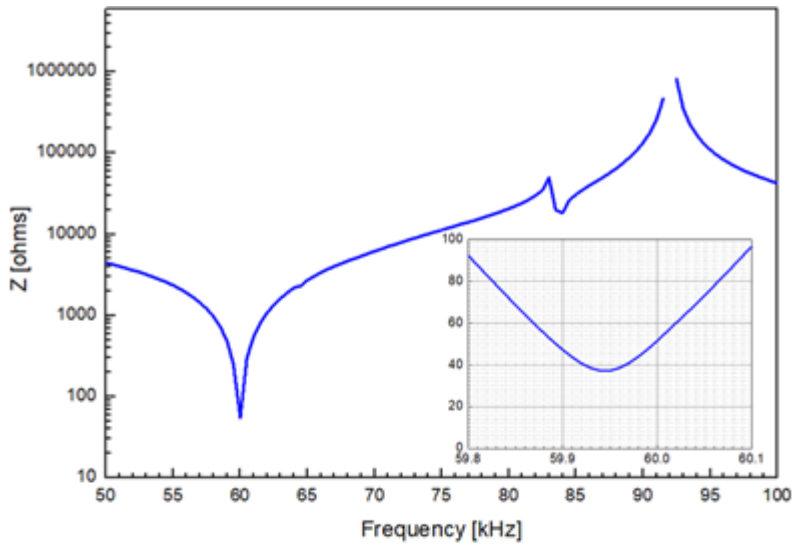
정 정	(pp.71) Fig. 3 구분 기호 삽입

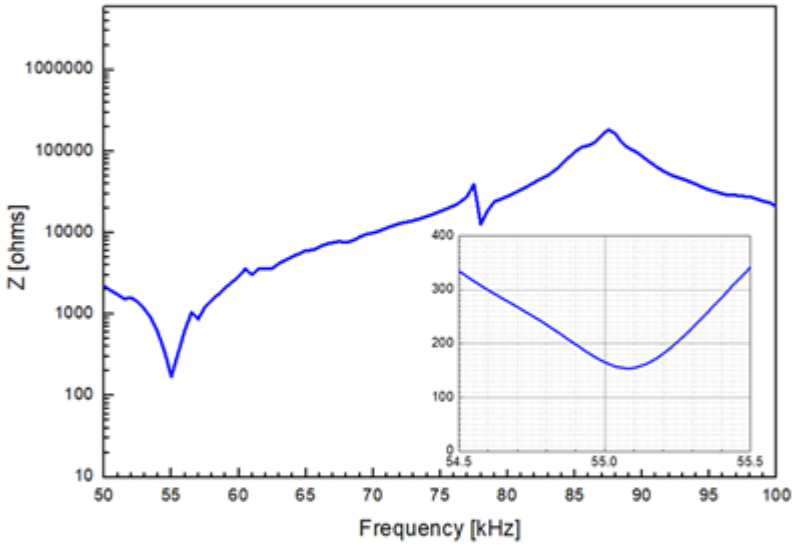


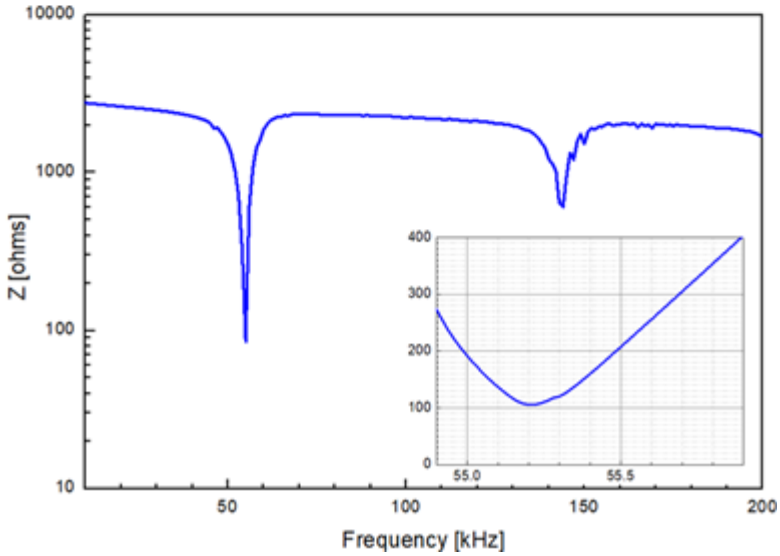


요청부분	(pp.72) Fig. 4 구분 기호 누락
	
정 정	(pp.72) Fig. 4 구분 기호 삽입
	

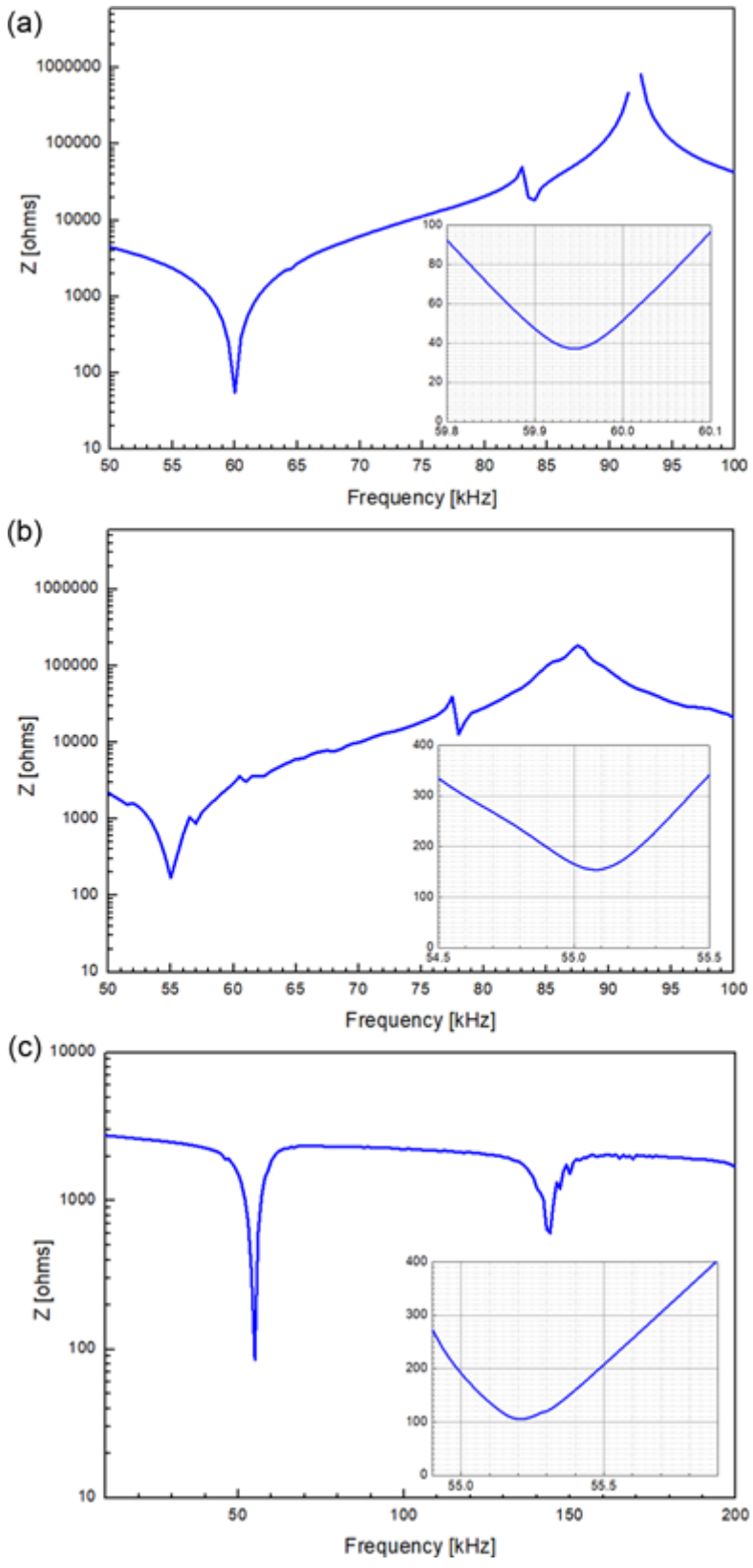
요청부분	(pp.73) Fig. 5 구분 기호 누락





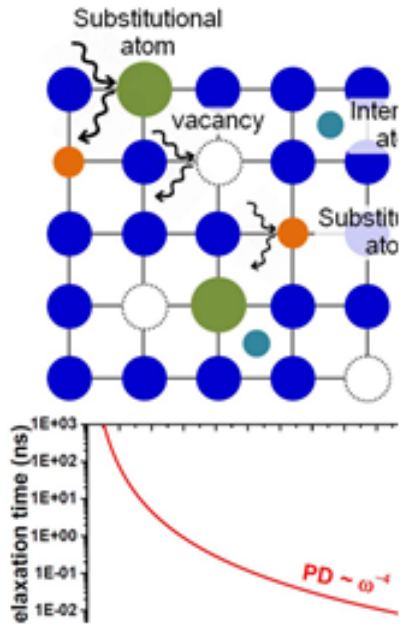


정 정	(pp.73) Fig. 5 구분 기호 삽입



학회지 및 페이지	J. Microelectron. Packag. Soc., 26(4), 83 (2019)
논문제목	“고상반응법에 의한 $LiBaPO_4:Eu^{2+}$ 계 형광체의 제조 및 광 발광 특성”
요청부분	(pp.88) 참고문헌 18번 오류
	18. S.-C. Kim et al., J. Kim, H. E. Lee, B. J. Kang, F. Rotermund, and S.–J. Kim, “The Crystal Structure and Phase Transitions of $LiBaPO_4$”, Solid State Sci., 83, 76 (2018).
정 정	(pp.88) 참고문헌 18번 수정
	18. S.-C. Kim, J. Kim, H. E. Lee, B. J. Kang, F. Rotermund, and S.–J. Kim, “The Crystal Structure and Phase Transitions of $LiBaPO_4$”, Solid State Sci., 83, 76 (2018).
학회지 및 페이지	J. Microelectron. Packag. Soc., 26(4), 101 (2019)
논문제목	“휨을 고려한 칩 패키지의 EMC/PCB 계면 접합 에너지 측정”
요청부분	(pp.105) 참고문헌 3번 쌍 따옴표 누락
	3. G. Kim, J. Lee, S.-H. Park, S. Kang, T.-S. Kim, and Y.-B. Park, “Comparison of Quantitative Interfacial Adhesion Energy Measurement Method between Copper RDL and WPR Dielectric Interface for FOWLP Applications (in Korean), J. Microelectron. Packag. Soc., 25(2), 41 (2018).
정 정	(pp.105) 참고문헌 3번 쌍 따옴표 삽입
	3. G. Kim, J. Lee, S.-H. Park, S. Kang, T.-S. Kim, and Y.-B. Park, “Comparison of Quantitative Interfacial Adhesion Energy Measurement Method between Copper RDL and WPR Dielectric Interface for FOWLP Applications (in Korean)”, J. Microelectron. Packag. Soc., 25(2), 41 (2018).
요청부분	(pp.105) 참고문헌 5번 오류
	5. I. Lee, S. Kim, J. Yun, K. Park
정 정	(pp.105) 참고문헌 5번 수정
	5. I. Lee, S. Kim, J. Yun, K. Park, and T.-S. Kim, "Interfacial toughening of solution processed Ag nanoparticle thin films by organic residuals", Nanotechnology, 23(48), 485704 (2012).
요청부분	(pp.105) 참고문헌 6번-15번 전체 번호 오류
	7. T. Yoon, W. C. Shin, T. Y. Kim, J. H. Mun, T.-S. Kim, and B. J. Cho, “Direct Measurement of Adhesion Energy of Monolayer Graphene As-Grown on Copper and Its Application to Renewable Transfer Process”, Nano Letters, 12(3), 1448 (2012). 8. W. Kim, J. Choi, J.-H. Kim, T. Kim, C. Lee, M. Kim, B. J. Kim, and T.-S. Kim, “Comparative Study of the Mechanical Properties of All-Polymer and Fullerene–Polymer Solar Cells: The Importance of Polymer Acceptors for High Fracture Resistance”, Chemistry of Materials, 30(6), 2102 (2018). 9. C. Kim, T.-I. Lee, M. S. Kim, and T.-S. Kim, “Mechanism of warpage orientation rotation due to viscoelastic polymer substrates during thermal processing”, Microelectronics Reliability, 73, 136 (2017). 10. M.-Y. Tsai, H.-Y. Chang, and M. Pecht, “Warpage analysis of flip-chip PBGA packages subject to thermal loading”, IEEE Transactions on Device and Materials Reliability, 9(3), 419 (2009). 11. H.-W. Liu, Y.-W. Liu, J. Ji, J. Liao, A. Chen, Y.-H. Chen, N. Kao, and Y.-C. Lai, “Warpage characterization of panel fanout (P-FO) package”, Proc. 64th Electronic Components and Technology Conference (ECTC), IEEE (2014). 12. G. Kelly, C. Lyden, W. Lawton, J. Barrett, A.Saboui, H. Pape, and H. J. B. Peters, “Importance of molding compound chemical shrinkage in the stress and warpage analysis of PQFPs”, IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, 19(2), 296 (1996). 13. C. Kim, H. Choi, M. Kim, and T.-S. Kim, “Packaging Substrate Bending Prediction due to Residual Stress (in Korean)”, J. Microelectron. Packag. Soc., 20(1), 21 (2013). 14. S. C. Liu, and S. J. Hu, “Variation simulation for deformable sheet metal assemblies using finite element methods”, Journal of manufacturing science and engineering, 119(3), 368 (1997). 15. D.-L. Chen., T.-C. Chiu, T.-C. Chen, M.-H. Chung, P.-F. Yang, and Y.-S. Lai, “Using DMA to simultaneously acquire Young's relaxation modulus and time-dependent Poisson's ratio of a viscoelastic material”, Procedia Engineering, 79, 153 (2014).

정 정	(pp.105) 참고문헌 6번-14번까지로 표기 수정
	6. T. Yoon, W. C. Shin, T. Y. Kim, J. H. Mun, T.-S. Kim, and B. J. Cho, “Direct Measurement of Adhesion Energy of Monolayer Graphene As-Grown on Copper and Its Application to Renewable Transfer Process”, Nano Letters, 12(3), 1448 (2012). 7. W. Kim, J. Choi, J.-H. Kim, T. Kim, C. Lee, M. Kim, B. J. Kim, and T.-S. Kim, “Comparative Study of the Mechanical Properties of All-Polymer and Fullerene–Polymer Solar Cells: The Importance of Polymer Acceptors for High Fracture Resistance”, Chemistry of Materials, 30(6), 2102 (2018). 8. C. Kim, T.-I. Lee, M. S. Kim, and T.-S. Kim, “Mechanism of warpage orientation rotation due to viscoelastic polymer substrates during thermal processing”, Microelectronics Reliability, 73, 136 (2017). 9. M.-Y. Tsai, H.-Y. Chang, and M. Pecht, “Warpage analysis of flip-chip PBGA packages subject to thermal loading”, IEEE Transactions on Device and Materials Reliability, 9(3), 419 (2009). 10. H.-W. Liu, Y.-W. Liu, J. Ji, J. Liao, A. Chen, Y.-H. Chen, N. Kao, and Y.-C. Lai, “Warpage characterization of panel fanout (P-FO) package”, Proc. 64th Electronic Components and Technology Conference (ECTC), IEEE (2014). 11. G. Kelly, C. Lyden, W. Lawton, J. Barrett, A.Saboui, H. Pape, and H. J. B. Peters, “Importance of molding compound chemical shrinkage in the stress and warpage analysis of PQFPs”, IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part B, 19(2), 296 (1996). 12. C. Kim, H. Choi, M. Kim, and T.-S. Kim, “Packaging Substrate Bending Prediction due to Residual Stress (in Korean)”, J. Microelectron. Packag. Soc., 20(1), 21 (2013). 13. S. C. Liu, and S. J. Hu, “Variation simulation for deformable sheet metal assemblies using finite element methods”, Journal of manufacturing science and engineering, 119(3), 368 (1997). 14. D.-L. Chen., T.-C. Chiu, T.-C. Chen, M.-H. Chung, P.-F. Yang, and Y.-S. Lai, “Using DMA to simultaneously acquire Young's relaxation modulus and time-dependent Poisson's ratio of a viscoelastic material”, Procedia Engineering, 79, 153 (2014).
학회지 및 페이지	J. Microelectron. Packag. Soc., 26(4), 141 (2019)
논문제목	“LED 광을 이용한 그림자 무아레 방법의 감도 향상 및 모바일 전자 기판의 변형 측정”
요청부분	(pp.148) 참고문헌 3번 시작 쌍 따옴표 누락
	3. Y. J. Kang, W. J. Ryu, and Y. K. Kwon, A Study on the Improvement of Accurasy of Surface Measurement in the Phase-Shifting Shadow Moiré Method”, J. of KSPE., 15(10), 96 (1998).
정 정	(pp.148) 참고문헌 3번 시작 쌍 따옴표 삽입
	3. Y. J. Kang, W. J. Ryu, and Y. K. Kwon, “A Study on the Improvement of Accurasy of Surface Measurement in the Phase-Shifting Shadow Moiré Method”, J. of KSPE., 15(10), 96 (1998).

학회지 및 페이지	J. Microelectron. Packag. Soc., 26(4), 157 (2019)
논문제목	“열전소재 성능 증대를 위한 점결함 제어 전략”
요청사항	(pp.159) Fig. 2 잘림
	
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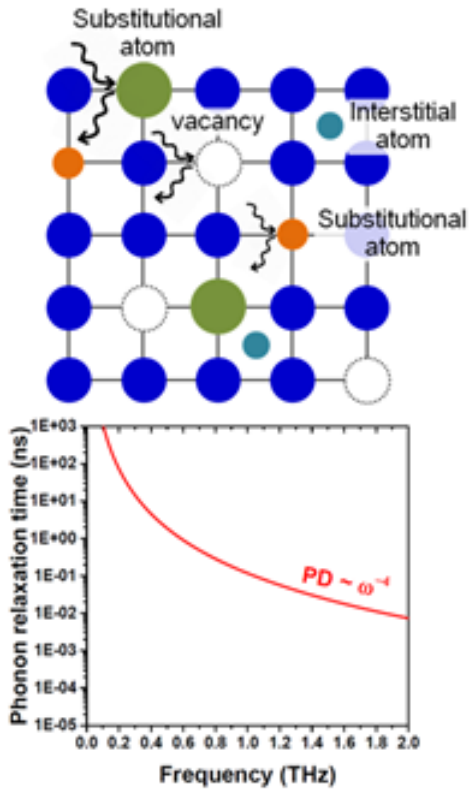
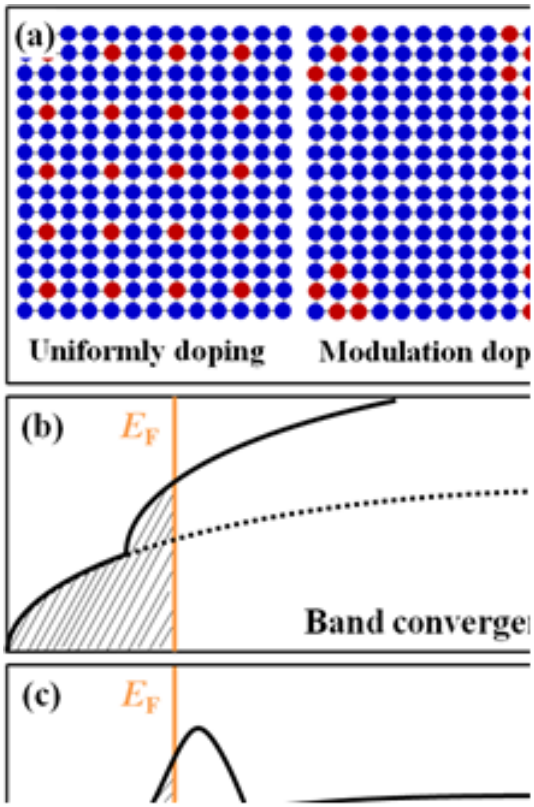
	

요청사항	(pp.159) Fig. 3 잘림
	
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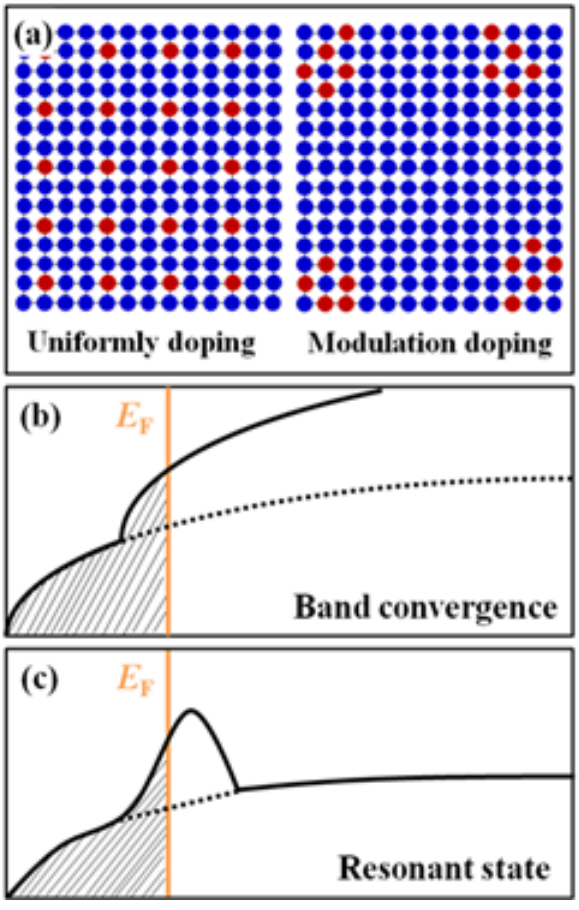
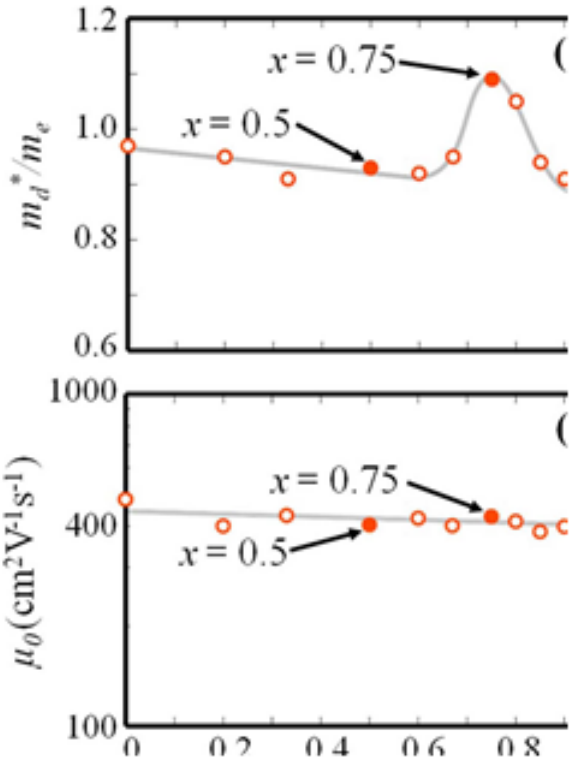
	

요청사항	(pp.160) Fig. 4 잘림
	
정 정	(pp.160) Fig. 4 교체