C_{gd} 성분을 포함한 공정별 주요 잡음원 천이 과정 연구

The transition of dominant noise source for different CMOS process with C_{gd} consideration

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ABSTRACT

In this paper, we analyze the dominant noise source of conventional inductively degenerated common-source (CS) cascode low noise amplifier (LNA) when width and gate length of stacked transistors vary. Analytical MOSFET and its noise model are used to estimate the contributions of noise sources. All parameters are based on measured data of 60nm, 90nm and 130nm CMOS devices. Based on the noise analysis for different frequencies and device parameters including process nodes, the dominant noise source can be analyzed to optimize noise figure on the configuration. We verified analytically that the intuctively degenerated CS topology can not sustain its benefits in noise above a certain operation frequency of LNA over different process nodes.

Keywords : CMOS process, noise figure, low noise amplifier (LNA), noise transition point, Cgd consideration.

Ⅰ. Introduction

A low noise amplifier (LNA) is one of the most critical circuit block in a wireless transceiver. As the first block to interface the incoming RF signal from antenna, noise figure of LNA dominates overall noise performance of the system. As the scaling down of CMOS technology continues, the most advanced short channel MOSFETs have achieved cutoff frequency (f_T) and maximum oscillation frequency (f_{MAX}) higher than 200 GHz [1-2]. Consequently, the operation frequency of CMOS circuits easily go up to several tens of gigahertz range. Although these indices suggest the feasibility of CMOS devices for the operation [3], they do not provide design insights for RF circuit optimization. To that affect, many researchers have explored the design optimization using device parameters in ahead of actual design [4-5]. Also, studies on different topologies of LNA for various frequency band with fixed process node have conducted [6-7]. However, little research results on dominant noise source analysis have been reported for different process node and design parameters.

In this paper, we analyze noise figure of LNA by dividing it into three components with analytical models. For better estimation, we additionally considered following components that are usually not considered in conventional model but affect more at higher frequency: gate to drain capacitance (C_{gd}), gate electrode resistance of transistor, parasitic resistance of inductors, and etc. We present an approach to optimize the design of LNA with inductively degenerated common-source (CS) cascode configuration. The analysis on transition point of dominant noise sources for different process node gives us an insight on design parameters that we are supposed to focus on to improve noise performance.

Ⅱ. Noise figure of cascode LNAs with Cgd consideration

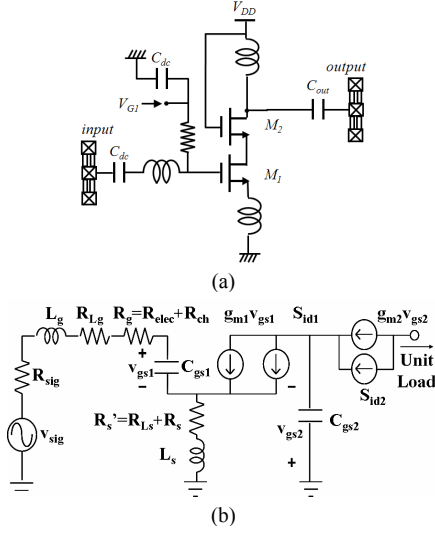Conventional inductively degenerated CS cascode

Fig. 1 (a) Schematic of inductively degenerated common-source cascode LNA. (b) Small signal equivalent circuit of (a)

LNAs schematic and its small signal equivalent circuit with Cgd consideration are shown in Fig. 1. As scaling down the technology, the effect of the C$_{gd}$ can not be ignored any more especially at mm-wave frequency range. From that equivalent circuit, the input matching condition (Re[Z$_{in}$], Im[Z$_{in}$]) and noise figure equation (NF-1) can be derived as equations (1)-(3) [7]. The channel thermal noise, Sid, is analytically modeled as equation (4).

$$\text{Re}[Z_{in}] = R_1 + \frac{\frac{g_{m1}L_s}{C_{gs1}}\left(1 + \frac{C_{gd1}}{C_{gs1}}\frac{g_{m1}}{g_{m2}}\right) + \frac{C_{gd1}}{C_{gs1}}\frac{g_{m1}}{g_{m2}}\left(\frac{C_{gd1}}{C_{gs1}}(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}) + \frac{C_{gs2}}{C_{gs1}}\frac{1}{g_{m2}}\right)}{\left[1 + \frac{C_{gd1}}{C_{gs1}}\left(1 + \frac{g_{m1}}{g_{m2}}\right)\right]^2} \quad \textbf{(1)}$$

$$\text{Im}[Z_{in}] = \omega L_g - \frac{1}{\omega C_{gs1}\left[1 + \frac{C_{gd1}}{C_{gs1}}\left(1 + \frac{g_{m1}}{g_{m2}}\right)\right]} \quad \textbf{(2)}$$

$$NF - 1 = \frac{R_1}{R_{sig}} + 4R_{sig}\frac{\alpha}{\gamma}\frac{S_{id1}}{4kT} + 4R_{sig}\frac{\beta}{\gamma}\frac{S_{id2}}{4kT} \quad \textbf{(3)}$$

$$S_{id} = 4kT_0\left(\frac{m}{(V_{GT} - V_0)} + \frac{mV_0}{V_{GT}(V_{GT} - V_0)}\right)I_D \quad \textbf{(4)}$$

In equation (1), R$_1$ is the sum of the parasitic

resistance of the gate inductor, gate electrode resistance of transistor, and the sum of parasitic resistance of the source inductor and transistor source resistance. Q-factor of inductors is assumed as 10 to extract the parasitic resistance. For the convenience, we call the 1st, the 2nd and the 3rd term of noise figure equation (3) as resistor, M1 transistor and M2 transistor noise term, respectively. The dominant term of noise figure varies for frequency range as explained in the next section. In other word, there are two cross point among three terms. These points varies with device width and process nodes. Therefore, design approach should be changed based on the target operating frequency and the process node to be used.
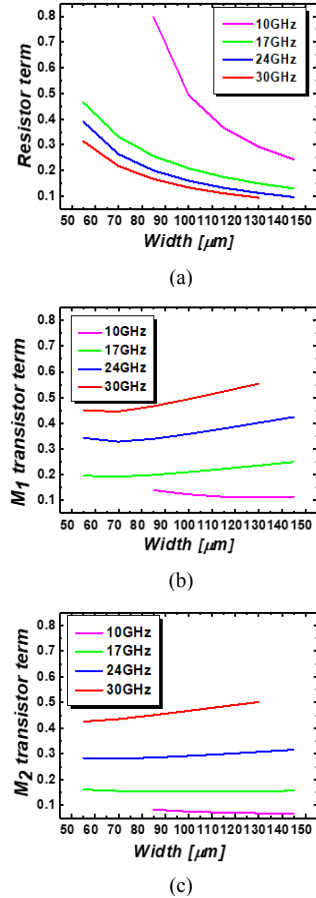

Fig. 2 At 60nm gate length, device width vs. (a) resistor term, (b) M1 transistor term, and (c) M2 transistor term

Ⅲ. Noise Analysis

Fig 2-(a), (b), (c) show each term in NF equation (3) for width variations as frequency increases. The resister noise term decrease as width increases to meet matching condition. On the contrary, both the transistor noise terms increase as width increases. The increasing of the width of transistors requires $1/\omega^2 C_{gs}$ to be decreased and R_1 also decreases. Therefore, the resistor term decreases as the width increases. Otherwise, transistor terms increase as width increases because S_{id} is proportional to IDS [8]. Consequently, the dominant noise term varies as frequency changes and its tendency for different process are shown in Fig 3-(a), (b), (c).
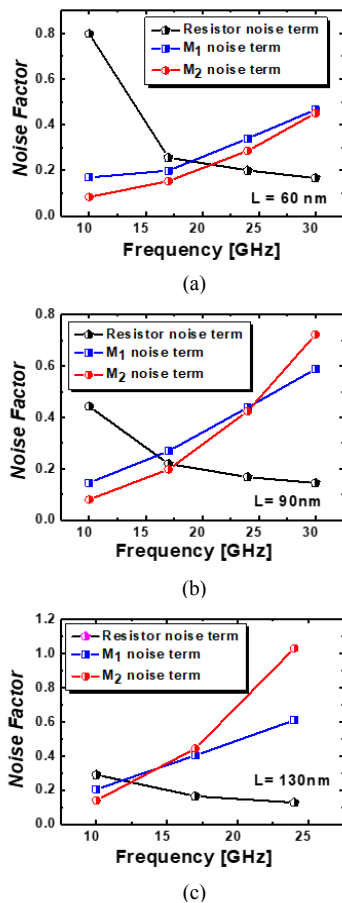
There are two cross points among three noise terms. We call the cross points as 1st and 2nd transition frequency where dominant noise term is changed from resistor term to M1 transistor term and from M1 transistor term to M2 transistor term, respectively. As the gate length decreases, both transition points increase for the same device width. Since gate resistance which mainly attributes to resistor noise term increases as gate length decreases, the 1st transition point increases as gate length decreases. On the other hand, cut-off frequency f_T increases as gate length decreases. Therefore, the 2nd transition point increases as gate length decreases. Considering the width variation, both transition points vary as shown in Fig. 4-(a),(b).
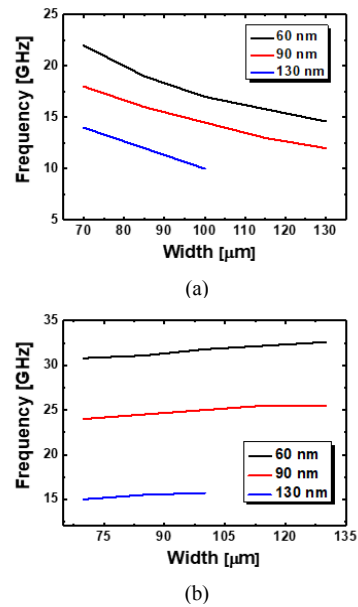

(a)

(b)

(c)

Fig. 3 Each noise term vs. frequency for gate length of (a) 60nm, (b) 90nm, and (c) 130nm.

(a)

(b)

Fig. 4 (a) The first transition frequency, and (b) the second transition frequency vs. width.

The gate resistance decreases as device width increases while the transistor noise terms increase. Therefore, the 1st transition point becomes lower as the width increases. However, the 2nd transition point is almost flat for the width variation. Because cut-off frequency of each device is almost same even with the width variation if the gate length is the same. In addition,

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S_{id} of both transistor terms increase proportional to width. Based on the results, we can claim the following design strategy. The Q-factor and gate resistance which largely contribute on the resistor noise term are most important factors at lower frequency than the 1st transition point. Furthermore, the conventional cascode topology has no more advantages in terms of noise at higher frequency than the 2nd transition point. At low frequency for example, the larger width of device can reduce the noise more by reducing the gate resistance. However, if the larger width of device is used, the lower 1st transition frequency is obtained. Consequently, using large width of device for reducing noise is only effective below the 1st transition frequency.

Ⅳ. Conclusion

In this paper, we analyze noise figure of LNAs for frequency and width variations. Also we explored the noise transition point for gate length variation. Two transition points vary for frequency and width and show the different tendency with the different gate length. Based on the results, we could claim that the conventional cascade topology has only advantages in noise performance until the operating frequency is lower than the 2nd transition point. Also, we verified that using larger width of device to reduce the noise is only effective below the 1st transition frequency.

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