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65nm CMOS 기술에서의 cascode기반 LNA 잡음지수 분석

Noise analysis of cascode LNA with 65nm CMOS technology

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ABSTRACT

In this paper, we analyzed the noise figure of cascode low noise amplifier (LNA) based on the measured data of 65nm CMOS devices. By using the channel thermal noise model of transistors, we expanded noise figure equation and divided the equation into three parts to see its contributions to noise figure. We also varied design parameters such as bias point, transistor gate width, and operating frequency. Our results show that different noise sources dominate at the different operating frequencies. One can easily find the noise transition frequency with device models in ahead of the practical design. Therefore, this research provides a low noise design approach for different operating frequencies.

Keywords : CMOS process, noise figure, low noise amplifier (LNA), cascode configuration, design optimization

Ⅰ. Introduction

In the past several decades, the scaling-down of CMOS technology has continued. As a result, the cut-off frequency (fT) and the maximum oscillation frequency (fMAX) of a MOS transistor has exceeded more than few hundred gigahertz [1-2]. Consequently, CMOS circuits also have extended its operation frequency to mm-wave regime. A CMOS low-noise Amplifier (LNA) is one of the most critical blocks in a CMOS wireless transceiver. As the first stage in the receiver, noise figure of LNA dominates overall noise figure of the system [3]. Many researchers have explored the different topologies of LNA for various but specific frequency band [4-6]. The inductively degenerated common-source topology is most conventional one because it achieves high gain and low noise figure with relatively easy input and output matching. Although many optimization studies on the conventional topology have conducted [7-8], little research results on noise characteristics of mm-wave LNA have been reported in scope of frequency and device parameter transitions.

In this paper, we present an approach to optimize the noise characteristics of mm-wave cascode LNA. Here, we focused on common-source topology with source degeneration inductor but same approach can be applied to other configurations. All parameters used in this research are based on measured data of 65 nm CMOS devices. The unit finger width of transistor is 0.8 μm.

Ⅱ. Noise figure of cascode LNAs

$$NF-1=\frac{R_1}{R_S}+\frac{S_{id1}}{4kT_S}\frac{(R_S+R_1)^2}{R_S}\left(\frac{f}{f_{T1}}\right)^2+\frac{S_{id2}}{4kT_S}(4R_S)\left(\frac{f}{f_{T1}}\right)^2\left(\frac{f}{f_{T2}}\right)^2 \quad (1)$$

$, where$

$S_{id}=$

$$4kT_0\frac{4V_{GT}^2+10V_0^2+7V_0V_{GT}+\frac{2}{3}\frac{V_0^3}{V_{GT}-V_0}ln\frac{|2V_{GT}-V_0|}{V_0}}{3(V_{GT}-V_0)(V_{GT}+V_0)^2}mI_{DS}$$

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Fig.1 shows a schematic of conventional cascode LNAs and its samll signal equivalent circuit. Noise figure of the LNA can be expressed as equation (1) when perfect input and output matching are assumed. Here, $V_{GT}=V_{GS}-V_{TH}$, $V_O=I_{DS}/WC_{ox}v_{sat}$, and m is the body-effect coefficient. In equation (1), R_1 is the sum of R_{Lg}, R_{elec} and R_s'. R_{Lg} is the parasitic resistance of the gate inductor, and R_{elec} is gate electrode resistance of transistor, and R_s' is the sum of parasitic resistance of the source inductor and transistor source resistance, R_s. Q-factor of inductors is set to be 10 to extract the parasitic resistance. The channel thermal noise, Sid is analytically modeled as shown in Fig.2. This model predicts S_{id} well for short channel device as well as long channel device [9]. Using these analytical models, we investigated a design approach based on the noise analysis which will be explained in the next section. We focused on the noise characteristics of single stage cascode LNA. Although additional stage might be required to obtain enough gain for millimeter freqeuncy band, noise figure of entire LNAs is dominated by noise figure of first stage by Friis equation [1].

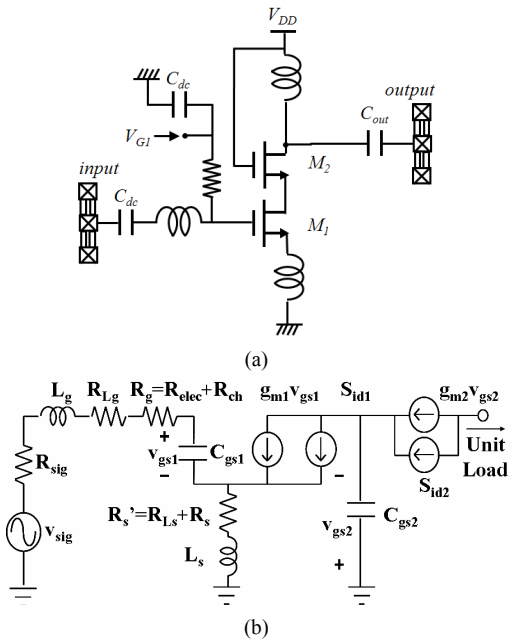

Fig. 1 (a)Schematic of a single stage cascode LNA. (b) Small signal equivalent circuit of cascode LNA.

Ⅲ. Noise Analysis of cascode LNAs

Fig 3-(a), (b), (c) show 3 terms in NF equation (1) as frequency increases. As frequency increases, $1/\omega^2C_{gs}$ decreases and L_g and L_s get smaller and thus, 1st term also decreases. However, the 2nd term and the 3rd term increase as f/f_t increases. Consequently, dominant term of equation (1) changes based on the frequency range as shown in Fig 3-(d). At frequency below 20 GHz, the 1st term dominates whereas the 3rd term dominates at frequency above 40 GHz. At frequency between 20 GHz and 40 GHz, the 2nd term dominates.

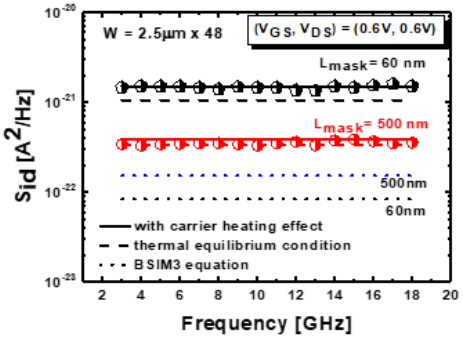

Fig. 2 Sid vs. Frequency

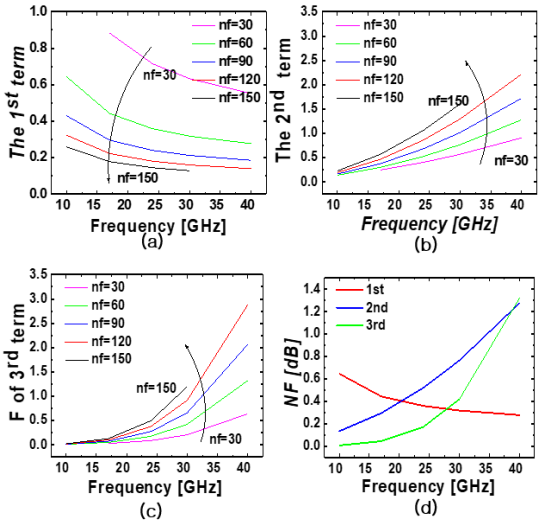

Fig. 3 (a) First term, (b) second term, and (c) third term of equation (1) vs. frequency variation. (d) Each term vs. frequency dependency for transistors with 60 fingers case.

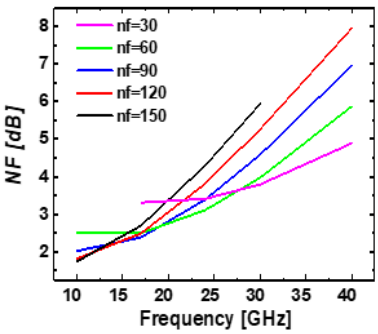

Fig. 4 Noise figure of LNA vs. frequency variation for different widths.

Consequently, noise figure of LNA is more dependent on frequency for wider devices as shown in Fig. 4. Here, we can explore noise figure dependancy on device width for different frequencies to optimize the noise figure. As shown in Fig. 5-(a), (b), (c), the 1st term of equation (1) decreases while the 2nd and the 3rd term increase as the number of fingers increases. To achieve input conjugate matching, the condition of $1/\omega^2C_{gs}= L_g+L_s$ should be satisfied. As the width increases, therefore, $1/\omega^2C_{gs}$ decreases and R_{Lg}, R_{elec}, and R_s also decrease. To that affect, the 1st term decreases as the width increases. On the contrary, the 2nd and the 3rd term increase as the width increases since S_{id} is proportional to I_{DS}. Based on

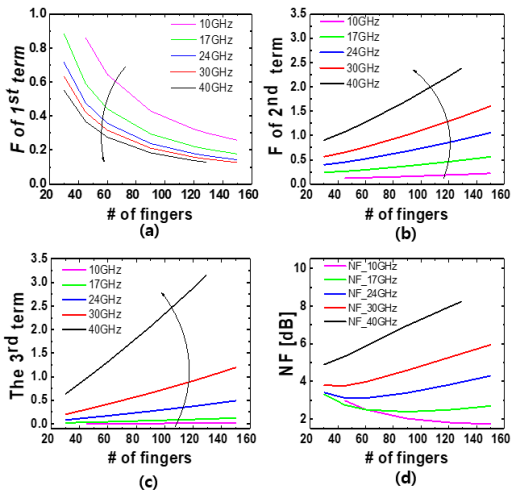

Fig. 5 (a) First term, (b) second term, and (c) third term of equation 1 vs. frequency. (d) Each term vs. frequency for transistors with 60 fingers.

the results, we can conclude that using smaller width of transistor for the first stage LNAs can be advantageous after certain point of frequency (here, ~30GHz in this case) in terms of noise figure and power consumption. Because both the 2nd and the 3rd term increase faster than the 1st term with number of fingers as shown in Fig. 5-(d).

Ⅳ. Conclusion

In this paper, we analyzed dominant noise sources for different frequency regimes. By investigating noise figure of mm-wave LNAs for different widths, we presented a method to optimize LNA design. This work can be performed for different process nodes to find the frequency point where the MOSFET channel noise dominates and smaller width is advantageous beyond the point.

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