Received: 11 December 2017 | Revised: 18 April 2018 | Accepted: 5 July 2018

DOI: 10.4218/etrij.2017-0319

ORIGINAL ARTICLE

WILEY ETRI Journal

Research of the adaptive control on modulation factor for PSR fly-back PSM converter

Lei Tian[1,2] | **Qinqin Li**[3] | **Weiheng Wang**[4]

[1]Institute of Modern Physics, Northwest University, Shaanxi Xi'an, China.

[2]Department of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an, China.

[3]Department of Electronic Engineering, Xidian University, CAD Institute, Xi'an, China.

[4]Institut Sup Galilée, Université Paris 13, Villetaneuse, France.

Correspondence
Lei Tian, Institute of Modern Physics, Northwest University, Shaanxi Xi'an, China and Department of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an, China.
Email: tianlei@xupt.edu.cn

Funding information
National scientific research foundation of China, Grant/Award Number: 61301067; Shaanxi Provincial Department of Education scientific research project, Grant/Award Number: 17JK0690; social science planning project of Shaanxi Province, Grant/Award Number: 2016R022

The energy balance (EB) model of a primary side regulation (PSR) fly-back converter in the discontinuous conduction mode (DCM) is discussed in this paper. Based on this EB model, the stability of a PSR fly-back converter in the pulse skipping mode (PSM) is analyzed, and a self-adapting modulation factor control strategy is proposed. Theoretical analysis and simulation results show that by saving an optocoupler and correlative circuits, which are necessary in traditional PSM fly-back converters, the modulation factor tolerance controlled by this method is 1.26% on average, corresponding to the ideal value. Compared with traditional fly-back PSM controllers, the power saved in the sampler/comparator modules is 87% on average for a load range of 1 Ω to 1 kΩ.

KEYWORDS
energy balance, fly-back, PSM, PSR, self-adapting

1 | INTRODUCTION

With the increasing demand for power systems with lower power dissipation, the pulse skipping mode (PSM) has been widely implemented in various small power AC-DC/DC-DC converters due to its high efficiency under light loads [1,2]. Traditional PSM fly-back converters use optocouplers as the feedback components [3,4] and for sampling and detecting the output voltage (cycle-by-cycle) to determine the action of the MOSFET switch in the next clock cycle. This topology can offer a more accurate output voltage. However, the optocoupler and the correlative circuit occupy more space in a PCB, and introduce additional power dissipation and cost [5]. More power will be dissipated in the PSM controllers for detecting the output voltage and comparing the signal with the reference voltage (cycle-by-cycle) [6,7].

To overcome the above drawbacks, a PSM control strategy based on the primary side regulation (PSR) fly-back topology is proposed. This structure uses a resistive divider on a bias winding to collect the feedback voltage [8]. The signal is sampled and compared to the reference only in

the normal on/off state operation periods. This could regulate the modulation factor adaptively according to the load status [9,10]. In this study, an EB model of a PSM fly-back converter working in discontinuous conduction mode (DCM) was set up, and the changes in PSM modulation factor with load variations were analyzed. A modulation factor control strategy based on load variations was then established. The analysis results show that bifurcation may happen in the PSR fly-back PSM converters, but no chaos will occur in such systems. This is quite different from PWM converters where slope compensation is not introduced [11–13]. The simulation results show that the proposed strategy can stabilize the output voltage under different loads. The modulation factor follows an ideal value, and changes with load variations. More energy can be saved in the sampler/comparator module compared with the traditional PSM controllers under light loads.

2 | PRINCIPLE OF PSR FLY-BACK PSM MODULATION

Pulse skipping mode is a novel modulation mode different from PWM and PFM, which are based on a constant-frequency constant-width (CFCW) control pulse signal [14–16]. PSR fly-back converters use sense voltage on a bias winding, coupled with the primary side winding as the feedback voltage, to form a closed-loop control. A typical PSR fly-back PSM converter is shown in Figure 1.

The traditional modulation principle shown in Figure 1 is based on the characteristics of the PSR feedback. The energy stored in the secondary winding L_1 is transferred to the output stage only after M_1 turns off. After M_1 turns off, the sampling of V_{FB} can reflect the output voltage V_{out} accurately; however, it cannot be sampled during the skip period [17–19], as shown in Figure 2.

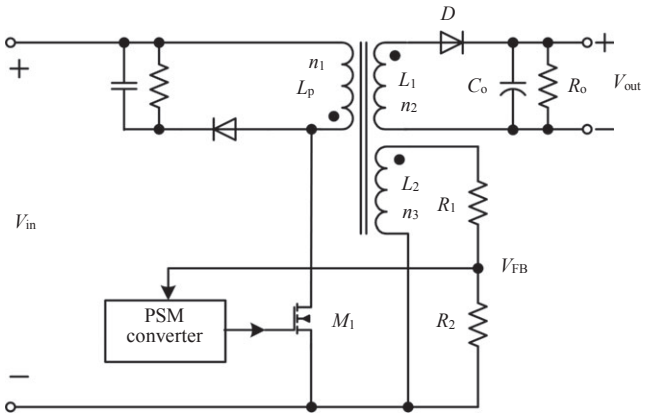

FIGURE 1 Topology of a primary side regulation fly-back converter

In Figure 2, the upper chart shows the sense voltage on the secondary winding, and the lower chart shows the driver signal. After M_1 turns off, V_{FB} is sampled after a delay of T_d (2.5 μs). If $V_{FB} < V_{ref}$ at the nth sampling, the PSM controller will send CFCW control pulses to M_1 and make it operate in the normal state during the next period; it then proceeds with the $(n + 1)$th sampling operation after M_1 turns off again. Otherwise, several control pulses are skipped according to the current load status to reduce V_{out}. Then, a detective pulse will be produced to turn off M_1 for the $(n + 1)$th sampling.

If $V_{FB} > V_{ref}$, in order to reduce the output voltage, the PSM controller controls M_1 across a number of conduction cycles.

After that, M_1 generates a pulse for the $(n + 1)$th sampling. In the PSM, the error amplifier can be replaced by an error comparator; therefore, the requirement of a feedback compensation circuit is greatly reduced and the circuit stability can be improved further.

Assume that the PSM controller makes M_1 work normally for k cycles in each energy cycle and skip s cycles. Here, the modulation factor M is set as $M = s/(k + s)$, $0 < M < 1$. In the traditional PSM modulation method, V_{FB} is sampled/compared $k + s$ times. On the other hand, in the proposed PSM modulation method based on PSR fly-back, V_{FB} is sampled k times. This reduces the power dissipations in the sampling circuits and error amplifier (EA). Especially, with a light load, the number of normal operation cycles k is less and the number of skipping cycles s is more. Therefore, the energy-saving effect is significant.

Thus, depending on the load, when $V_{FB} > V_{ref}$, the strategy of adaptively adjusting M_1 skips s cycles before detecting the pulse, resulting in a stable output voltage and reduced output ripples.

3 | EB MODEL OF DCM PSR FLY-BACK PSM CONVERTER

Ignoring the power consumed by the auxiliary winding L_2 (shown in Figure 1) in one period T, with the energy balance rule (EBR), the power supply energy is as follows [20]:

$$\Delta E_{in} = \Delta E_{Co} + \Delta E_{Lp} + \Delta E_{R_L}. \quad (1)$$

Here, ΔE_{Co} is the energy variation in C_o, ΔE_{Lp} is the energy variation in L_p, and ΔE_{RL} is the consumed energy by the load. When M_1 turns on, (1) becomes

$$\Delta E_{in} = \int_0^{DT} V_{in} I_{in} dt = V_{in}^2 (DT)^2 / 2L_p. \quad (2)$$

Here, D is the on-time duty cycle. ΔE_{Co} is the energy difference between the $(n + 1)$th and nth cycles in C_o:

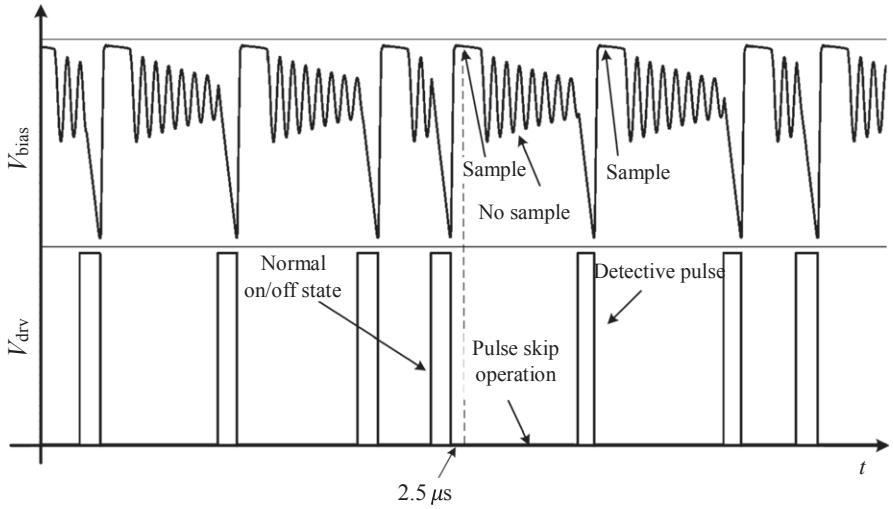

FIGURE 2 Sampling characteristics of a primary side regulation fly-back converter

$$\Delta E_{\mathrm{Co}} = E_{\mathrm{Co}}^{(n+1)} - E_{\mathrm{Co}}^{(n)} = \frac{1}{2} C_{\mathrm{o}} \left[\left(V_{\mathrm{out}}^{(n+1)}\right)^2 - \left(V_{\mathrm{out}}^{(n)}\right)^2 \right]. \quad (3)$$

The converter works in the DCM, and the inductance current is zero at the end of each period, that is,

$$\Delta E_{\mathrm{Lp}} = 0. \quad (4)$$

ΔE_{RL} can be approximated with the trapezoid integral rule and (3):

$$\begin{aligned} \Delta E_{R_{\mathrm{L}}} &\cong \left[\frac{\left(V_{\mathrm{out}}^{(n+1)}\right)^2 - \left(V_{\mathrm{out}}^{(n)}\right)^2}{R_{\mathrm{o}}} \right] \cdot \frac{T}{2} \\ &= \frac{T}{R_{\mathrm{o}} C_{\mathrm{o}}} \left(E_{\mathrm{Co}}^{(n+1)} + E_{\mathrm{Co}}^{(n)} \right). \end{aligned} \quad (5)$$

Substituting (3), (4), and (5) into (1), the output energy relationship within the nth and $(n + 1)$th periods is as follows:

$$\Delta E_{\mathrm{Co}}^{(n+1)} = \left(\frac{1 - \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}}{1 + \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}} \right) E_{\mathrm{Co}}^{(n)} + \frac{1}{1 + \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}} \Delta E_{\mathrm{in}}. \quad (6)$$

Set

$$\lambda = \frac{1 - \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}}{1 + \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}} < 1. \quad (7)$$

In Figure 1, as M_1 turns off at T_{d}, the sampled feedback voltage is

$$V_{\mathrm{FB}} = \frac{1}{N} \left(\frac{R_2}{R_1 + R_2} \right) V_{\mathrm{out}}. \quad (8)$$

where $N = n_2/n_3$.

For the EB model of the PSR fly-back PSM converter, assuming that the PSM controller samples during each cycle, a relation between the load condition and ideal modulation factor can be obtained.

Thus, when $V_{\mathrm{FB}} > V_{\mathrm{ref}}$, the PSM controller skips the next cycle. Substituting (3) into this condition, we get

$$E_{\mathrm{Co}}^{(n)} > \frac{1}{2} C_{\mathrm{o}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2. \quad (9)$$

Similarly, the condition where PSM controller operates in the next normal state is given by

$$E_{\mathrm{Co}}^{(n)} < \frac{1}{2} C_{\mathrm{o}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2. \quad (10)$$

When the control cycle is skipped, the system cannot draw energy from the power source; then, $\Delta E_{\mathrm{in}} = 0$. The EB model of the PSR fly-back PSM converter can be expressed as follows:

$$E_{\mathrm{Co}}^{(n+1)} \begin{cases} = \lambda E_{\mathrm{Co}}^{(n)} + \frac{1}{1 + \frac{T}{R_{\mathrm{L}} C_{\mathrm{o}}}} \Delta E_{\mathrm{in}} \\ \text{if } E_{\mathrm{Co}}^{(n)} < \frac{1}{2} C_{\mathrm{o}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2 \\ = \lambda E_{\mathrm{Co}}^{(n)} \\ \text{if } E_{\mathrm{Co}}^{(n)} > \frac{1}{2} C_{\mathrm{o}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2. \end{cases} \quad (11)$$

Here, the reference energy is defined as:

$$E_{\mathrm{ref}} = \frac{1}{2} C_{\mathrm{o}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2. \quad (12)$$

Assume that $E_{\mathrm{Co}} = E_{\mathrm{ref}}$ in the nth cycle, but E_{Co} cannot preserve the E_{ref} level in the $(n + 1)$th cycle; therefore, the maximum load of the system is

$$R_{\mathrm{min}} = \frac{2 L_{\mathrm{p}} \left[k \left(\frac{R_1 + R_2}{R_2} \right) V_{\mathrm{ref}} \right]^2}{V_{\mathrm{in}} D^2 T}. \quad (13)$$

$R_{\mathrm{L}} \geq R_{\mathrm{min}}$ is an essential condition for the capacitor energy to reach E_{ref}. Otherwise, it is impossible to maintain the output at the reference level, even if no control cycle is skipped.

Similarly, the range of the load needed to make the system operate in the period-2 bifurcation ($k = 1$, $s = 1$) is as follows:

$$R_{\min}^{\text{period}-2} = \frac{T}{C}\left(\frac{4E_{\text{ref}}}{\Delta E_{\text{in}}} - 1\right), \tag{14}$$

$$R_{\max}^{\text{period}-2} = \frac{T}{C}\left(\frac{4E_{\text{ref}}}{\Delta E_{\text{in}}} + 1\right). \tag{15}$$

When $R_{\text{L}} \in \left[R_{\max}^{\text{period}-2}, R_{\max}^{\text{period}-2}\right]$, the modulation factor M is 0.5 and the system works in period-2 bifurcation.

4 | RELATIONSHIP BETWEEN THE MODULATION FACTOR AND THE VARIABLE LOAD

If the parameters in Figure 1 are set properly, the output energy trajectory with different loads can be obtained as shown in Figure 3.

In Figure 3A, points a-e represent E_{Co} in five consecutive cycles. E_{ref} is the energy reference line. When $E_{\text{Co}} < E_{\text{ref}}$, the system operates in the normal state corresponding to the energy locus from a to e. When $E_{\text{Co}} > E_{\text{ref}}$, the system skips to the next control cycle, corresponding to points e and f. Thus, the modulation factor $M = 0.2$. This system can be stabilized at five different energy stages under this load status and form a period-5 bifurcation.

In Figure 3B, this system shows a periodic behavior with 15 different energy stages and forms a period-15 bifurcation. If the load is reduced, M increases and becomes 0.53 with E_{Co} being stable.

Figure 4 illustrates the bifurcation diagram of the output energy in a PSR fly-back PSM converter. The points below E_{ref} are the energy stages after the normal on/off states. The points at the top are the energy stages after pulse skipping. When the load is smaller than $R_{\min}^{\text{period}-2}$ as the load decreases, the system enters into a multi-cycle steady state, and the number of pulses skipped becomes significantly larger (so does M). Because $\lambda < 1$ in (11), the PSM system in DCM is a closed-loop system, and chaos will not occur in such a system.

5 | MODULATION FACTOR FOR ADAPTIVE CONTROL

The PSR fly-back PSM converter cannot sample the output voltage to control the pulse skipping operation cycle-by-cycle; therefore, it is necessary for the PSM controller to determine the number of cycles skipped s and generate a detective pulse, which takes D_s as the duty cycle, to continue monitoring V_{out}.

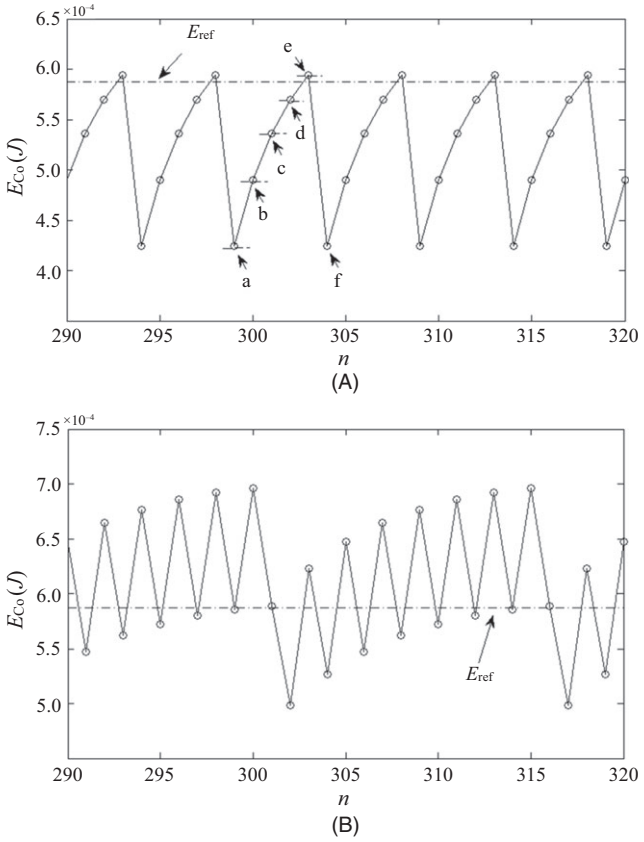

FIGURE 3 Trajectory of the output energy: (A) energy trajectory when $R_{\text{L}} = 6\ \Omega$ and (B) energy trajectory when $R_{\text{L}} = 12\ \Omega$

Here, S_s is set as the state of the system when it skips s cycles continuously (S_0 indicates $s = 0$), and c_n is set as the comparison between the sampled feedback voltage and V_{ref}, as shown below.

$$c_n = \begin{cases} 1 & V_{\text{FB}} < V_{\text{ref}} \\ 0 & V_{\text{FB}} > V_{\text{ref}} \end{cases}. \tag{16}$$

Initially, $c_n = 1$, and the system operates in the state S_0. When $V_{\text{FB}} > V_{\text{ref}}$, as $c_n = 0$ during the nth cycle, the system enters the state S_s ($s > 1$) from the $(n + 1)$th cycle. The operation state S_s is determined by the load status. According to the principle that M changes with load variations, s is set higher as the load gets heavier and vice versa. The load status is determined by i, which is defined as the number of $c = 0$ or $c = 1$ continuously.

The complete adaptive control can be described as follows:

1. If the system detects $c = 0$ continuously for i times in state S_s, it indicates that the load is too light for the current state, and then the number of skipped pulses s is

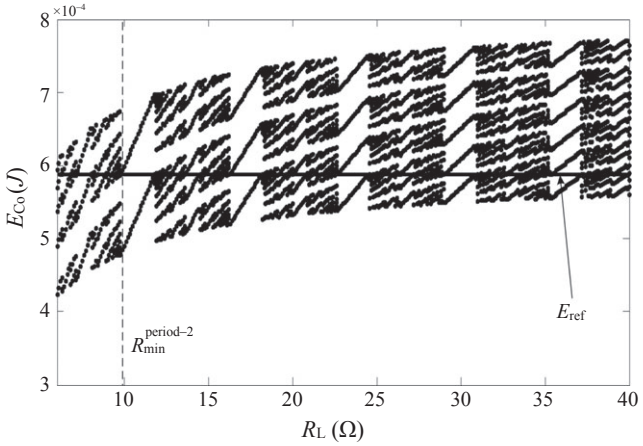

FIGURE 4 Relationship between E_{Co} and R_L

increased to increase M for fitting the current load status.

2. If the system detects $c = 1$ continuously for i times in state S_s, it indicates that the load is too heavy for the current state, and then s is decreased to decrease M for fitting the current load status.
3. If it is still $c = 0$ after the system reaches the maximum cycle skipping state S_{max}, it outputs a no-load signal to shut down parts of the modules to save energy. S_{max} is set as the number of pulses skipped to ensure that the real switch frequency does not enter into the audio range.

D_s is set properly to maintain the same output energy before and after the detective pulses. When the system enters the state S_{s+1} from S_s, the duty cycle of the detective pulses is $D_{s+1} = \alpha D_s$ ($\alpha > 1$) to reduce the energy of the detective pulse and the output ripple.

Apparently, i determines the response speed of the system with the variable load. When $i = 1$, the system response is sensitive but stability becomes worse. In the AC-DC converter, the system can never operates in a single state S_s due to the influence of factors such as V_{in}, self-tuning duty cycle D, frequency jittering, and other external interferences. Then, we set $i = 2$ or 3 to stabilize the output voltage. A state-transition diagram is shown in Figure 5.

This can be realized by the state machine. Especially, in PSM controllers, a state machine that controls the current limit threshold according to load status is usually introduced. When $k \geq s = 1$, the range of the load is:

$$R_{min} < R_L \leq R_{max}^{period-2}. \quad (17)$$

Here, $M \leq 0.5$; the number of sampling/comparing can be reduced to at most 50% of the cycle-by-cycle sampling

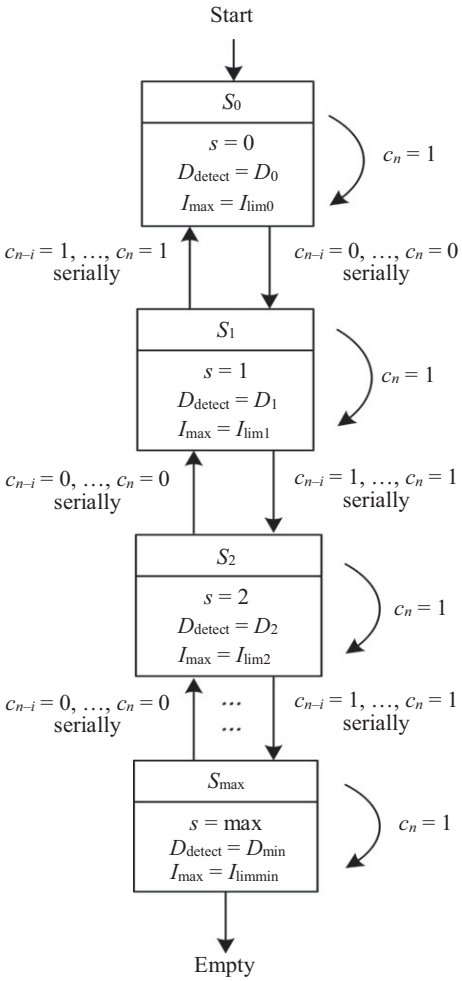

FIGURE 5 State-transition diagram of the strategy

($k = s = 1$). If the sampling/comparing module is in the sleep mode during the skipped pulses, then the output remains the same theoretically. These two modules can save at most 50% of the dissipated power.

As the load gets lighter, $s > k = 1$ after the system is steady, and the load range is

$$R_L \geq R_{max}^{period-2}. \quad (18)$$

Here, $M > 0.5$, and this strategy adaptively controls the number of pulses skipped according to the load variation. The sampling/comparing module saves most of dissipated power compared to that in the case of cycle-by-cycle sampling.

The initial detective pulse duty cycle D_1 and α are important for reducing the output voltage ripple. To eliminate the effect of the sampling pulse on the system, it is necessary to ensure that the output energy remains the same before and after the detective pulses. From (5) and (6), D_1 can be expressed as

$$D_1 = \frac{1}{V_{\text{in}}T}\sqrt{\frac{2Lp(E_{\text{Co}}^{(n+1)} - \lambda E_{\text{Co}}^{(n)})}{\frac{T}{R_{\min}C_{\text{o}}}}}. \tag{19}$$

In practical applications,

$$E_{\text{Co}}^{(n+1)} = E_{\text{Co}}^{(n)} = \beta E_{\text{ref}} \tag{20}$$

where β is a scale factor. The load range is approximately the same between the neighboring states; therefore, α can be estimated by the two initial states S_0 and S_1.

$$\alpha \cong \sqrt{\frac{R_{\min}^{\text{period}-2} - R_{\min}}{R_{\min}}}. \tag{21}$$

The bifurcation diagram with load variations obtained using the M adaptive control strategy is shown in Figure 6.

When the load becomes lighter, the system status becomes S_5 ($s = 5$) from S_1 ($s = 1$). The two energy loci at the bottom of each state show the energy trajectories before and after the detective pulses. We can change D_s properly to maintain the output energy at both ends of the detective pulses.

The EB model of PSM is established for the structure of PSR fly-back converter. According to the system energy bifurcation diagram, the output energy of the PSR fly-back PSM structure may enter the bifurcation state but not the homogeneous state. The proposed strategy can stabilize the output voltage with different loads, and the modulation degree changes with the load.

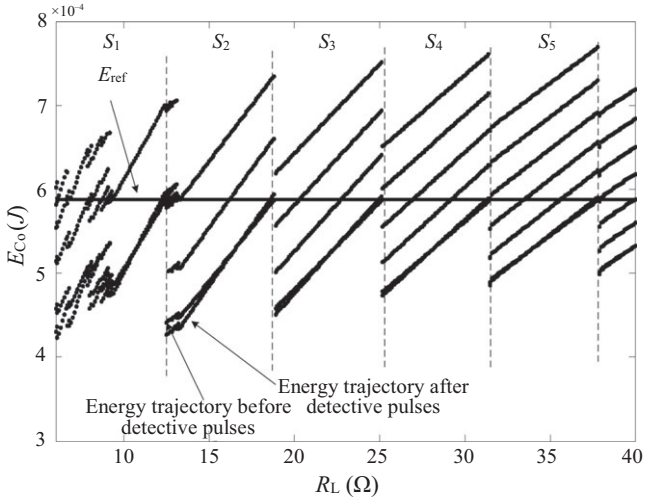

FIGURE 6 Bifurcation diagram of the output energy

6 | SIMULATION ANALYSIS AND DISCUSSION

Figure 7 shows the energy track response for the variable load with the modulation factor adaptive control strategy ($i = 1$, $\alpha = 0.66$, $\beta = 0.9$).

When the load R_{L} changes from 6 Ω to 16 Ω, it can regulate the number of pulses skipped effectively and make the output energy remain close to E_{ref} with minor ripple. Ignoring the influence of the detective pulses, M tracks the ideal value from 0.2 to 0.66. Accordingly, the output energy bifurcation changes from period-5 to period-2 and finally to period-3.

The regulation of the modulation factor by the adaptive control strategy is compared with its ideal value in Figure 8.

In Figure 8A, the dashed line represents the ideal M value and the solid line represents the M regulated by the strategy. For the range of 1 Ω to 1 kΩ, M changes adaptively according to the load variations and follows its ideal value perfectly. Figure 8B shows the modulation factor tolerance for the strategy and the ideal value. Using the proposed method, the tolerance is 20% at maximum and 1.26% on average.

The traditional control strategy uses an error amplifier, which has some disadvantages in terms of noise suppression. The proposed control strategy uses a resistive divider on the bias winding for negative feedback. It samples and compares at a certain moment after the normal switching. The modulation degree is adjusted adaptively according to the load condition.

The power dissipated by the sampler/comparator module of the traditional PSM controller is compared with the M factor adaptive control strategy, as shown in Figure 9.

When $R_{\text{L}} < R_{\min}$, the sampling/comparing frequencies of these two methods are the same, and so are the power dissipations. If $R_{\text{L}} > R_{\min}$, the sampling/comparing

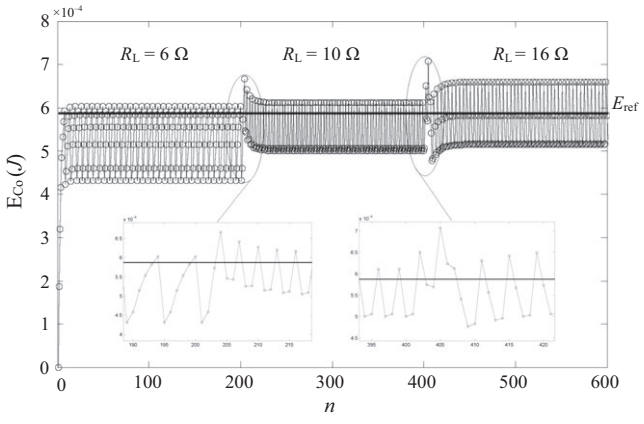

FIGURE 7 E_{Co} adaptive variable with the load changed

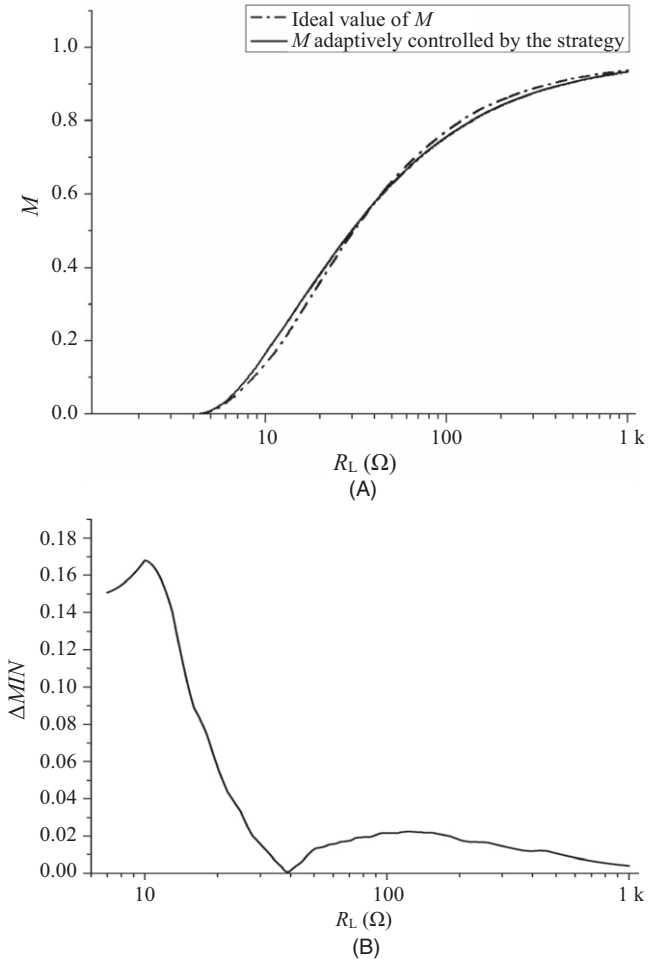

FIGURE 8 Comparison between the adaptive control and the ideal modulation: (A) Comparison with the ideal M and (B) M tolerance corresponding with the ideal value

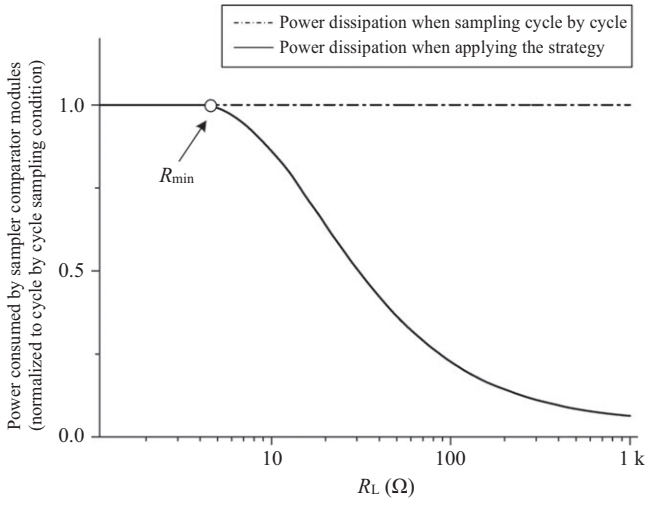

FIGURE 9 Power consumed by sampler modules

operations take place only at the normal states with the M factor adaptive strategy, and the power dissipation of the related modules declines fast and shows a significant

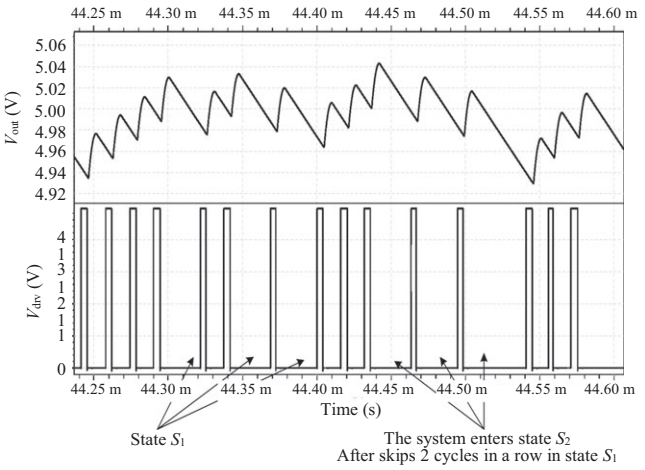

FIGURE 10 Simulation results of the AC-DC output voltage

TABLE 1 Parameters of the AC-DC converter circuit

Parameter	Definition	Value
V_{in}	Input voltage	220 V
V_{ref}	Reference voltage	2 V
R_1	Upper divider resistance	14.88 kΩ
R_2	Lower divider resistance	8.72 kΩ
L_p	Primary magnetizing inductance	1.0945 mH
n_1:n_2:n_3	Turns ratio of transformer	115:6:7
C_o	Output capacitor	47 μF
f	Switch frequency	65 kHz
R_L	Load resistance	6 Ω

superiority under light loads. Within the load range of 1 Ω to 1 kΩ, the related modules can save an average of 87% of the power compared with traditional fly-back PSM controllers.

Using this control strategy on a PSR fly-back structure, a PSM mode AC-DC converter is designed. The simulation result is depicted in Figure 10.

This prototype was designed to convert 220 V AC to 5 V DC, and the parameters are defined in Table 1 ($i = 2$, $\alpha = 1$, $\beta = 1$).

The simulation result shows that M is well modified to fit the load. The output voltage ripple is limited within ±2.5%. Besides, the sampling/comparing frequency is approximately 33% less than that of the traditional PSM controllers. It reduces 33% of the power dissipation in the related modules.

7 | CONCLUSIONS

To overcome the drawbacks of traditional PSM controllers, this paper proposes a PSM control strategy. This

strategy enables PSM controllers to adjust the modulation factor adaptively according to the load status. The energy model based on a PSR fly-back converter in DCM is established, and the stability of its structure is analyzed. Simulation results show that the modulation factor tolerance controlled by this strategy is 1.26% on average corresponding to its ideal value. Compared with traditional fly-back PSM controllers, the power saved in the sampler/comparator modules is 87% on average for a load range of 1 Ω to 1 kΩ. In terms of cost and power dissipation, this strategy controls the modulation factor very well. This is important for the research on cost-efficient and low power consumption converters.

ACKNOWLEDGMENTS

This work was partly supported by the National Scientific Research Foundation of China (No. 61301067), the Shaanxi Provincial Department of Education scientific research project (No. 17JK0690) of China, and the social science planning project of Shaanxi Province (No. 2016R022).

ORCID

Lei Tian http://orcid.org/0000-0002-3574-0450

REFERENCES

1. S.-J. Lee and H. –L. Do, *Boost-integrated two-switch forward AC-DC LED driver with high power factor and Ripple-free output inductor current*, IEEE Trans. Ind. Electron. **64** (2017), no. 7, 5789–5796.
2. S.-H. Lee, W.-J. Cha, and B.-H. Kwon, *High-efficiency soft-switching AC-DC converter with single-power-conversion method*, IEEE Trans. Ind. Electron. **64** (2017), no. 6, 4483–4490.
3. A. Ghosh et al., *Design and implementation of type-II and type-III controller for DC-DC switched-mode boost converter by using K-factor approach and optimisation techniques*, IET Power Electron. **9** (2016), no. 5, 938–950.
4. T.-T. Li, M. Zhang, and M.-J. Pan, *Design and analysis of an optocoupler isolation amplifier with MHz bandwidth*, Acta Electronica Sinica **42** (2014), no. 7, 1398–1402.
5. M. Ferdowsi et al., *Pulse regulation control technique for fly back converter*, IEEE Trans. Power Electron. **20** (2005), no. 4, 798–805.
6. L. L. Xia et al., *Analysis of the soft-start circuit of the high voltage power supply based on PSM technology*, IEEE Trans. Plasma Sci. **42** (2014), no. 4, 1026–1031.
7. H. Li et al., *A miniature high-efficiency fully digital adaptive voltage scaling buck converter*, Int. J. Electron. **102** (2015), no. 9, 1520–1534.
8. J. P. V. S. Cunha, M. Begalli, and M. D. Bellar, *High voltage power supply with high output current and low power consumption for photomultiplier tubes*, IEEE Trans. Nucl. Sci. **59** (2012), no. 2, 281–288.
9. D. Sun et al., *Digital controller for single-phase DCM boost PFC converter with high power factor over wide input voltage and load range*, IEICE Trans. Electron. **E97-C** (2014), no. 4, 377–385.
10. B. N. Singh et al., *Digital implementation of an advanced static compensator for voltage profile improvement, power-factor correction and balancing of unbalanced reactive loads*, Elect. Power Syst. Res. **54** (2000), no. 2, 101–111.
11. L.-Y. Wang, M.-L. Zhao, and X.-B. Wu, *A monolithic high-performance buck converter with enhanced current-mode control and advanced protection circuits*, IEEE Trans. Power Electron. **31** (2016), no. 1, 793–805.
12. M. S. Manoharan, A. Ahmed, and J.-H. Park, *Peak-valley current mode controlled h-bridge inverter with digital slope compensation for cycle-by-cycle current regulation*, J. Elect. Eng. Technol. **10** (2015), no. 5, 1989–2000.
13. Y. Zhang and C. Qu, *Direct power control of a pulse width modulation rectifier using space vector modulation under unbalanced grid voltages*, IEEE Trans. Power Electron. **30** (2015), no. 10, 5892–5901.
14. B. J. Culpepper and H. Suzuki, *Switching DC-to-DC converter with discontinuous pulse skipping and continuous operating mode without external sense resistor*, US Patent 6, 396, 252, filed Dec. 14, 2000, issued May 28, 2002.
15. Y. Wang, P. Li, and S. Lai, *Robust and efficient transistor-level envelope-following analysis of PWM/PFM/PSM DC-DC converters*, IEEE Trans. Comput.-Aided Design Integr. Circuits Syst. **35** (2016), no. 11, 1836–1847.
16. L. George et al., *A 0.04 mm^2 buck-boost DC-DC converter for biomedical implants using adaptive gain and discrete frequency scaling control*, IEEE Trans. Biomed. Circuits Syst. **10** (2016), no. 3, 668–678.
17. S. Zhong et al., *Low-frequency oscillation of continuous conduction mode buck converter with pulse skipped modulation*, Acta Physica Sinica **63** (2014), no. 19, 198401-1–198401-8.
18. Z.-H. Ning, L.-N. He, and Z.-C. Hu, *A high voltage high stability switching-mode controller chip*, J. Zhejiang University **48** (2014), no. 3, 377–383.
19. J. Sun, *Characterization and performance comparison of ripple-based control for voltage regulator modules*, IEEE Trans. Power Electron. **21** (2006), no. 2, 346–353.
20. P. Luo et al., A high energy efficiency PSM/PWM dual-mode for DC-DC converter in portable applications, *Int. Conf. Commun. Circuits and Syst.*, Milpitas, CA, USA, July 23–25, 2009, pp. 702–706.

AUTHOR BIOGRAPHIES

Lei Tian received his Master degree in mobile communication from Xi'an University of Science and Technology in 2006. In 2015, he got his PhD in optoelectronic integrated circuit design (OEIC) from Xidian University. Then he is a post doctor in Northwest University. His research interest includes analog and mixed integrated circuits, photoelectric signal processing, optocoupler, SOC design, infrared communications.

Qinqin Li received his Master degree in circuit and system from Xidian University in 2014. She has been studying for a doctoral degree in Xidian University. Her research interest includes digital and analog mixed integrated circuits, optoelectric processing circuit.

Weiheng Wang received his BS degree in electronic from Xi'an University of Posts and Telecommunication in 2010. He received his Master degree and engineer title in telecom and network from Institut Sup Galilée, Université Paris 13, Villetaneuse, France, in 2014. From 2014, he works for Vente-Privée (Top 1 French e-commerce firm). His research interest includes power electronic design and testing of the integrated optoelectric circuit.