Received: 20 September 2018 | Revised: 21 November 2018 | Accepted: 2 December 2018

DOI: 10.4218/etrij.2018-0523

SPECIAL ISSUE

WILEY ETRI Journal

Evolution of spatial light modulator for high-definition digital holography

Ji Hun Choi[1] | Jae-Eun Pi[1] | Chi-Young Hwang[1] | Jong-Heon Yang[1] | Yong-Hae Kim[1] | Gi Heon Kim[1] | Hee-Ok Kim[1] | Kyunghee Choi[1] | Jinwoong Kim[2] | Chi-Sun Hwang[1]

[1]ICT Materials & Components Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea.

[2]Broadcasting and Media Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea.

Correspondence
Ji Hun Choi, ICT Materials & Components Research Laboratory, Electronics and Telecommunications Research Institute, Daejeon, Rep. of Korea.
Email: hunbaksa@etri.re.kr

Funding Information
This work was supported by "The Cross-Ministry Giga KOREA Project" grant funded by the Korea government (MSIT) (1711073921, Development of Telecommunications Terminal with Digital Holographic Table-top Display).

Since the late 20th century, there has been rapid development in the display industry. Only 30 years ago, we used big cathode ray tube displays with poor resolution, but now most people use televisions or smartphones with very high-quality displays. People now want images that are more realistic, beyond the two-dimensional images that exist on the flat screen, and digital holography—one of the next-generation displays—is expected to meet that need. The most important parameter that determines the performance of a digital hologram is the pixel pitch. The smaller the pixel pitch, the higher the level of hologram implementation possible. In this study, we fabricated the world-smallest 3-μm-pixel-pitch holographic backplane based on the spatial light modulator technology. This panel could display images with a viewing angle of more than 10°. Furthermore, a comparative study was conducted on the fabrication processes and the corresponding holographic results from the large to the small pixel-pitch panels.

KEYWORDS
Digital holography, holographic panel, pixel pitch, spatial light modulator, viewing angle

1 | INTRODUCTION

Display technology has evolved from cathode ray tube displays to flat-panel displays (FPDs) such as thin film transistor-liquid crystal displays (TFT-LCDs), plasma display panels (PDPs), and active matrix organic light-emitting diodes (AMOLEDs) owing to the advent of large-area electronics such as amorphous Si thin-film transistors as the switching and/or driving electronic devices for active matrix addressing. Currently, one of the key aspects of next-generation FPDs is how to provide a realistic image, for which high resolution, high frame rate, and large size panels are being actively pursued. Recently, three-dimensional (3D) displays using the principle of binocular parallax were commercialized, spurred on by the success of the movie Avatar; however, they have not generated much public interest, due to the discomfort and nausea caused by the psychological fatigue when viewing a 3D display.

Holographic displays are known to be one of the ideal 3D displays because they can reconstruct accurate object wavefronts [1]. The analog hologram is a well-known type of hologram, and it provides very natural and realistic 3D images due to its tens-nanometer grain size. However, an analog hologram has some limitations. First, it is difficult and expensive to fabricate and define its very fine patterns. In addition, it only provides static images. On the other hand, digital holography,

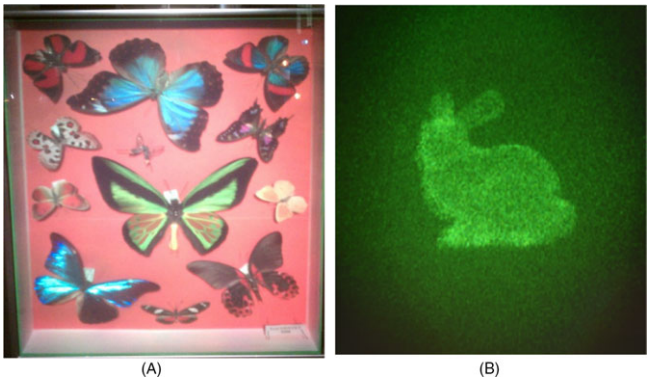

FIGURE 1 Example of two types of hologram: (A) analog hologram image and (B) digital hologram image. Reprinted from Monsterman222 [CC0], from Wikimedia Commons

which needs electrically addressed spatial light modulators (SLM) [2], can generate dynamic images, but the image quality is worse compared to analog hologram because it has a relatively large pixel pitch of tens-micrometer order. Figure 1 shows a comparison of analog hologram and digital hologram images. In digital holograms, the pixel pitch is an important factor in determining the resolution of an image, because a narrower pixel pitch ensures that more information is obtained from a coherent beam spot. Furthermore, it is essential to reduce the pixel pitch because the smaller the pixel pitch, the wider the viewing angle, as shown in Figure 2.

From a practical implementation perspective, many kinds of SLMs have been widely studied and developed, including a digital micro mirror display (DMD), a liquid crystal on silicon (LCoS), and an acoustic optic modulator [3–7]. Among them, LCoS has been widely used as an SLM with a high resolution owing to its compatibility with the well-established complementary metal-oxide semiconductor (CMOS) process technology [4,5]. However, the scalability of an LCoS SLM is limited in size owing to the finite wafer dimensions, which deteriorate the spatial resolution in terms of the real size of the 3D images. The TFT technology fabricated on a glass substrate is considered as a good alternative to overcome the aforementioned problem.

In this study, we fabricated SLM on glass (SLMoG) holographic backplanes with various pixel pitches ranging from 20 μm to 3 μm, in order to figure out how the pixel pitch actually affects the resolution and viewing angle of the images. The changes in design rule and fabrication processes due to the reduction of the pixel pitch are explained, and the corresponding reconstructed holographic images are demonstrated.

2 | EXPERIMENTAL PROCEDURE

2.1 | Structure of SLMoG panel

A schematic diagram of the cross-section of a reflective mode SLM panel on glass substrate is shown in Figure 3.

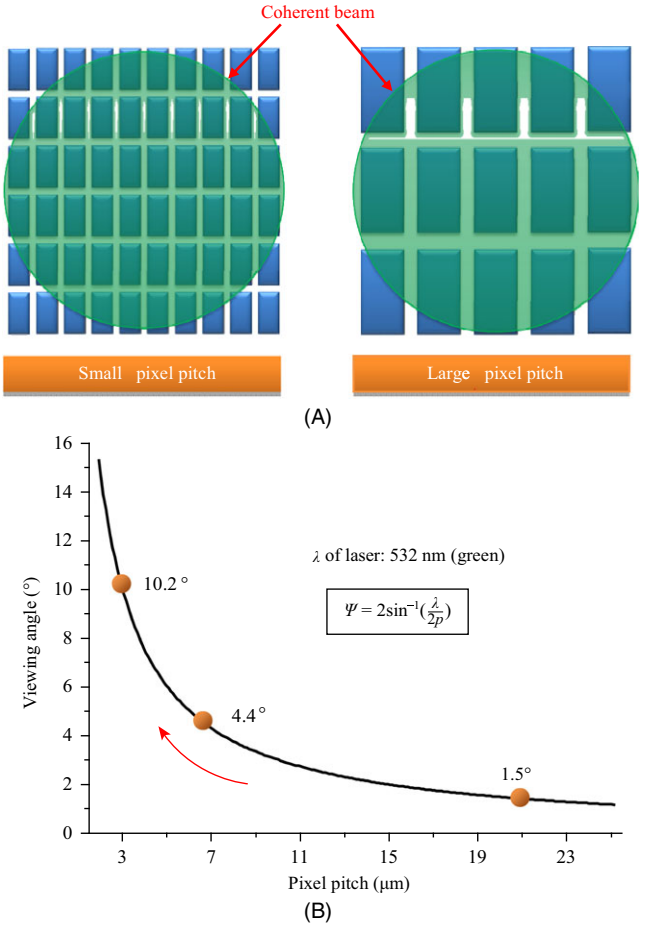

FIGURE 2 Correlation between pixel pitch and (A) resolution, (B) viewing angle of holographic image. λ is the wavelength of the incident laser to the panel. p is the pixel pitch of the panel

The holographic backplane for the active matrix addressing of the SLM panel was integrated with the oxide thin-film transistor (TFT) array. This system was processed on a glass substrate, which is suitable for large-scale display applications. The structure consisted of mainly two parts. First, the electrical operation part, including the switching TFT, storage capacitor, and reflector layer, was fabricated on the lower side of the panel. The switching TFT adopted an inverted-staggered structure with a back-channel etch (BCE) scheme. Here, it is possible to minimize the channel length up to the limitation of the lithography resolution, and therefore the integration density, such as the pixel resolution, can be maximized. On the other hand, the etch-stopper scheme will have a longer channel length owing to the overlap consideration between the etch stop layer and source/drain (S/D) layer [8]. The optical operation part above the reflector was placed at the upper level of the panel. In order to achieve a sufficient phase shift using the applied voltage with a small fringe field effect, a nematic liquid crystal was used and aligned in the cell using a pair of parallel rubbed polyimide alignment layers. The cell gap of 2.5 μm was controlled using a 2.5-μm-thick ball spacer.

Liquid crystal was introduced into the cell using a vacuum injection method. Reflectors were employed for reflective mode operation, which has the advantage of phase modulation of up to 2π as the incident light enters the panel through the liquid crystal and is reflected off the reflective layer, resulting in phase modulation twice. Furthermore, considering that it is difficult to obtain a sufficient aperture ratio as the pixel pitch decreases, the use of the reflective mode display is imperative. In this study, we fabricated three kinds of panels with pixel pitches of 20 μm, 7 μm, and 3 μm. The pixel structure shown in Figure 3 was applied to all the panels regardless of the pixel pitch.

2.2 | Fabrication of SLMoG panel

For a 20-μm-pixel-pitch holographic backplane, the inverted-staggered BCE configuration with a channel length of 6 μm was adopted for the switching TFT, as depicted in Figure 4. For the gate, S/D, and reflector electrodes, 150-nm-thick DC-sputtered Molybdenum (Mo) was used. They were patterned using a wet chemical solution of a strong acid mixture comprised of phosphoric acid, acetic acid, and nitric acid (PAN). As the gate dielectric layer, 200-nm-thick silicon dioxide (SiO_2), which was grown by plasma-enhanced chemical vapor deposition (PECVD) method at 380°C, was used. For the active layer, we used a 40-nm-thick layer of aluminum-doped indium-tin-zinc-oxide (in a ratio of about 4:4:2, respectively) deposited by RF magnetron sputtering of the sintered single metal oxide target under 0.1 Pa process pressure with an oxygen partial pressure of 40% of the $O_2/(Ar + O_2)$ mixture. The oxalic acid-based wet chemical solution at room temperature was used to define the active pattern by photolithography. For the passivation layer, 100 nm-thick SiO_2 was grown by using the PECVD method at 300°C following N_2O plasma treatment. After the fabrication of the switching TFT, the thermal-curable photosensitive polyacrylate polymer (TR 8887-SA7 from Dongjin Semichem Co., Ltd.) with a thickness of 2.3 μm was used to planarize the TFT surface so that the subsequent reflector layer could be deposited flat. The via hole was opened by the exposure and development process, because this planarization polymer could be patterned like a normal positive photoresist. A 2.38% NMD3-diluted solution was used as the developer. After backplane fabrication, the panel, including the switching TFTs, was annealed at 200°C for 2 hours under vacuum condition. The top-view of the optical microscope images of the 20-μm-pixel-pitch panel after S/D patterning and reflector patterning are shown in Figure 5A,D.

The process methods were applied differently depending on the pixel pitch of the panel although the overall structure of the switching TFT was almost retained. The critical dimension (CD) of the panel and the channel length of the switching TFT of the 7-μm-pixel-pitch panel were 1 μm and 2 μm, respectively, whereas those of the 3-μm-pixel-pitch panel were 0.5 μm and 1 μm, respectively. Therefore, the anisotropic dry etch process was employed to define very fine patterns and narrow spaces. The Mo layers were etched using the mixture of chlorine and oxygen gases at 10 mTorr process pressure. Unfortunately, Cl_2, the etching gas of S/D Mo, also affected the metal-oxide channel material during the dry etching process, resulting in physical damage to the back-channel surface. Therefore, the deposition thickness of the channel material was increased to 70 nm, and the broken metal-oxygen bond was restored by introducing an effective wet treatment process to remove the damage. In addition, as the pixel pitch of the panel and the channel length of the switching TFT decreased in the horizontal direction, the thickness of the gate insulator was decreased to 100 nm in the vertical direction to maintain device controllability. In this case, it was difficult to reduce the gate layer thickness to prevent the increase in sheet resistance of the signal lines. In this process, the gate insulator thin film, which was thinner than the lower gate metal, was broken by the steep slope near the gate pattern edge. Previously, this critical problem had been solved smoothly by forming a triangular-shape silicon nitride (Si_3N_4) spacer at the gate pattern side prior to the

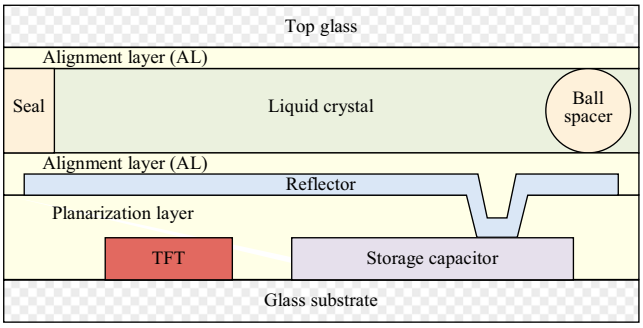

FIGURE 3 A schematic diagram of pixel cross-section view of reflective-mode SLMoG panel

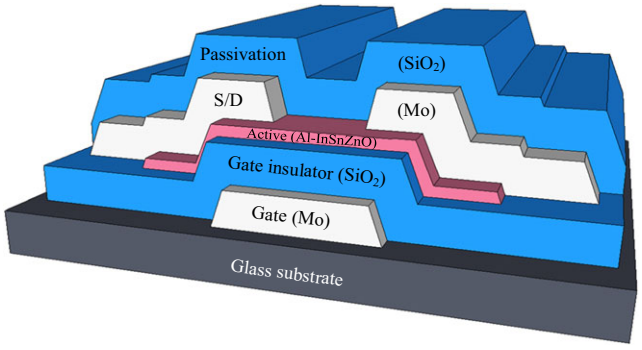

FIGURE 4 A schematic diagram of BCE type switching oxide thin-film transistor

SiO_2 gate insulator deposition process [9]. Furthermore, the thickness of the planarization layer was scaled down to about 0.6 μm in order to define very small via hole patterns as the pixel pitch of the panel decreased, and the process for the metal contact via hole through the planarization layer was also changed from the wet development process to the dry etching process. In order to define sub-micrometer-sized via holes, a mixture of carbon fluoride and oxygen in the ratio 1:1 was used at a process pressure of 5 mTorr. The revised via hole pattern had a diameter of <0.6 μm and a very steep slope compared to that fabricated through the wet-process. The fine structures were measured by using a scanning electron microscope (SEM). Figure 6 shows the difference in pattern shapes due to such via hole process variations. Incidentally, Mo with a high linearity covered the conventional smooth via-hole inclination, as shown in Figure 6B, but a problem such as breakage of the reflector metal occurred in the dry-etched via hole having a narrow diameter and steep-slope shape. TiW with improved step coverage was applied to the reflector metal and the S/D-reflector metal contact was achieved successfully. The top-view of the optical microscope images of the resulting 7 μm-pixel-pitch panel after S/D patterning and reflector patterning are shown in Figure 5B and E, respectively, whereas those of the 3 μm-pixel-pitch panel are depicted in Figure 5C and F, respectively.

In particular, the main change due to the decrease in pixel pitch in the fabrication of holographic panels is the variation in the exposure method in the photolithography process. Both the pixel part and the signal line part of the 20-μm-pixel-pitch panel was developed by using a contact aligner exposure system because the CD was sufficiently large (3 μm), as shown in Figure 7A. However, since the line width/space and the pixel pitch were considerably reduced in the 7-μm-pixel-pitch panel, the backplane was formed by using a mix-and-match process. The signal line part was developed by using a projection aligner and the pixel part was developed by using an i-line stepper equipment (Nikon NSR2205i12D), as shown in Figure 7B. The overlap margin between the patterns developed by the projection aligner and stepper was precisely controlled under 0.5 μm. For the 3-μm-pixel-pitch panel fabrication, the overall mix-and-match process was retained, and the detailed exposure and alignment conditions were optimized for smaller CD implementation. Figure 8 shows the real images of the fabricated holographic panels with various pixel pitches, namely 20 μm, 7 μm, and 3 μm. The images show the ratio of the actual panel size. The panel specifications for various pixel pitches are summarized in Table 1.

3 | RESULT AND DISCUSSION

3.1 | Electrical characteristics of switching transistors

For stable panel operation, a large on/off ratio and low subthreshold slope (*SS*) of the switching device should be

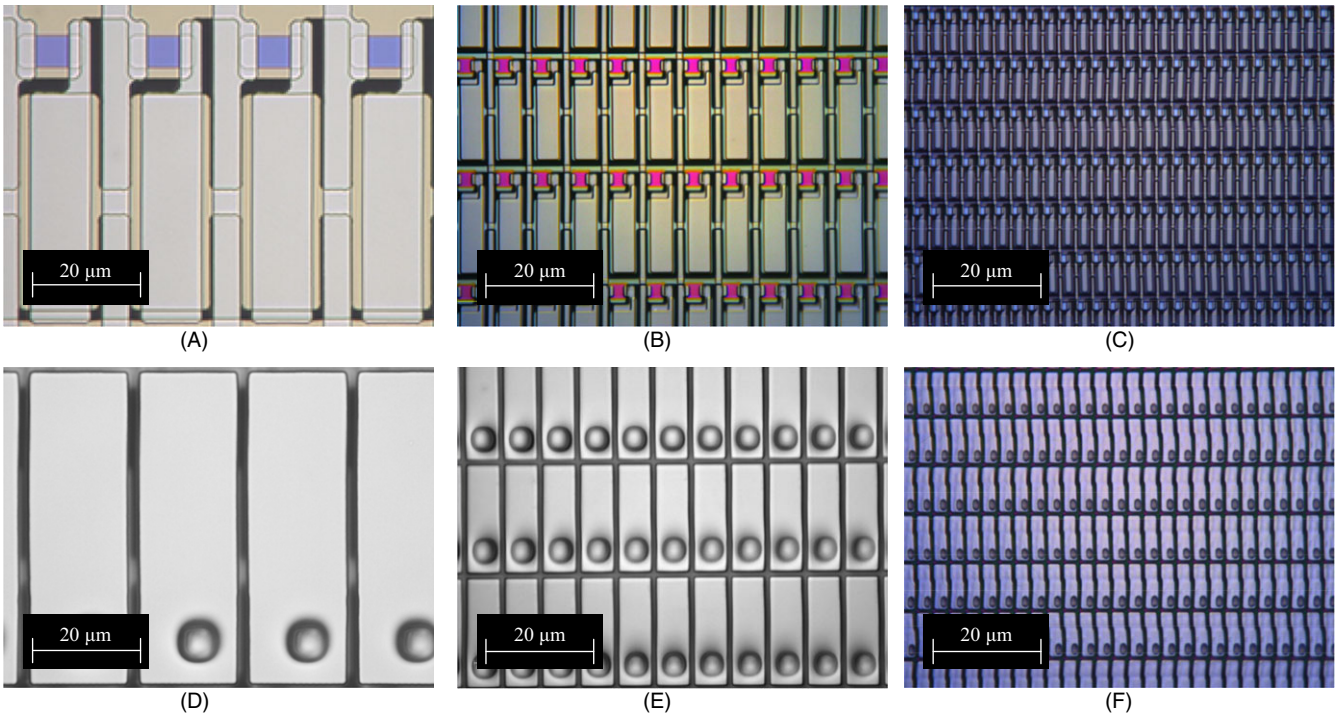

FIGURE 5 Optical microscope images at the same scale after (A), (B), (C) S/D patterning and (D), (E), (F) electrical operation part fabrication for various pixel-pitch panels. (A), (D) were for 20-μm-pixel-pitch panel. (B), (E) were for 7-μm-pixel-pitch panel. (C), (F) were for 3-μm-pixel-pitch panel. Approximately 4 pixels, 33 pixels, and 178 pixels are shown in each image in sequence as the pixel pitch decrease

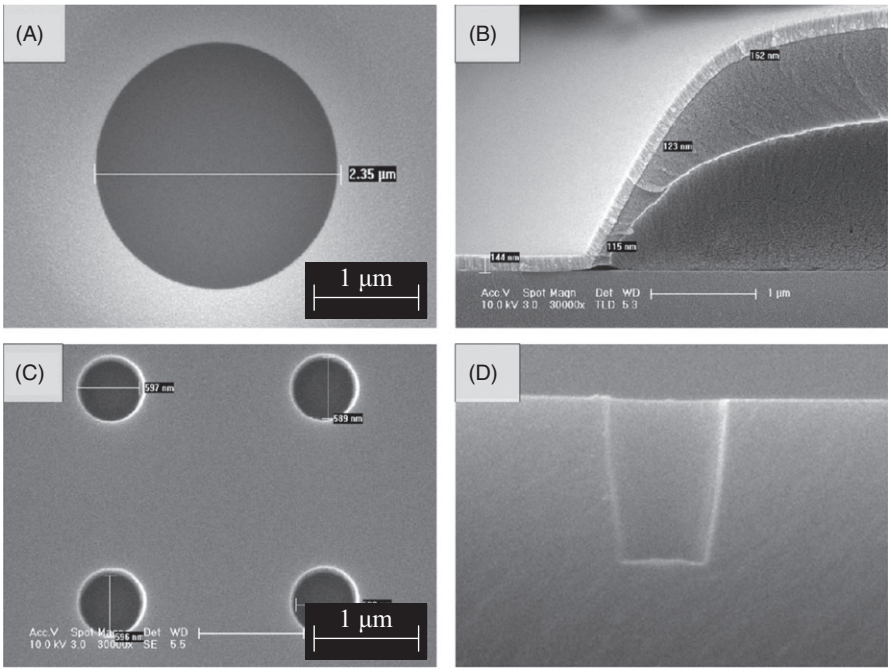

FIGURE 6 The SEM images of the via hole patterns. (A) Top view and (B) cross-section view images of the wet-processed via hole with over 2 μm diameter. (C) Top view and (D) cross-section view images of the dry-etched via hole with a diameter of under 0.6 μm

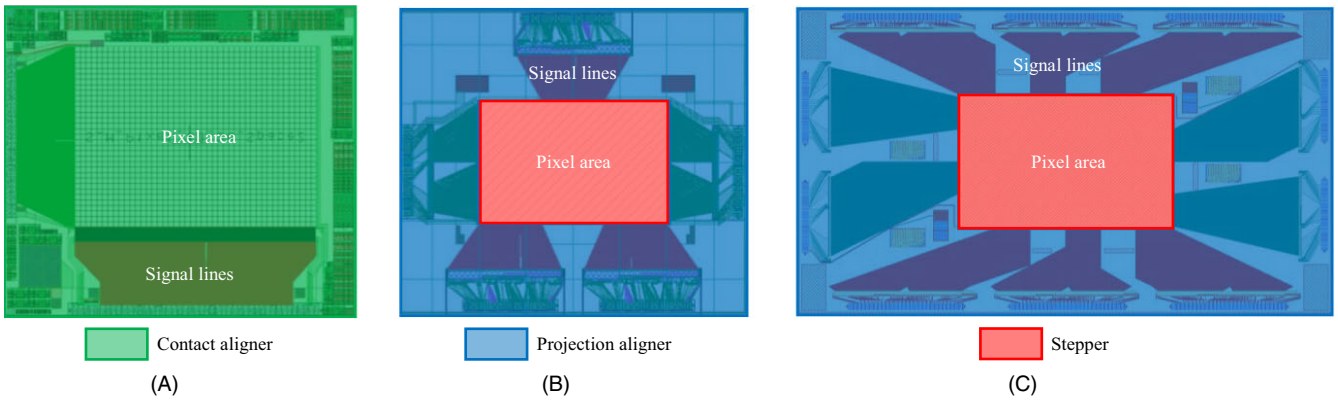

FIGURE 7 Applied exposure methods for various pixel-pitch panels. (A) 20-μm-pixel-pitch panel. Only contact aligner tool was used for photoresist patterning. (B) and (C) 7-μm-pixel-pitch panel and 3-μm-pixel-pitch panel, respectively. Inner pixel part was patterned by stepper tool, and outer signal lines were patterned by projection aligner tool

ensured, and a near-zero turn-on voltage (V_{on}) must be supplied. At the same time, an on-state current of several tens of μA must be supplied. The channel length of the switching transistors decreased from 6 μm to 1 μm with changes in the pixel pitch of the display panel; however, stable switching performance was maintained without degradation of the off-state leakage or *SS*., as shown in Figure 9.

3.2 | Reconstructed holographic images

We set up the holographic display system, as shown in Figure 10A. For the light source, a green laser with a wavelength of 532 nm was used. When the light was illuminated on the SLMoG through optical components such as mirror, filter, and beam expander, diffraction occurred at the panel plane according to the input phase-only computer-generated hologram (CGH) pattern, and an image was formed at a specific focal depth away from the panel on the optical rail path. The driving module of the SLMoG is presented in Figure 10B.

On the basis of the optical setup, we verified the performance of the fabricated display panels by reconstructing CGHs having two different focal distances. The source images of the letters "ET" and "RI" were used for the CGHs generations based on the iterative Fourier transform algorithm (IFTA). Figure 11A,B shows the reconstructed images from the 20-μm-pixel-pitch panel, and Figure 11C,D shows the reconstructed images from the 7-μm-pixel-pitch panel. Figure 11E,F shows the holographic reconstructions using the 3-μm-pixel-pitch panel. For the three cases, we could observe differently focused images at two intended focal distances. Although the reconstruction conditions are slightly different, we can see a clear improvement in the image quality in

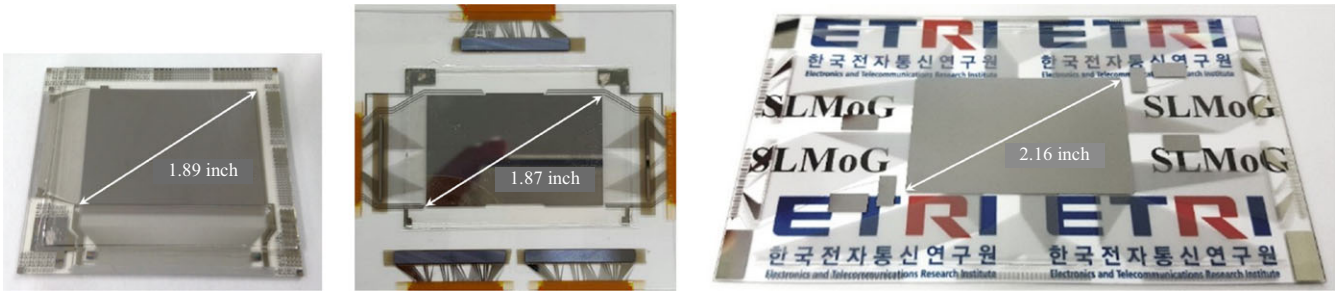

FIGURE 8 The real images of the fabricated holographic panels. (A) 20-μm-pixel-pitch panel with 1.89-inch diagonal size. (B) 7-μm-pixel-pitch panel with 1.87-inch diagonal size. (C) 3-μm-pixel-pitch panel with 2.16-inch diagonal size

TABLE 1 The summary of panel specifications for various pixel pitches

	1st SLMoG	2nd SLMoG	3rd SLMoG
Pixel pitch	20 μm (H) × 60 μm (V)	7 μm (H) × 21 μm (V)	3 μm (H) × 9 μm (V)
Panel size (diagonal of display)	1.89 inch	1.87 inch	2.16 inch
Resolution (mono)	1920 (H) × 480 (V)	5760 (H) × 1080 (V)	15 600 (H) × 3200 (V)
CD	3 μm	1 μm	0.5 μm
Switching TFT channel size	6 μm (H) × 6 μm (V)	2 μm (H) × 2 μm (V)	1 μm (H) × 1 μm (V)
Lithography tool	Contact aligner	Stepper + Projection aligner	Stepper + Projection aligner

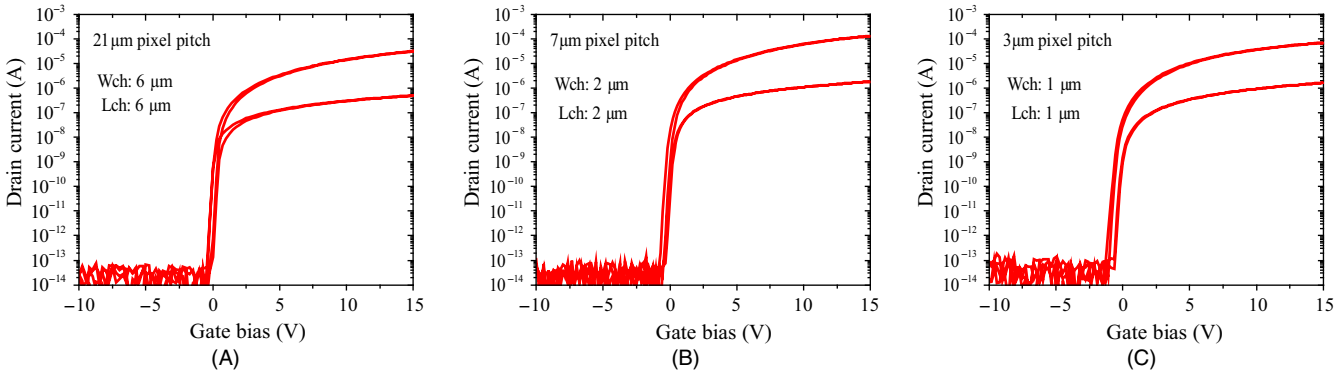

FIGURE 9 The device characteristics of the switching TFTs for the (A) 20 μm-pixel-pitch panel, (B) 7 μm-pixel-pitch panel, and (C) 3 μm-pixel-pitch panel. All the devices show near-zero turn-on voltage and very low off-leakage current

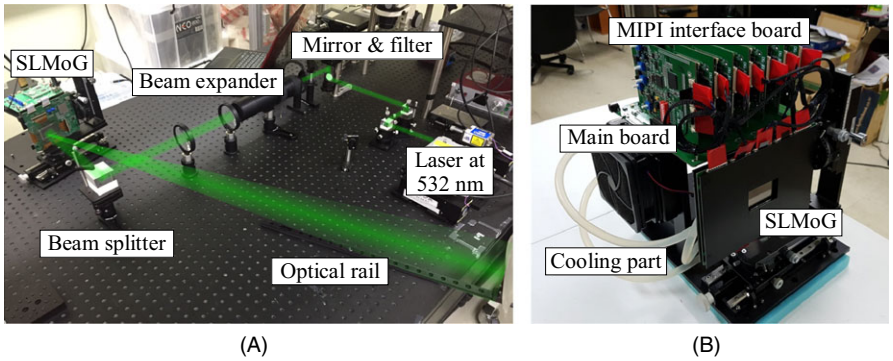

FIGURE 10 The holographic display system. (A) Optical setup for the reconstruction of computer-generated holograms using the fabricated SLMoG. (B) SLMoG set installed in driving stage

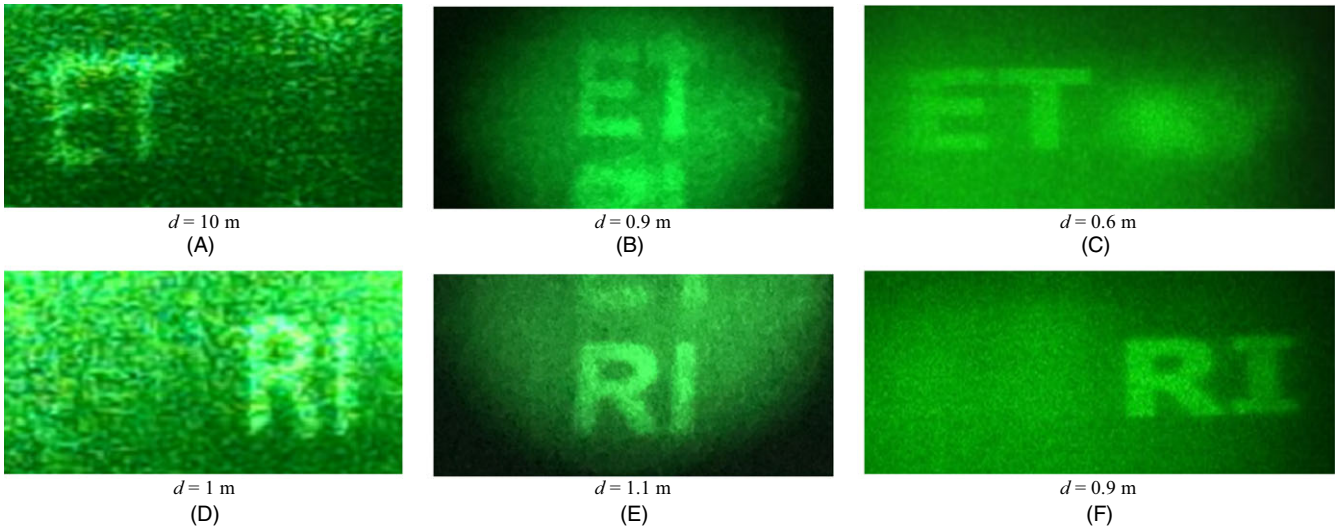

FIGURE 11 The reconstructed digital hologram images with different focal depths for the letters "ET" and "RI". (A) "ET" at 10 m, (B) "RI" at 1 m from the 20-μm-pixel-pitch panel. (C) "ET" at 0.9 m, (D) RI at 1.1 m from the 7-μm-pixel-pitch panel. (C) "ET" at 0.6 m, (D) RI at 0.9 m from the 3-μm-pixel-pitch panel

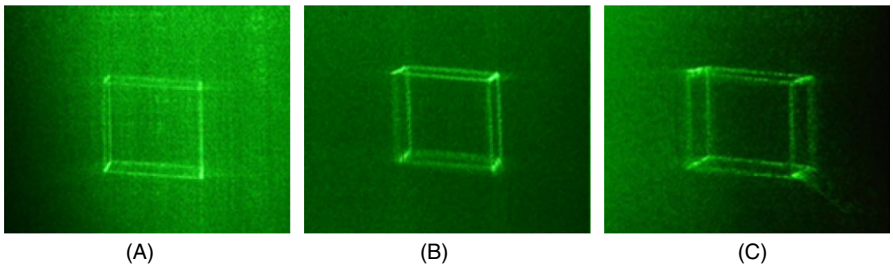

FIGURE 12 The change in hexahedron-shape holographic image according to the viewing angle. (A) Left-side view. (B) Front view. (C) Right-side view

accordance with the evolution of our SLMoG system. For the images from the 20-μm-pixel-pitch panel, it was hard to distinguish the letters due to noise. In addition, the boundaries of the letters were not clear because the resolution of the panel was low. On the other hand, in the images from the 3-μm-pixel-pitch panel, the desired letters were clearly expressed for each focal distance. This can be attributed to the notable progress in the pixel pitch and resolution of the panel. In addition, it was possible to easily demonstrate the effect of viewing angle using the 3-μm-pixel-pitch panel without any additional optical component. This is because the maximum horizontal diffraction angle that can be supported by the panel is approximately 10° for 532 nm light. For experimental validation, the CGHs generated from the three-dimensional hexahedron point cloud object were observed from three different perspectives. As shown in Figure 12, the three distinct perspectives result in different images, from which the effect of viewing angle can be confirmed. The point cloud object, whose horizontal and longitudinal lengths are around 1 cm and 6 cm, respectively, consists of 1,212 point light sources. For our phase-only CGH, the phase information was selected from the complex field on the CGH plane, which was obtained by the superposition of spherical waves radiated from point sources.

Note that background noise components are mainly caused by the incomplete compensation of nonideal optical responses, such as the nonlinear phase modulation for input gray level and the spatial phase nonuniformity [10–12]. The desired linear phase modulation characteristic can be obtained by the sophisticated tuning of the input voltage values with respect to the input gray levels. The spatial phase nonuniformity can be reduced by imposing a compensating spatial phase profile that is appropriately tailored for each specific display panel. We expect that the image quality could be further improved by compensating those degrading factors.

4 | CONCLUSION

In this paper, we presented the fabrication methods, device performance, and holographic results of a series of spatial light modulators with different pixel pitches—20 μm, 7 μm, and 3 μm. The change in the process according to the reduction in the pixel pitch is expressed in detail. In the process of high-resolution holographic backplanes fabrication, a mix-and-match exposure system with stepper tool was introduced to obtain very fine patterns. The dry etch

process was also employed to define narrow lines and spaces. In particular, we successfully fabricated a 3-μm-pixel-pitch panel, which is the smallest pixel pitch SLMoG for digital hologram in the world. The experimental results showed that holographic images could be clearly defined as the pixel pitch of the panel decreased. Furthermore, we demonstrated that a three-dimensional image changes according to the viewing angle based on the high-resolution SLMoG.

ACKNOWLEDGMENTS

The holographic panels in this work were fabricated by using the facilities of Convergence Components Technology Center (CCTC) at ETRI.

ORCID

Ji Hun Choi https://orcid.org/0000-0002-4857-4260

REFERENCES

1. J. Hahn et al., *Wide viewing angle dynamic holographic stereogram with a curved array of spatial light modulators*, Opt. Express **16** (2008), 12372–12386.
2. K. Machida et al., Three-dimensional image reconstruction with a wide viewing-zone-angle using a GMR-based hologram, in *Proc. Digit. Holography Three-Dimensional Image*, Kohala Coast, HI, USA, Apr. 21–25, 2013, DTh2A.5:1– DTh2A.5:5.
3. D. Dudley, W. M. Duncan, J. Slaughter, *Emerging digital micromirror device (DMD) applications*, Proc. SPIE **4985** (2003), 14–25.
4. W. P. Bleha, L. A. Lei, *Advances in Liquid Crystal on Silicon (LCoS) Spatial Light Modulator Technology*, Proc. SPIE **8736** (2013), 87360A:1–87360A:8.
5. S. Reichelt, *Spatially resolved phase-response calibration of liquid-crystal-based spatial light modulators*, Appl. Opt. **52** (2013), 2610–2618.
6. D. E. Smalley et al., *Anisotropic leaky-mode modulator for holographic video displays*, Nature **498** (2013), 313–318.
7. R. Stahl et al., *Modular sub-wavelength diffractive light modulator for high-definition holographic displays*, J. Phys. **415** (2013), 012057.
8. J. H. Choi et al., *InZnO/AlSnZnInO bilayer oxide thin-film transistors with high mobility and high uniformity*, IEEE Electron Device Lett. **37** (2016), 1295–1298.
9. J. H. Choi et al., *1-μm short-channel oxide thin-film transistors with triangular gate spacer*, IEEE Electron Device Lett. **38** (2017), 1398–1400.
10. X. Xun, R. W. Cohn, *Phase calibration of spatially nonuniform spatial light modulators*, Appl. Opt. **43** (2004), 6400–6406.
11. Z. Zhang et al., *Diffraction based phase compensation method for phase-only liquid crystal on silicon devices in operation*, Appl. Opt. **51** (2012), 3837–3846.
12. V. Lopez et al., *Non-uniform spatial response of the LCoS spatial light modulator*, Opt. Commun. **366** (2016), 419–424.

AUTHOR BIOGRAPHIES

Ji Hun Choi received his BS and MS degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Rep. of Korea, in 2012 and 2014, respectively. Since 2014, he has been with ETRI as a member of the research engineering staff. He has worked on high-performance short channel oxide thin-film transistors with high mobility based on the double channel scheme. His current research interests include short channel oxide TFTs and their application to high-resolution digital holography.

Jae-Eun Pi received his BS and MS degrees in electronic engineering from Konkuk University, Seoul, Rep. of Korea, in 2009 and 2011, respectively. In 2011, he joined the Smart I/O Control Device Research Section of ETRI. His main research interests include transparent and flexible electronics and the design of driving circuits for flat-panel and digital holographic displays.

Chi-Young Hwang received his BS and MS degrees in electrical engineering from Seoul National University, Rep. of Korea, in 2010 and 2012, respectively. He joined ETRI in 2012 as a member of the engineering staff. His current research interests include digital holography and its applications.

Jong-Heon Yang received his BS degree in electrical engineering from the Korea Advanced Institute of Science And Technology, Daejeon, Rep. of Korea, in 2000, and his MS degree in electronic engineering from Pohang University of Science and Technology, Rep. of Korea, in 2002. He is currently a senior engineer with the Convergence Technology Research Division of ETRI.

Yong-Hae Kim received his BS and PhD in physics from the Korea Advanced Institute of Science and Technology (KAIST), in 1993 and 1997, respectively. From 1997 to 2000, he worked with SK Hynix Semiconductor Inc., and developed the 0.13 μm DRAM technology. He joined ETRI in 2000, and has been involved in the development of flexible display technologies, such as low temperature poly-Si TFT on plastic substrates and active matrix OLED. His research interests include digital paper, application of meta-materials, and wireless power transmission.

Gi Heon Kim received his BS and MS degrees from Kyungpook National University, Daegu, Rep. of Korea, in 1991 and 1993, respectively. He received the PhD degree in chemical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2000. From 1993 to 1995, he was a researcher at LG Chem. Research Park. From 2000 to 2001, his work focused on liquid crystal display at Samsung Electronics Co., Ltd. Since joining ETRI in 2001, his research interests have included organic materials for electronics and plastic-based displays.

Hee-Ok Kim received her BS degree from Chungnam University in 2009. She joined ETRI in 2009, and since then she has been engaged in the research and development of oxide display devices and their holographic applications, especially on the sputtering system and in measurements.

Kyunghee Choi received her BS degree from Kyungpook National University in 2004. She earned her MS degree in applied physics from Yonsei University in 2007 and worked at Samsung Electronics until 2010. She obtained her PhD from Yonsei University in 2016. Currently, she works at ETRI as a senior researcher. Her research interests include oxide thin-films and van der Waals nanosheet-based electronics.

Jinwoong Kim received his BS and MS degrees in electronics engineering from Seoul National University, Seoul, Rep. of Korea, in 1981 and 1983, respectively. He received his PhD degree in electrical engineering from Texas A&M University, College Station, TX, USA, in 1993. He has been working in ETRI, Daejeon, Rep. of Korea since 1983, leading many projects in the telecommunications and digital broadcasting areas.

Chi-Sun Hwang received his BS degree from Seoul National University, Rep. of Korea, in 1991 and his PhD degree from the Korea Advanced Institute of Science and Technology, Daejeon, Rep. of Korea, in 1996, both in physics. From 1996 to 2000, he worked on the development of DRAM devices with 0.18 μm technology at Hyundai Semiconductor Inc., Incheon, Rep. of Korea. In 2000, he joined ETRI. Since then, his research has focused on display technology based on active matrix FPDs using TFTs, especially oxide TFTs. His recent research interests include environment adaptive displays, digital holography, and novel switching devices.