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Si-core/SiGe-shell channel nanowire FET for sub-10-nm logic technology in the THz regime

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The *p*-type nanowire field-effect transistor (FET) with a SiGe shell channel on a Si core is optimally designed and characterized using in-depth technology computer-aided design (TCAD) with quantum models for sub-10-nm advanced logic technology. SiGe is adopted as the material for the ultrathin shell channel owing to its two primary merits of high hole mobility and strong Si compatibility. The SiGe shell can effectively confine the hole because of the large valence-band offset (VBO) between the Si core and the SiGe channel arranged in the radial direction. The proposed device is optimized in terms of the Ge shell channel thickness, Ge fraction in the SiGe channel, and the channel length (L_g) by examining a set of primary DC and AC parameters. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) of the proposed device were determined to be 440.0 and 753.9 GHz when L_g is 5 nm, respectively, with an intrinsic delay time (τ) of 3.14 ps. The proposed SiGe-shell channel *p*-type nanowire FET has demonstrated a strong potential for low-power and high-speed applications in 10-nm-and-beyond complementary metal-oxide-semiconductor (CMOS) technology.

KEYWORDS
CMOS technology, high hole mobility, low-power high-speed operation, nanowire FET, SiGe shell channel, sub-10-nm logic technology, valence-band offset

1 | INTRODUCTION

For several decades, much effort has been focused on the investigation of continuous device scaling. Recently, reliability issues with respect to short-channel effects (SCEs) have been encountered when targeting 10-nm-and-beyond logic technologies. Advanced logic devices with extremely small volumes are required to achieve not only low-power (LP) consumption but also high-speed performance capabilities [1]. In particular, the demand for LP operation is higher than ever, and it is notable that the drive voltages (V_{DD}'s) for LP and high-performance (HP) tracks have remained unchanged since 2013, as can be confirmed by the most recent international technology roadmap for semiconductors (ITRS) [2]. Various emerging research devices (ERDs) with novel structures have been proposed to enhance gate controllability over the channel and to suppress the SCEs [3–8]. To achieve sub-10-nm nodes, it is expected that emerging research materials (ERMs) should be developed in parallel with device scaling and ERDs [9].

In designing Si-CMOS digital circuits, *p*-type metal-oxide-semiconductor field-effect transistors (PMOSFETs) require larger device widths compared with *n*-type MOSFETs (NMOSFETs) to compensate for the lower hole mobility

values compared to that of an electron. Although NMOSFETs have been widely researched, there has been relatively limited research on PMOSFETs due to their lower hole mobility and area efficiency. A strong candidate that has the highest hole mobility material among semiconductor materials is Ge [10]. The large difference between the bandgap energy values (E_g) of Si (1.12 eV) and Ge (0.66 eV) of 0.46 eV is mostly projected to the valence-band offset (VBO) because the difference between their electron affinity values (χ) is only 0.1 eV [11,12]. Thereby, the mobile holes are effectively confined in the ultrathin Ge channel due to the constructed hole quantum well (QW). Using the large VBO, a Ge-core/Si-shell nanowire FET has been proposed with the aim of achieving high hole mobility and current drive using quasi one-dimensional (1D) transport in the Ge hole gas system [13,14]. However, even with these benefits, there are some limitations in scaling the Ge area using the structure, which induces stronger volume inversion resulting in a drive current reduction [15]. In addition, the Si shell develops a parasitic capacitance that limits high-speed operation. For these reasons, we propose a device that has the advantages of both scalability and device performance.

In this work, Ge is introduced as the shell channel material for a *p*-type nanowire FET due to its high hole mobility and strong Si compatibility [16,17]. An extremely thin SiGe channel is constructed on a Si nanowire core, in which the channel region is composed of a coaxial SiGe shell to achieve higher current drivability and higher gate controllability over the highly restricted channel region. In this study, a *p*-type nanowire FET with a Si-core/SiGe-shell channel heterostructure is proposed and optimally designed based on quantitative analyses. Compared with a previous study [18], a quantum-mechanical model has been newly equipped for achieving higher accuracy. Moreover, the parameters related to the carriers and energy bands were carefully prepared to more precisely design the *p*-type nanowire MOSFET. The dependence of device performance on Ge fraction in the shell channel was closely investigated, in comparison with the different types of nanowire MOSFET in the extremely scaled L_g regime. Finally, the high-frequency operation characteristics were quantitatively studied to evaluate the potential in both analog and digital applications.

2 | SIMULATION APPROACH AND DEVICE STRUCTURE

In this numerical simulation study, various approaches have been made. To closely reflect the depth of the hole in the QW at the $Si_{1-x}Ge_x$ shell channel, the values of $E_g(x)$ and $\chi(x)$ are adopted from the literature [19]. These data were then implemented into the simulation system. For greater accuracy and reliability of the simulation results, multiple models were activated simultaneously. These included field-dependent and concentration-dependent mobility models, band-to-band tunneling model, bandgap narrowing model, the Fermi-Dirac statistics model, and quantum-mechanical models [20]. To avoid a shortage of models that cannot be applied to three-dimensional (3D) simulations and the resulting inaccuracy, a rectangular structure was first constructed and then rotated to create a nanowire device structure with perfect cylindrical symmetry to perform a two-dimensional (2D) simulation that incorporates a larger number of accurate models [21].

Figure 1A illustrates a perspective view of the proposed *p*-type nanowire FET with a SiGe shell channel in addition to the names of the functional regions and the design variables. The total radius includes the Si-core radius (r) and SiGe shell thickness (t), and it is set to 10 nm to realize a small footprint. L_g is the gate length. Figure 1B shows the energy-band diagram across the nanowire at the channel center and the hole-current density contour when the device is fully turned on. The large VBO between the Si core and SiGe shell can confine and accumulate mobile holes in the SiGe channel with higher hole mobility and stronger gate controllability over the ultrathin channel, with effective electrical isolation from the Si core. From a processing point of view, low-temperature epitaxy or Ge condensation techniques can be employed to obtain an ultrathin SiGe channel with a seamless

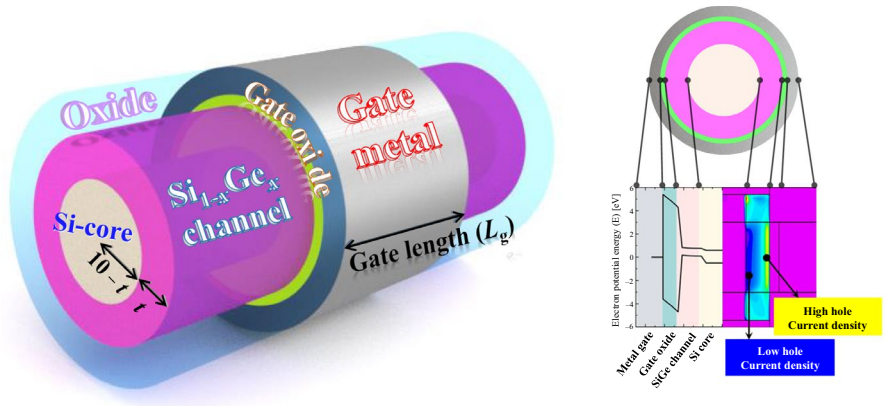

FIGURE 1 Schematics of the proposed *p*-type nanowire FET with SiGe shell channel. (A) Perspective view and (B) cross-sectional view with the energy-band diagram and hole-current density contours

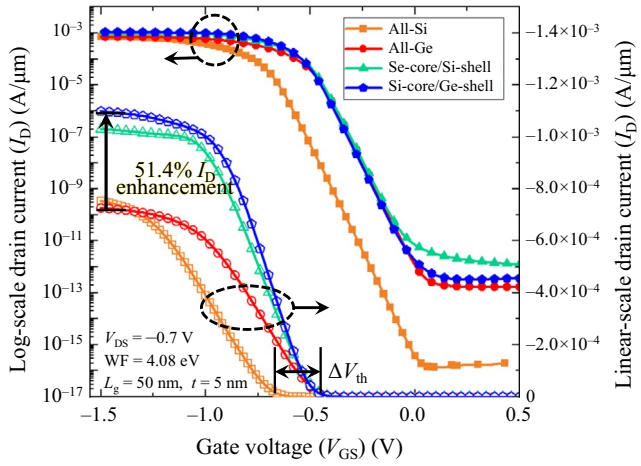

FIGURE 2 Transfer curves of different *p*-type nanowire FETs: all-Si, all-Ge, Ge-core/Si-shell, and the proposed Si-core/Ge-shell

heterojunction to minimize the scattering and to obtain the intended VBO [22–24].

The various structures and material combinations of the nanowire FETs with 10-nm radius such as all-Si, all-Ge, and Ge-core/Si-shell were simulated as the control group and the results were compared with those of the proposed Si-core/SiGe-shell in Figure 2 and Table 1. Figure 2 shows the drain current (I_D)-gate voltage (V_{GS}) characteristics and Table 1 includes the DC parameters of different structures of *p*-type nanowire FETs at a drain voltage (V_{DS}) of –0.7 V. The nanowire radius is 10 nm and the core radius and shell thickness were designed to be 5 nm and 5 nm respectively, for fair reflection of effects by Si and Ge in the radial direction. In this case, the *n*-type channel doping concentration was 10^{15} cm^{-3} for better logic switching with an increased on-state current (I_{on}), smaller depletion capacitance, minimized random-dopant fluctuation (RDF), and decreased impurity scattering to realize high-speed transportation [25]. Considering both DC and AC parameters, the doping concentration of the source and drain (S/D) has an optimum range between 5×10^{18} cm^{-3} and 10^{19} cm^{-3}, which provides a narrow design window to achieve not only high-current drivability but also to suppress the off-state current (I_{off}). In the simulation, the S/D doping concentration is set to 5×10^{18} cm^{-3} as the lower value of the optimum range to avoid junction-formation issues for Ge [26,27]. The maximum transconductance, subthreshold swing, and drain-induced barrier lowering are denoted by $g_{m,max}$, S, and DIBL, respectively. Since different structures have different effective channel areas due to VBO, I_D is normalized by the effective channel width for a fair comparison. All-Si or all-Ge nanowires are normalized by the nanowire diameter of 20 nm and Ge-core/Si-channel. The Si-core/Ge-shell FETs with a QW channel are normalized by 2t. The threshold voltage (V_{th}) is extracted via the constant current method where I_D is 10^{-7} A/μm. The all-Si nanowire FET demonstrates a higher V_{th} and lower I_{on} due to the relatively large E_g. The proposed Si-core/Ge-shell nanowire FET exhibits the highest I_{on} and $g_{m,max}$ values among the devices in the comparison group. The devices with the homogeneous structures have several superior DC parameters than those with the heterogeneous structures. In Table 1, the core-shell nanowire FETs show better g_m while S and DIBL are inferior compared with those of homogeneous structure nanowire FETs. The weight can be applied differently to the parameters depending on the importance assigned by the designers. However, the higher g_m would be advantageous in high-frequency applications in which the representative parameters of f_T and f_{max} are strongly correlated with g_m. Compared with the Ge-core/Si-shell device, the proposed device demonstrates good performance, a higher I_{on} and I_{on}/I_{off} ratio, smaller S near 60 mV/dec, and a small DIBL. It should be noted that the Si-core/Ge-shell nanowire *p*-type FET can be a device for LP and HP operation.

3 | RESULTS AND DISCUSSION

3.1 | Optimization of Ge shell channel thickness

The proposed Si-core/SiGe-shell nanowire FET has been optimally designed with respect to t and x in sequence and then the effects of L_g scaling and frequency characteristics on the operation characteristics have been closely investigated. The nanowire was designed to have a 10-nm radius to ensure a small dimension and the ratio between the Si core and Ge shell channel was controlled to be 10-t and t, respectively. L_g is fixed to 50 nm to observe the pure

TABLE 1 DC parameters of different *p*-type nanowire FETs

Nanowire FETs	All-Si	All-Ge	Ge-core/Si-shell	Si-core/Ge-shell
Channel structure				
$g_{m,max}$ (S/μm)	1.34×10^{-3}	1.15×10^{-3}	2.12×10^{-3}	2.53×10^{-3}
S (mV/dec)	60.39	61.75	62.49	61.71
DIBL (mV/V)	16.71	19.04	21.17	19.83

effects of the control parameters before the SCEs became dominant. In Figure 3, I_D vs. V_{GS} curves are depicted and normalized with the channel width of $2t$. A large portion in t above 3 nm has the effect of reducing I_{off} because there is a higher potential barrier seen from the carriers in the source junction toward the channel direction. As t gets thinner, there is a quantum shift in V_{th} that increases V_{th} due to the stronger energy-level quantization of the cylindrical confinement potential, which has an inverse relation to the square of r and t (1):

$$E = \frac{\hbar^2 u_{ni}^2}{2m^*(r+t)^2} - \frac{\hbar^2 u_{ni}^2}{2m^* r^2} \quad (1)$$

where u_{ni} and m^* are the ith zero value of the Bessel function $J_n(x)$ and the effective mass of the hole, respectively. In the inset of Figure 3, the hole concentration for different t values of 0, 1, 3, 5, and 10 nm are depicted. When t is 1, 3, and 5 nm, 53.1%, 92.1%, and 97.68% of the holes are confined in the Ge QW, respectively. It is confirmed that for a thinner t, it is more difficult to collect holes in the hole gas. There are two reasons for this. Firstly, the wavefunction's peak in the inversion layer is approximately 20 Å from the gate oxide-semiconductor interface [28,29]. In addition, the wavefunction with a thinner channel has a wider distribution in the momentum space due to the uncertainty principle [30]. Figure 4 shows I_{on} and S, where I_{on} is evaluated at $V_{DD} = V_{GS} = V_{DS} = -0.7$ V. The I_{on} shows a turn-around characteristic, which has a maximum at t of 3 nm. Although S is retained near 60 mV/dec at room temperature, a thinner t demonstrates a smaller S. As a result, for LP and HP operation, t has a lower limit at 3 nm for high I_{on} and low I_{off}.

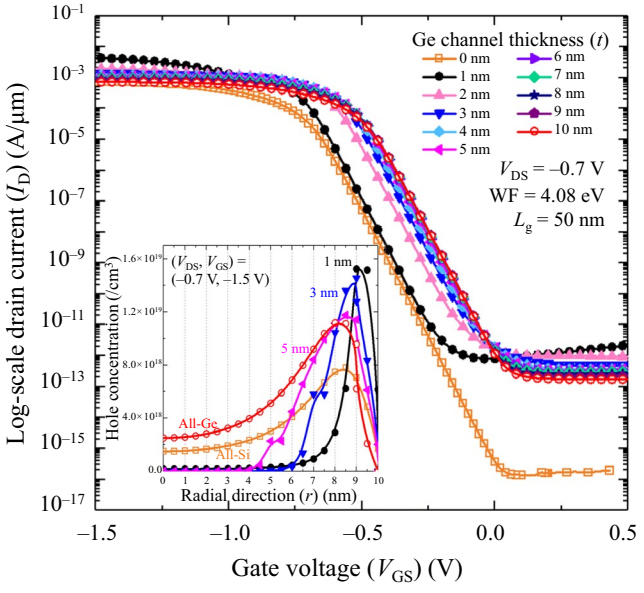

FIGURE 3 I_D-V_{GS} curves of the proposed device for different t with the total radius ($r + t$) fixed at 10 nm. Hole concentration values are included with respect to $t = 0$, 1, 3, 5, and 10 nm in the middle of the channel in the radial direction

3.2 | Optimization of Ge fraction in the SiGe channel

There is a large lattice mismatch between Si and Ge, which induces serious interface status and stacking faults. The critical thickness of Ge is only a few nanometers, which is responsible for the limit in determining t [31,32]. Therefore, in this structure, the SiGe channel is considered and the thickness is restricted below 10 nm. For the growth of the thin SiGe channel on the Si core without severe defect formation, either reduced-pressure chemical vapor deposition (RPCVD) or Ge condensation technique can be used. To optimize the Ge fraction in the $Si_{1-x}Ge_x$ channel, x is controlled from 0 to 1 in increments of 0.2 for L_g = 50 nm. Considering the layout dependency and critical thickness, the t value of the Si-core/Ge-shell nanowire FET is fixed to the lower limit of 3 nm [33]. As a function of x, the mobilities, saturation velocities, E_g, and χ of electrons and holes are modeled for

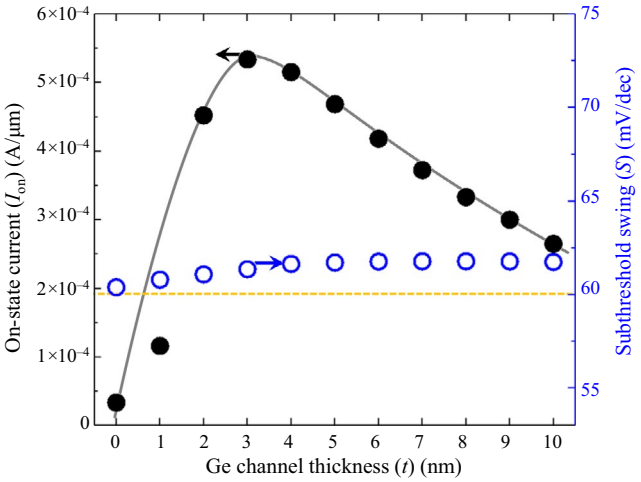

FIGURE 4 I_{on} vs S as a function of t

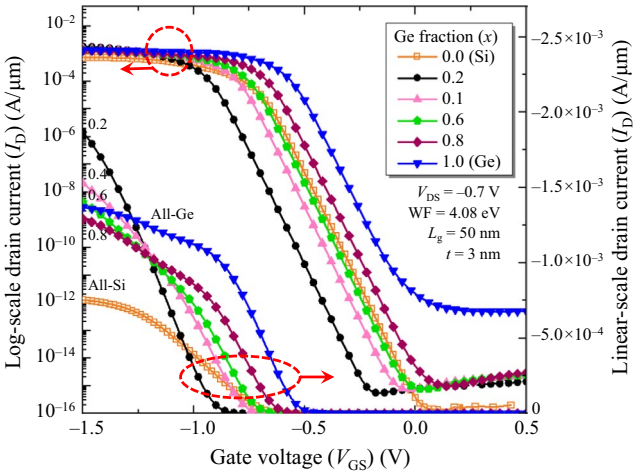

FIGURE 5 Transfer curves of SiGe shell channel nanowire FETs with different values of x

different values of x and implemented in the numerical device simulation. The density-of-states (D.O.S) for x are also considered in the series of simulation works. Figure 5 shows the transfer curves of the proposed device for different values of x. As x increases, the transfer curve shifts toward the right side due to the decrease in the built-in potential between the source and the channel. E_g becomes smaller as x increases, introducing a larger number of thermally generated electrons. In addition, I_{off} increases by an order of 10^3 as x changes from 0 to 1, which corresponds to the amount of change in intrinsic carriers in the order of 10^3. In addition, E_g simultaneously increases the inter-band tunneling probability. These results are attributed to the increased leakage current in the off state. However, the shell channel device shows a satisfactorily suppressed leakage current because of the increase in the effective E_g, which increases the effective tunneling barrier width by energy-level quantization [34,35]. The Si-core/$Si_{0.8}Ge_{0.2}$ shell indicates the highest $I_{d,sat}$ and $g_{m,max}$, and $I_{d,sat}$ decreases with increasing x, except for $x = 1.0$. In Figure 6A, the hole-current densities with valence bands and z-direction electric field contours are presented. In addition, the hole-current densities with valence bands and z-direction electric field contours with the direction identified are shown with respect to the shell channel nanowires where x is 0.2 and 0.8, respectively.

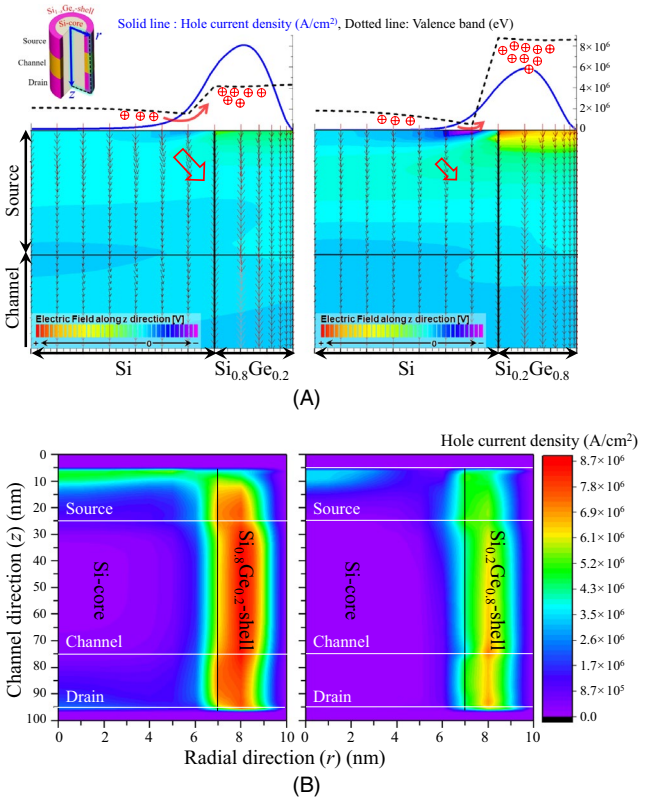

FIGURE 6 On-state characteristics with x values of 0.2 and 0.8 at (V_{DS}, V_{GS}) = (–0.7 V, –1.5 V). (A) Hole-current densities with valence bands along the radial direction and electric field contours. (B) Hole-current density contours

The size and color brightness of the vector indicates the amount of current. The work function (WF) difference between Si and $Si_{1-x}Ge_x$ increases with x and this induces a potential difference between the source-metal/$Si_{1-x}Ge_x$ junction and the source-metal/Si junction. As a result, a higher potential barrier seen by the holes in Si becomes high. The heights of the barrier are 0.03 eV and 0.068 eV for x values of 0.2 and 0.8, respectively, as shown in Figure 6A. At room temperature, the carrier's thermal energy is 0.0259 eV. As such, it is easy for the holes to overcome the 0.03-eV barrier height and enter the SiGe QW. Otherwise, 0.068 eV is relatively large for holes to diffuse toward the SiGe QW, as shown in Figure 6A. This concurs with the hole-current density contour of Figure 6B. At a higher x of 0.8, the holes are electrically insulated between Si and SiGe at the source region and this results in a decrease in the carrier population in the SiGe QW. S is kept very small near 60 mV/dec over the entire Ge fraction variation range. The DIBL has a small value with a 4-mV/V window over the entire x, which is converted to a V_{th} shift range between 9.09 mV and 11.5 mV. Such small deviations in S and DIBL are attributed to the strong gate controllability prepared by the proposed device structure and material composition with an ultrathin shell channel and effective E_g. Optimum device performances are observed for values of x above 0.2 except for 1.0 because of the high leakage current. From a device structuring perspective, a higher x also provides a small window for the shell thickness and a clean interface is required. This can be achieved by *in-situ* cleaning by removing the native oxide for superior crystallinity and roughness minimization [36]. To obtain the intended low-power and high-speed operation characteristics of the proposed device, the growth of a conformal and defect-free shell channel with high crystallinity are paramount issues. These requirements can be achieved by considering the thickness of the shell channel to be less than the critical thickness. However, for the core/shell nanowire structure, the critical thickness is larger than that of the planar growth, which reduces the burden in terms of the selection of the thickness and Ge fraction of the shell layer [37]. Furthermore, conformal and either a single-like or polycrystalline shell layer can be obtained by choosing the appropriate gas-phase species, employing a vapor-liquid-solid chemical vapor deposition (VLSCVD), adopting the nucleation properties of Ge adatoms on the Si facets, and making the core structure similar to a circle [38–41]. With respect to the gate stack, a Si-capping layer and post-deposition annealing (PDA) can be solutions for higher mobility and a reduced gate leakage current [42,43].

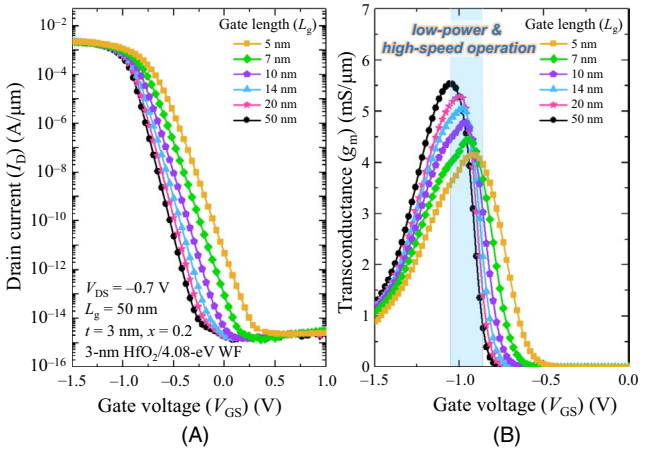

FIGURE 7 Gate length scaling. (A) Transfer curves and (B) g_m as a function of V_{GS} at V_{DS} = –0.7 V

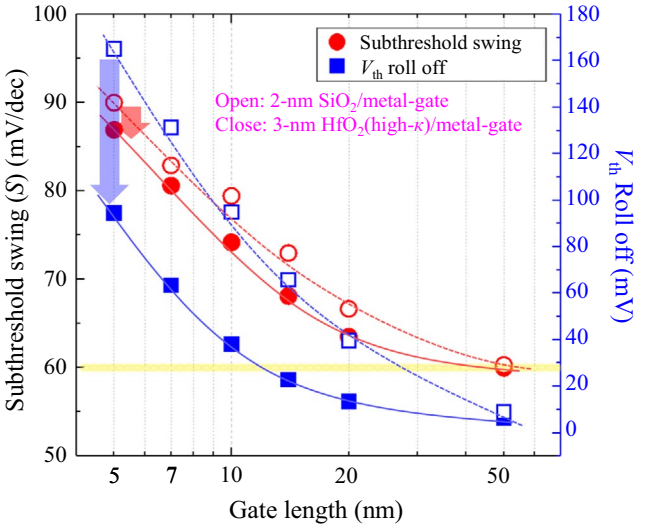

FIGURE 8 S and V_{th} roll-off as a function of L_g under different gate oxide conditions: 2-nm SiO_2 (open symbol) and 3-nm HfO_2 (closed symbol)

3.3 | Gate length scalability and high-frequency performance

The investigation of L_g scaling leverage was performed under the conditions of t = 3 nm and x = 0.2. These are the lower limits of the provided optimum range in this study. With a 3-nm SiGe, the critical x is approximately 0.85 and this study considers practical values. L_g scaling is performed in the range from 50 nm down to 5 nm, and a high-κ (3-nm HfO_2 was adopted for the 2025 ITRS)/metal-gate (HKMG) technology for the year 2023 and after as targeted by the ITRS. Due to the higher gate electrostatics over the nanowire and shell structures, the I_{on}/I_{off} ratio is determined to be above 10^7. At L_g = 5 nm, a high I_{on} value of 1398 μA/μm is obtained under a low V_{DD} of –0.7 V, which is aligned to indicate an I_{off} value of 100 nA/μm at V_{GS} = 0 V [2]. With respect to the 2018 ITRS HP chapter requirement of 1353 μA/μm for p-type channels, the proposed device shows strong HP operation capability even at a low V_{DD}. Figure 7A shows the transfer curves for different values of L_g. In this case, V_{DD} is set to –0.7 V to meet the requirement that the S and V_{th} roll-off decrease by 3.1 mV/dec and 70.6 mV, respectively, for 5-nm L_g. Although the S characteristic is reduced with L_g scaling, it is suppressed well-below 90 mV/dec. Given that the channel doping is as low as 10^{15} cm^{-3}, the reduction in the barrier height becomes significant as L_g gets shorter due to the relatively faster expansion of the depletion region into the channel in source-to-channel or drain-to-substrate p-n junctions. However, the gate-induced-drain leakage (GIDL) is successfully suppressed. Figure 7B depicts the first derivatives of the I_D-V_{GS} curves and g_m values at various L_g values. All the g_m-V_{GS} curves indicate maximum values that range between –0.85 V and –1.05 V and show the strong potential for LP and high-speed operation capabilities. As L_g gets shorter, S and V_{th} roll-off (calculated from DIBL) are degraded as shown in Figure 8. However, the device performances are improved at the same L_g condition by using the HKMG stack, compared with the case of 2-nm SiO_2 stack, which was employed based on the 45-nm logic technology node [44]. Even for L_g values that are extremely scaled down below 7 nm, the V_{th} roll-off appears to be smaller than 100 mV with the HKMG stack.

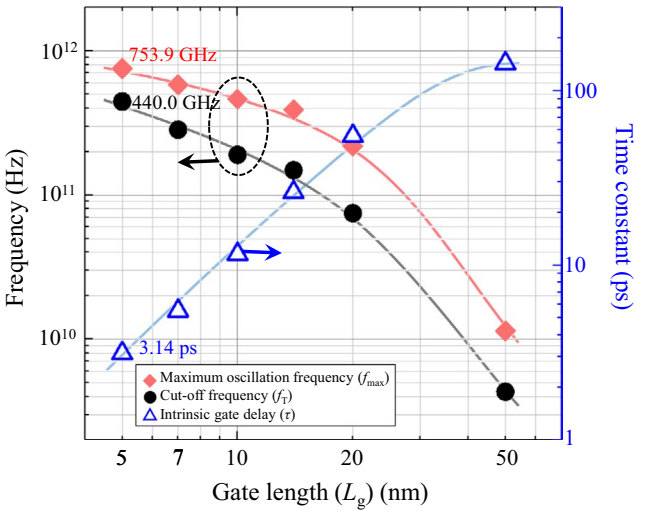

FIGURE 9 High-frequency performance as a function of L_g at V_{DD} = –0.85 V

The cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) are depicted in Figure 9 at V_{DD} = –0.85 V at the lower limit of $g_{m,max}$. From Figure 9, f_T = 440.0 GHz and f_{max} = 753.9 GHz are obtained. f_T is proportional to g_m and f_{max} is proportional to f_T [45]. The intrinsic gate delay ($\tau = C_g|V_{DD}|/I_{on}$) was calculated as in Figure 9. The gate capacitance (C_g) is evaluated from the quasi-static capacitance-voltage (QSCV) curve at V_{DD} = –0.85 V, and τ is determined to be as small as 3.14 ps. By considering the possibility of operating

in the THz regime under LP conditions, it is encouraging that an f_{max} value near 1 THz and a τ value near 1 ps were obtained.

The proposed *p*-type nanowire MOSFET has been compared with other devices with different channel compositions with respect to analog and digital performances at $L_g = 10$ nm. The nanowires have 10-nm radii divided into 7-nm core radii and 3-nm shell thickness. For a fair comparison, $V_{DD} = -1.0$ V was applied such that all the nanowire MOSFETs are in the saturation region. As one of the key high-speed performance parameters for analog applications, f_T values were extracted and depicted in Figure 10A. The highest f_T was obtained from the proposed device due to the superior current drivability, as proven in the previous section. The rising ($t_{d,rise}$) and falling delay times ($t_{d,fall}$) were extracted from the nanowire MOSFETs as shown in Figure 10B to evaluate the high-speed performance required for digital applications. The input V_{GS} pulse has rising, duration, and falling times of 20/20/20 ns at $V_{DS} = 1.0$ V, respectively. $t_{d,rise}$ and $t_{d,fall}$ are evaluated based on the time difference between the instants when V_{GS} reaches the targeted high/low values and when I_D finally saturates to the maximum/minimum values in accordance with the input voltages. All the nanowire MOSFETs exhibited ultrafast switching below 25 ps regardless of the channel material configuration, as indicated by Figure 10B. The nanowire MOSFET devices employing Ge channel, all-Ge device, and the proposed MOSFET demonstrated the shortest delay times. It is confirmed that the proposed Si-core/SiGe-shell *p*-type nanowire MOSFET is potentially a strong candidate for both high-speed analog and digital applications.

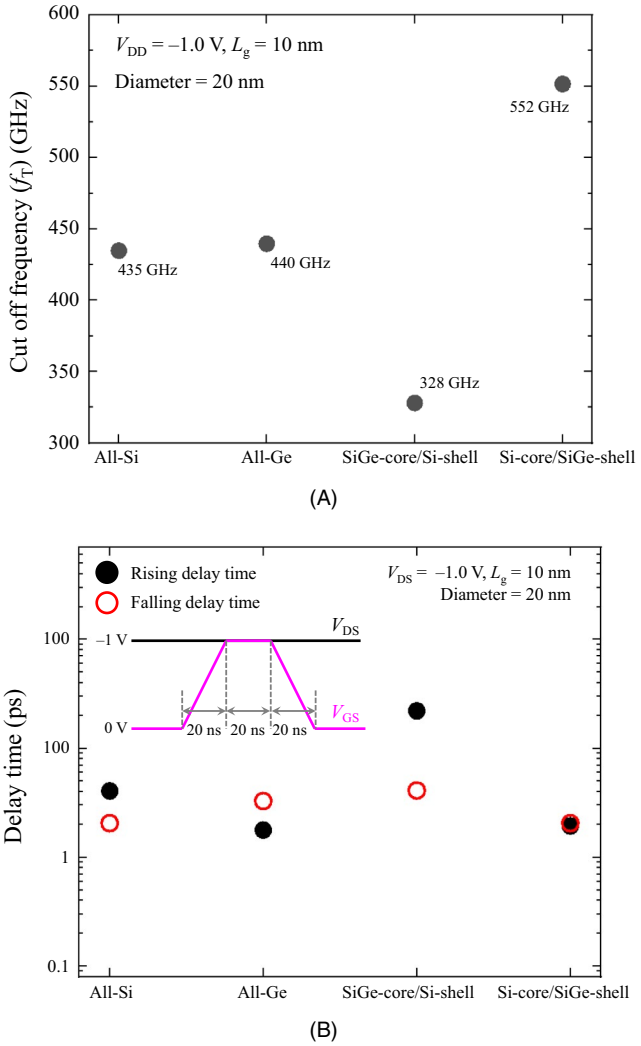

FIGURE 10 Analog and digital performance parameters. (A) f_T and (B) rising ($t_{d,rise}$) and falling delay time ($t_{d,fall}$)

4 | CONCLUSION

In this work, a Si-core/SiGe-shell channel *p*-type nanowire FET was proposed, optimally designed, and characterized. The high I_{on}/I_{off} ratio above 10^7, small *S* near 60 mV/dec, and extremely small DIBL of only a few millivolts demonstrate the superior performance of the proposed design. Considering not only the process point but also device performance, device structuring is carried out and the results indicate a lower limit for *t* of 3 nm and *x* of 0.2, to ensure LP and high-speed operation characteristics. Considering the lower values for device structuring, the obtained values of f_{max} and τ were approximately 1 THz and 1 ps, respectively. The SiGe shell channel nanowire FET has good potential not only for applications to realize more ideal logic but also as an important RF component that is fully functional in the THz frequency regime.

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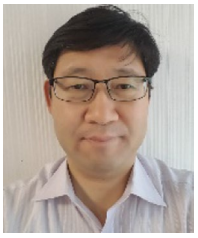

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