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Common-Mode Voltage and Current Harmonic Reduction for Five-Phase VSIs with Model Predictive Current Control

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Abstract

This paper proposes an effective model predictive current control (MPCC) that involves using 10 virtual voltage vectors to reduce the current harmonics and common-mode voltage (CMV) for a two-level five-phase voltage source inverter (VSI). In the proposed scheme, 10 virtual voltage vectors are included to reduce the CMV and low-order current harmonics. These virtual voltage vectors are employed as the input control set for the MPCC. Among the 10 virtual voltage vectors, two are applied throughout the whole sampling period to reduce current ripples. The two selected virtual voltage vectors are based on location information of the reference voltage vector, and their duration times are calculated using a simple algorithm. This significantly reduces the computational burden. Simulation and experimental results are provided to verify the effectiveness of the proposed scheme.

Key words: Common-mode voltage (CMV), Five-phase voltage source inverter, Model predictive current control (MPCC), Reduced current harmonics

I. INTRODUCTION

Over the last decade, a number of five-phase drives have been developed for various applications such as naval propulsion systems, more-electric aircraft, electric vehicle traction drives and offshore turbines due to their advantages over their three-phase counterparts: enhanced faulty tolerance, lower torque pulsation, higher torque density, reduced per phase current without an increased per phase voltage, and lower dc-link current harmonics [1]-[6]. Typically, five-phase drives are supplied by a two-level five-phase voltage source inverter (VSI).

Some of the modulation and control schemes that have been developed for five-phase VSIs include space vector pulse-width modulation (PWM) [7], carrier-based PWM [8], and model predictive current control [9]. Among these, model predictive current control (MPCC) is the most effective and simplest current control scheme for five-phase VSIs due to its simple principle, quick response, and control flexibility [10]-[12]. In the MPCC for five-phase VSIs, the output current is predicted for all of the possible voltage vectors of a five-phase VSI, while the optimal voltage vector is selected using a predefined cost function with error terms between the predicted output current and the reference. Finally, the optimal voltage vector is applied during the sampling time period to drive the five-phase VSI.

Despite these advances, the MPCC for five-phase VSIs still suffers some certain problems, namely high computational burden, low-order current harmonics, and common-mode voltage (CMV). CMV causes electromagnetic interference effect where the fault activation of current detector circuits and common-mode currents leads to motor bearing failures [13], [14]. Some MPCC schemes have been developed in attempts to reduce the CMV for five-phase VSIs by selecting suitable voltage vectors for the input control set [15], [16]. When compared to the conventional MPCC scheme, the peak CMV of these schemes is reduced by 80%. However, large low-order current harmonics are inevitable due to the fact that only one voltage vector is applied during one sampling period to drive the VSI. In [17], virtual voltage vectors were employed as an input control set of MPCC to reduce low-order current

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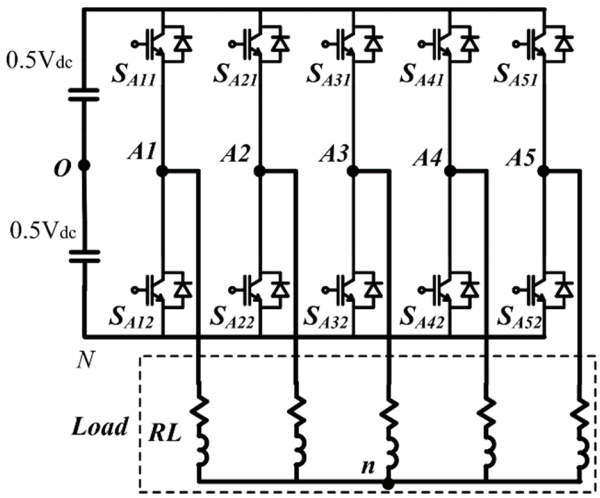

Fig. 1. Two-level five-phase voltage source inverter.

harmonics. Although the low-order current harmonics were significantly reduced in this scheme, the computation time remained relatively high since it involved a large number of current predictions and cost function evaluations. Furthermore, the CMV problem was not considered.

In order to overcome these limitations, this paper proposes an effective MPCC scheme using 10 virtual voltage vectors to reduce the CMV and current harmonics for a five-phase VSI. In the proposed scheme, 10 virtual voltage vectors are used as an input control set for the MPCC scheme to simultaneously reduce the CMV and low-order current harmonics. Furthermore, two of the 10 virtual voltage vectors are applied during one sampling period to reduce current ripples. The two virtual voltage vectors are determined according to the location of the reference voltage vector. In addition, their duration times are calculated using a simple algorithm. This considerably reduces the computation time. Simulation and experimental results are provided to verify the effectiveness of the proposed scheme.

II. Conventional MPCC Scheme of a Two-Level Five-Phase VSI

A. Model of Two-Level Five-Phase VSI

An electrical diagram of a two-level five-phase VSI is shown in Fig. 1. The switching function of each phase S_i (i=*A1, A2, A3, A4, A5*) is defined as:

$$S_i = \begin{cases} 1 \text{ if } S_{i1} = 1 \text{ and } S_{i2} = 0 \\ 0 \text{ if } S_{i1} = 0 \text{ and } S_{i2} = 1 \end{cases} \quad (1)$$

Then, the inverter pole voltages are expressed as:

$$V_{iN} = S_i V_{dc}, \quad (2)$$

where V_{dc} is the DC-link voltage.

The inverter phase voltages are written as functions of the inverter pole voltages:

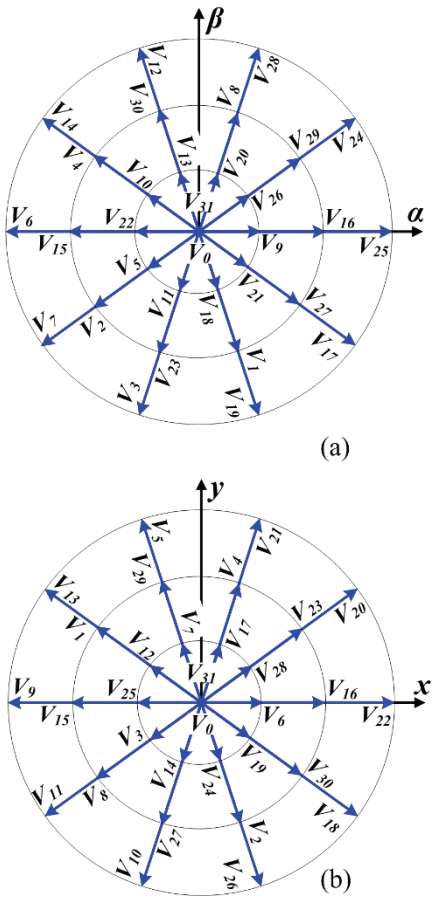

Fig. 2. Five-phase VSI voltage space vectors in: (a) (α-β) plane, (b) (x-y) plane.

$$\begin{aligned} V_{A1} &= (4/5)V_{A1N} - (1/5)(V_{A2N} + V_{A3N} + V_{A4N} + V_{A5N}) \\ V_{A2} &= (4/5)V_{A2N} - (1/5)(V_{A1N} + V_{A3N} + V_{A4N} + V_{A5N}) \\ V_{A3} &= (4/5)V_{A3N} - (1/5)(V_{A1N} + V_{A2N} + V_{A4N} + V_{A5N}) \\ V_{A4} &= (4/5)V_{A4N} - (1/5)(V_{A1N} + V_{A2N} + V_{A3N} + V_{A5N}) \\ V_{A5} &= (4/5)V_{A5N} - (1/5)(V_{A1N} + V_{A2N} + V_{A3N} + V_{A4N}) \end{aligned} \quad (3)$$

The five-phase VSI generates 32 switching state combinations. Each switching state combination corresponds to a voltage vector, which is mapped into both the (α-β) and (x-y) planes using a Clarke transformation as follows [13]:

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_x \\ V_y \end{bmatrix} = \frac{2}{5} \begin{bmatrix} 1 & \cos\delta & \cos 2\delta & \cos 3\delta & \cos 4\delta \\ 0 & \sin\delta & \sin 2\delta & \sin 3\delta & \sin 4\delta \\ 1 & \cos 3\delta & \cos\delta & \cos 4\delta & \cos 2\delta \\ 0 & \sin 3\delta & \sin\delta & \sin 4\delta & \sin 2\delta \end{bmatrix} \begin{bmatrix} V_{A1} \\ V_{A2} \\ V_{A3} \\ V_{A4} \\ V_{A5} \end{bmatrix}, \quad (4)$$

where δ=2π/5.

Figs. 2(a)-2(b) show the space vectors for the five-phase VSI in the (α-β) and (x-y) planes. The obtained voltage vectors are classified into four groups, as shown in Table I: zero vectors (ZV), small vectors (SV), medium vectors (MV), and large vectors (LV).

TABLE I
CMV ASSOCIATED WITH DIFFERENT VOLTAGE VECTOR GROUPS

Group	Voltage vectors	$\|V_{\alpha\beta}\|$	$\|V_{xy}\|$	$\|V_{CM}\|$
ZV	V_0(00000), V_{31}(11111)	0	0	$0.5V_{dc}$
SV	V_9(01001), V_{26}(11010), V_{20}(10100), V_{13}(01101), V_{10}(01010), V_{22}(10110), V_5(00101), V_{11}(01011), V_{18}(10010), V_{21}(10101)	$0.2472V_{dc}$	$0.6472V_{dc}$	$0.1V_{dc}$
MV	V_{16}(10000), V_{29}(11101), V_8(01000), V_{30}(11110), V_4(00100), V_{15}(01111), V_2(00010), V_{23}(10111), V_1(00001), V_{27}(11011)	$0.4V_{dc}$	$0.4V_{dc}$	$0.3V_{dc}$
LV	V_{25}(11001), V_{24}(11000), V_{28}(11100), V_{12}(01100), V_{14}(01110), V_6(00110), V_7(00111), V_3(00011), V_{19}(10011), V_{17}(10001)	$0.6472V_{dc}$	$0.2472V_{dc}$	$0.1V_{dc}$

B. Common-Mode Voltage Analysis

The common-mode voltage (CMV) in a five-phase VSI is expressed as:

$$V_{CM} = V_{nO} = V_{nN} - V_{dc}/2 \tag{5}$$

The absolute value of the CMV for each voltage vector group is:

$$|V_{CM}| = |V_{nN} - V_{dc}/2| = \begin{cases} 0.5V_{dc} \text{ for zero vectors} \\ 0.1V_{dc} \text{ for small vectors} \\ 0.3V_{dc} \text{ for medium vectors} \\ 0.1V_{dc} \text{ for larger vectors} \end{cases} \tag{6}$$

From Table I, it can be clearly seen that the large voltage vector group provides the lowest CMV with the highest output voltage in the (α-β) planes.

C. Conventional MPCC Scheme

As shown in Fig. 1, the relationships between the output voltage and current of a five-phase VSI with an RL load in the (α-β) and (x-y) planes are expressed as follows:

$$\boldsymbol{V}_{\alpha\beta} = R\boldsymbol{i}_{\alpha\beta} + L\frac{d\boldsymbol{i}_{\alpha\beta}}{dt}, \tag{7}$$

$$\boldsymbol{V}_{xy} = R\boldsymbol{i}_{xy} + L\frac{d\boldsymbol{i}_{xy}}{dt}, \tag{8}$$

where $\boldsymbol{i}_{\alpha\beta}$ and $\boldsymbol{V}_{\alpha\beta}$ are the current and voltage vectors in the (α-β) plane; $\boldsymbol{i}_{xy}$ and $\boldsymbol{V}_{xy}$ are current and voltage vectors in the (x-y) plane; and R and L are the load resistance and inductance, respectively.

The derivatives of the currents in (7) and (8) are approximated using a forward Euler approximation with a sampling period T_s as follows:

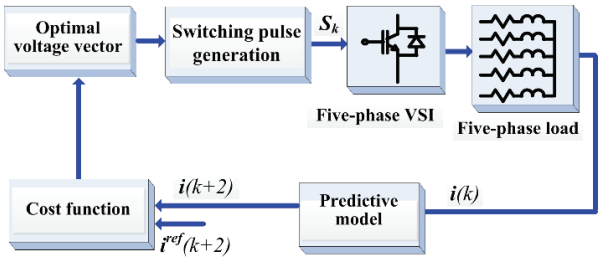

Fig. 3. Block diagram of the conventional MPCC scheme.

$$\frac{d\boldsymbol{i}_{\alpha\beta}}{dt} = \frac{\boldsymbol{i}_{\alpha\beta}(k+1) - \boldsymbol{i}_{\alpha\beta}(k)}{T_s} \tag{9}$$

$$\frac{d\boldsymbol{i}_{xy}}{dt} = \frac{\boldsymbol{i}_{xy}(k+1) - \boldsymbol{i}_{xy}(k)}{T_s} \tag{10}$$

By substituting (9) into (7) and (10) into (8), the relationship between the output voltage and current in the discrete-time domain can be obtained as follows:

$$\boldsymbol{i}_{\alpha\beta}(k+1) = \boldsymbol{i}_{\alpha\beta}(k) + \frac{T_s}{L}(\boldsymbol{V}_{\alpha\beta}(k) - R\boldsymbol{i}_{\alpha\beta}(k)) \tag{11}$$

$$\boldsymbol{i}_{xy}(k+1) = \boldsymbol{i}_{xy}(k) + \frac{T_s}{L}(\boldsymbol{V}_{xy}(k) - R\boldsymbol{i}_{xy}(k)) \tag{12}$$

A one-step delay compensation method is adopted to compensate for the time delay caused by the digital implementation, where the currents and voltages in (11) and (12) are shifted one step forward in time to obtain the currents at the instant (k+2), as in [18]:

$$\boldsymbol{i}_{\alpha\beta}(k+2) = \boldsymbol{i}_{\alpha\beta}(k+1) + \frac{T_s}{L}(\boldsymbol{V}_{\alpha\beta}(k+1) - R\boldsymbol{i}_{\alpha\beta}(k+1)) \tag{13}$$

$$\boldsymbol{i}_{xy}(k+2) = \boldsymbol{i}_{xy}(k+1) + \frac{T_s}{L}(\boldsymbol{V}_{xy}(k+1) - R\boldsymbol{i}_{xy}(k+1)) \tag{14}$$

In the MPCC for a five-phase VSI, four current components must be simultaneously controlled in two planes, and the cost function g is defined as follows:

$$\begin{aligned} g = &\left|i_\alpha^{ref}(k+2) - i_\alpha(k+2)\right| + \left|i_\beta^{ref}(k+2) - i_\beta(k+2)\right| \\ &+ \lambda_{xy}\left(\left|i_x^{ref}(k+2) - i_x(k+2)\right| + \left|i_y^{ref}(k+2) - i_y(k+2)\right|\right) \end{aligned}, \tag{15}$$

where i_α, i_β, i_x and i_y are the α, β, x and y components of the current vector; i_α^{ref}, i_β^{ref}, i_x^{ref} and i_y^{ref} are the α, β, x and y components of the reference current vector; and λ_{xy} is a weighting factor.

A block diagram of the conventional MPCC scheme for a five-phase VSI is shown in Fig. 3, where an optimal voltage vector that minimizes the cost function (15) is selected to drive a five-phase VSI. Since a larger number of current predictions and cost function evaluations are required to select the optimal voltage vector, the computation time of the MPCC scheme is high. Furthermore, only one voltage vector is applied during one sampling period. This means that the i_x and i_y currents cannot be eliminated. Thus, large low-order harmonics are inevitable in the output current.

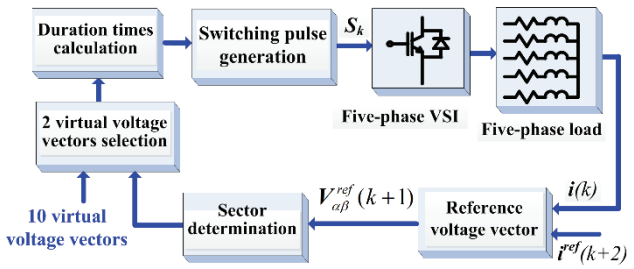

Fig. 4. Block diagram of the proposed MPCC scheme.

III. Proposed MPCC Scheme

In order to minimize the CMV and reduce the low-order current harmonics, 10 virtual voltage vectors with eliminated voltage components in the *(x-y)* sub-plane, which are synthesized from the voltage vectors of the LV group, are used as the input control set in the MPCC scheme. Then, two of the 10 virtual voltage vectors are applied throughout the whole sampling period to reduce the output current ripples. They are selected based on the location information of a reference voltage vector without current predictions. In addition, a new cost function is used to calculate the durations of the selected virtual voltage vectors. Therefore, the computational burden is significantly reduced. Fig. 4 shows a block diagram of the proposed MPCC scheme, which comprises three main parts: 1) the synthesized virtual vectors, 2) the selected virtual vectors and the calculation of their duration times, and 3) the generated switching pulse.

A. Synthesized Virtual Vectors

In order to minimize CMV, 10 voltage vectors of the LV group with the lowest CMV and highest length in the (α-β) plane are employed to construct the input control set of the proposed MPCC scheme. The input control set consists of 10 virtual voltage vectors, and each virtual voltage vector is obtained by combining three adjacent voltage vectors of the LV group to eliminate the x and y voltage components in order to reduce the low-order current harmonics.

For example, the virtual voltage vector $\boldsymbol{V}_{v1}$, which is formed by a combination of voltage vectors $\boldsymbol{V}_{17}$, $\boldsymbol{V}_{25}$ and $\boldsymbol{V}_{24}$, is expressed as:

$$\boldsymbol{V}_{v1} = d_1\boldsymbol{V}_{17} + d_2\boldsymbol{V}_{25} + d_1\boldsymbol{V}_{24} \tag{16}$$

The factors d_1 and d_2 are calculated using the following constraint:

$$\begin{cases} d_1\boldsymbol{V}_{17xy} + d_2\boldsymbol{V}_{25xy} + d_1\boldsymbol{V}_{24xy} = \boldsymbol{0} \\ 2d_1 + d_2 = 1 \end{cases} \tag{17}$$

From (17), the factors d_1 and d_2 are given as follows:

$$\begin{cases} d_1 = 0.381966 \\ d_2 = 0.236068 \end{cases} \tag{18}$$

By inserting (18) into (16), the virtual voltage vector $\boldsymbol{V}_{v1}$ is given as:

TABLE II
Synthesized Virtual Voltage Vectors

Virtual voltage vector	Virtual voltage vector synthesis	$\lvert V_{xy}\rvert$	$\lvert V_{CM}\rvert$
$\boldsymbol{V}_{v1}$	$d_1\boldsymbol{V}_{17} + d_2\boldsymbol{V}_{25} + d_1\boldsymbol{V}_{24}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v2}$	$d_1\boldsymbol{V}_{25} + d_2\boldsymbol{V}_{24} + d_1\boldsymbol{V}_{28}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v3}$	$d_1\boldsymbol{V}_{24} + d_2\boldsymbol{V}_{28} + d_1\boldsymbol{V}_{12}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v4}$	$d_1\boldsymbol{V}_{28} + d_2\boldsymbol{V}_{12} + d_1\boldsymbol{V}_{14}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v5}$	$d_1\boldsymbol{V}_{12} + d_2\boldsymbol{V}_{14} + d_1\boldsymbol{V}_{6}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v6}$	$d_1\boldsymbol{V}_{14} + d_2\boldsymbol{V}_{6} + d_1\boldsymbol{V}_{7}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v7}$	$d_1\boldsymbol{V}_{6} + d_2\boldsymbol{V}_{7} + d_1\boldsymbol{V}_{3}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v8}$	$d_1\boldsymbol{V}_{7} + d_2\boldsymbol{V}_{3} + d_1\boldsymbol{V}_{19}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v9}$	$d_1\boldsymbol{V}_{3} + d_2\boldsymbol{V}_{19} + d_1\boldsymbol{V}_{17}$	0	$0.1V_{dc}$
$\boldsymbol{V}_{v10}$	$d_1\boldsymbol{V}_{19} + d_2\boldsymbol{V}_{17} + d_1\boldsymbol{V}_{25}$	0	$0.1V_{dc}$

$$\begin{cases} \boldsymbol{V}_{v1\alpha\beta} = d_1\boldsymbol{V}_{17\alpha\beta} + d_2\boldsymbol{V}_{25\alpha\beta} + d_1\boldsymbol{V}_{24\alpha\beta} = 0.5528V_{dc}\angle 0^0 \\ \boldsymbol{V}_{v1xy} = \boldsymbol{0} \end{cases} \tag{19}$$

The other virtual voltage vectors can be derived similarly based on the relationships presented in Table II. The 10 virtual voltage vectors have the minimum CMV as well as zero x and y voltage components. Therefore, the CMV is minimized and the i_x, and i_y currents are automatically nullified by employing these virtual voltage vectors as the input control set. As a result, the low-order current harmonics are significantly reduced and only the α and β current components need to be controlled.

B. Selected Virtual Vectors and Their Duration Time Calculation

By employing 10 virtual voltage vectors as the input control set, the low-order current harmonics are significantly reduced. However, if only a single virtual voltage vector is applied to drive a five-phase VSI, the output current ripples can remain high due to the absence of a zero voltage vector. In order to reduce the output current ripples, two virtual voltage vectors are selected to drive the five-phase VSI based on location information of the reference voltage vector. The reference voltage vector is obtained from the output current equation in (13):

$$\boldsymbol{V}_{\alpha\beta}^{ref}(k+1) = \frac{L}{T_s}\boldsymbol{i}_{\alpha\beta}^{ref}(k+2) + \frac{R*T_s - L}{T_s}\boldsymbol{i}_{\alpha\beta}(k+1) \tag{20}$$

In the proposed MPCC scheme, the two virtual voltage vectors nearest the reference voltage vector are selected to drive the five-phase VSI. After calculating the reference voltage vector from (20), its location and the two virtual voltage vectors can be determined from the *(α-β)* plane in Fig. 5, which is divided into 10 sectors.

For example, when the reference voltage vector is located in sector 1, the virtual voltage vectors $\boldsymbol{V}_{v1}$ and $\boldsymbol{V}_{v2}$ are selected to drive the five-phase VSI. Then, in order to calculate the duration time of $\boldsymbol{V}_{v1}$ and $\boldsymbol{V}_{v2}$, a new cost function is defined as:

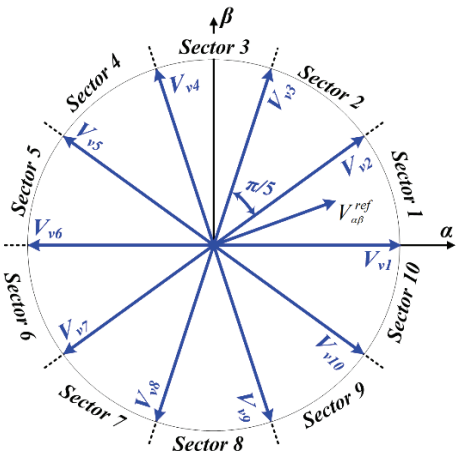

Fig. 5. Distributed virtual voltage vectors in the *(α-β)* plane.

$$g_{new} = \left|V_{\alpha}^{ref}(k+1) - V_{v_i\alpha}\right| + \left|V_{\beta}^{ref}(k+1) - V_{v_i\beta}\right|, \quad (21)$$

where V_{α}^{ref} and V_{β}^{ref} are the α and β components of the reference voltage vector, while $V_{i\alpha}$ and $V_{i\beta}$ are the α and β components of the virtual voltage vector i, respectively.

The cost function value in (21) of $\boldsymbol{V}_{v1}$ and $\boldsymbol{V}_{v2}$ is expressed as:

$$\begin{aligned} g_{new1} &= \left|V_{\alpha}^{ref}(k+1) - V_{v1\alpha}\right| + \left|V_{\beta}^{ref}(k+1) - V_{v1\beta}\right| \\ g_{new2} &= \left|V_{\alpha}^{ref}(k+1) - V_{v2\alpha}\right| + \left|V_{\beta}^{ref}(k+1) - V_{v2\beta}\right| \end{aligned} \quad (22)$$

Then, the duration times of the two virtual voltage vectors, which are inversely proportional to their cost function values, are expressed as follows:

$$\begin{cases} T_1 = g_{new2} T_s / (g_{new1} + g_{new2}) \\ T_2 = g_{new1} T_s / (g_{new1} + g_{new2}) \end{cases}, \quad (23)$$

where T_1 and T_2 are the duration times of $\boldsymbol{V}_{v1}$ and $\boldsymbol{V}_{v2}$, respectively.

It can be clearly seen that in the proposed scheme, the current predictions and weighting factor tuning are avoided and that the duration times of the selected virtual voltage vectors are calculated according to their cost function values. As a result, the computational burden is considerably reduced.

C. Generated Switching Pulse

After determining the two virtual voltage vectors, the corresponding switching pulses are required to drive the five-phase VSI. Typically, symmetrical switching pulses are adopted to reduce the output current harmonics [17]. To this end, the dwell times of the voltage vectors, which are used to synthesize the two selected virtual voltage vectors, must be determined. For example, when the virtual voltage vectors $\boldsymbol{V}_{v1}$ and $\boldsymbol{V}_{v2}$ are selected, the dwell times of the voltage vectors $\boldsymbol{V}_{17}$, $\boldsymbol{V}_{25}$, $\boldsymbol{V}_{24}$ and $\boldsymbol{V}_{28}$ are as follows:

$$\begin{cases} d_{V_{17}} = d_1 T_1; d_{V_{25}} = d_2 T_1 + d_1 T_2; \\ d_{V_{24}} = d_1 T_1 + d_2 T_2; d_{V_{28}} = d_1 T_2; \end{cases} \quad (24)$$

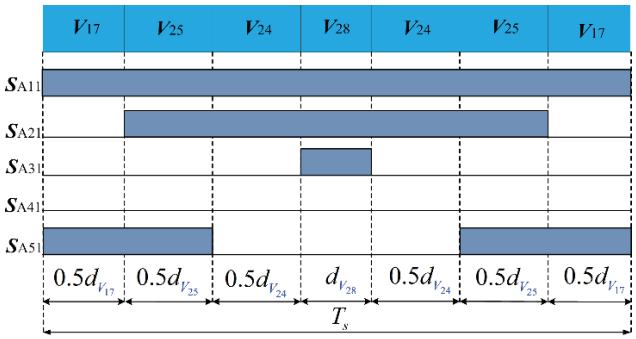

Fig. 6. Generated switching pulse in sector 1.

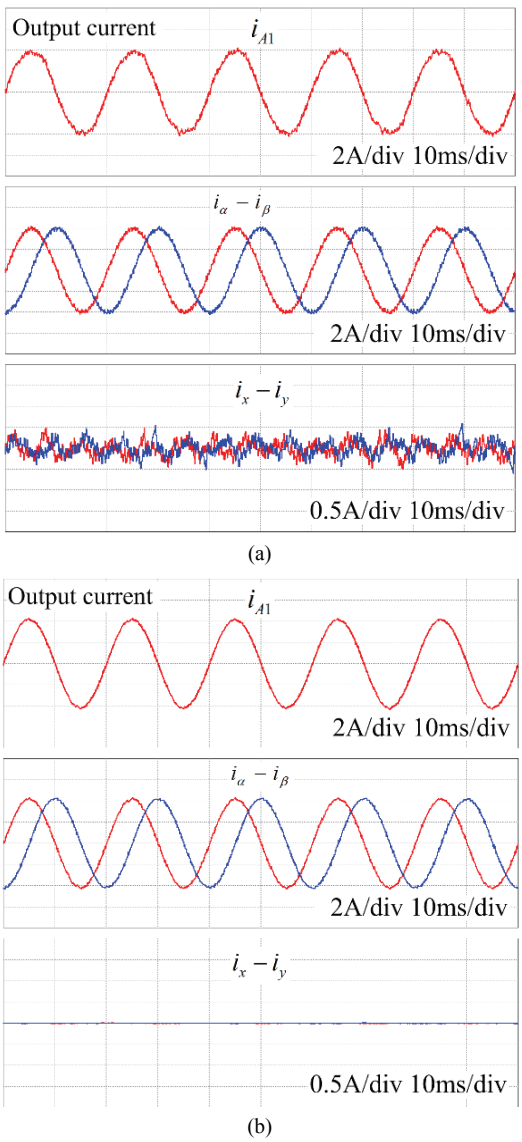

Fig. 7. Steady-state performance simulation of: (a) Conventional scheme, (b) Proposed scheme.

where d_{V17}, d_{V25}, d_{V24} and d_{V28} are the dwell times of the voltage vectors $\boldsymbol{V}_{17}$, $\boldsymbol{V}_{25}$, $\boldsymbol{V}_{24}$ and $\boldsymbol{V}_{28}$, respectively. Fig. 6 shows the symmetrical switching pulses in sector 1, which are used to control the five-phase VSI.

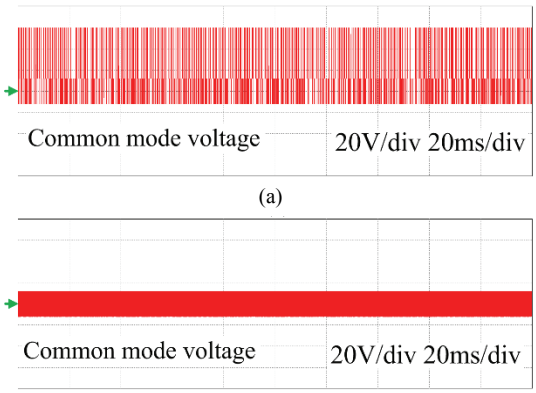

Fig. 8. CMV waveform simulation of: (a) Conventional scheme, (b) Proposed scheme.

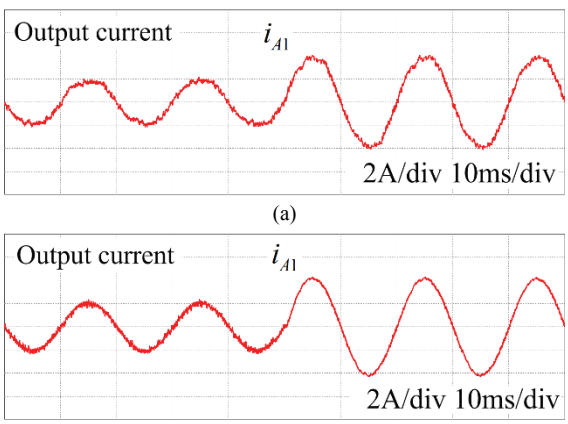

Fig. 9. Dynamic performance simulation of: (a) Conventional scheme, (b) Proposed scheme.

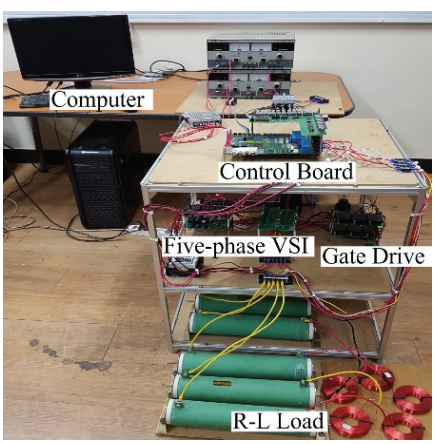

Fig. 10. Experimental system for a five-phase VSI.

IV. Simulation Results

Simulations were conducted using PSIM software to verify the effectiveness of the proposed MPCC scheme. The simulated parameters are as follows: the dc-link voltage Vdc is 120V; the R-L load has R = 13 Ω and L = 15 mH; the output frequency is 50 Hz; and the sampling period is 100us. For the sake of simplicity, the conventional MPCC scheme directly evaluates 11 voltage vectors consisting of one zero voltage vector and 10 voltage vectors of the LV group with the cost function presented in (15).

Fig. 7 shows the steady-state performances of the conventional and the proposed MPCC schemes when the amplitude of the reference current is 4A. From top to the bottom, the waveforms show the phase current i_{A1} as well as the currents in the (α-β) plane and (x-y) plane for both schemes. As shown in the figure, the currents in the (α-β) plane are sinusoidal for both schemes. Meanwhile, the currents in the (x-y) plane of the proposed scheme are effectively eliminated by using virtual voltage vectors. Therefore, the phase current i_{A1} is sinusoidal with the proposed scheme. On the other hand, the phase current i_{A1} is distorted with the conventional scheme due to the large magnitudes of the x and y current components. In addition, CMV waveforms delivered by the two MPCC schemes are shown in Fig. 8. In the conventional scheme, the absolute peak value of the CMV is about 60V, which is $0.5V_{dc}$. Meanwhile, the absolute peak value of the CMV is reduced to 12V in the proposed scheme. This represents an 80% reduction in the absolute peak value of the CMV. In addition, Fig. 9 shows the dynamic performance when the amplitude of the reference current is suddenly changed from 2A to 4A. It can be clearly seen that the proposed scheme has a dynamic response that is similar to that of the conventional scheme.

V. Experimental Results

In order to validate the simulation results, a prototype of a five-phase VSI is implemented in the laboratory as shown in Fig. 10. The proposed scheme is realized using a DSP 32-bit floating-point TI TMS320F28335 and a CPLD Altera EPM7128SLC81-15. The parameters used in the experiment are the same as those used in the simulation.

Fig. 11 shows experimental results of the conventional and the proposed MPCC schemes at the steady-state when the amplitude of the reference current is 4A. From top to bottom, the waveforms contain phase current i_{A1}, its fast Fourier transform (FFT), and the x and y current components for both schemes. As shown in the figure, the x and y current components of the conventional scheme are substantially higher than those of the proposed scheme due to the fact that only one voltage vector is applied during the whole sampling period in the conventional scheme. As a result, the output current phase i_{A1} with the conventional scheme, which consists of high magnitude low-order harmonics (particularly third order), is seriously distorted. On the other hand, the output current phase i_{A1} is sinusoidal with the proposed scheme due to the utilization of two virtual voltage vectors in each sampling period. When compared with the conventional scheme, the total harmonic distortion (THD) of the output

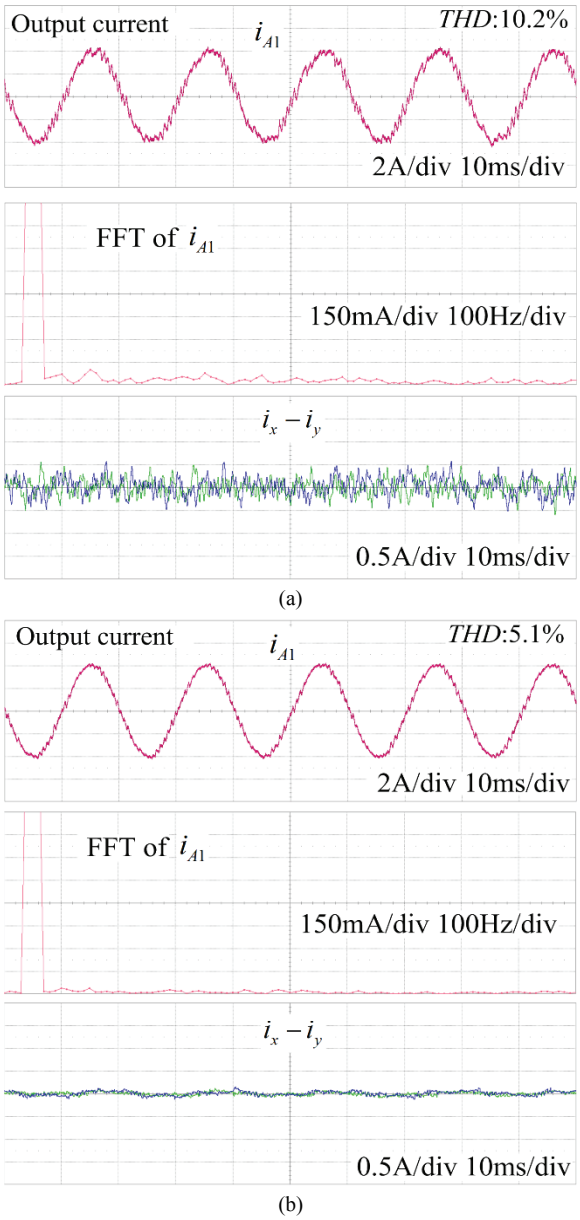

Fig. 11. Steady-state performance experiment of: (a) Conventional scheme, (b) Proposed scheme.

current with the proposed scheme is effectively reduced. In addition, the CMV waveforms generated by the conventional and the proposed MPCC schemes are shown in Fig. 12. It can be seen that the proposed scheme reduced the absolute peak value by 80% when compared to the conventional scheme. This is attributed to the fact that only the voltage vectors of the LV group are used to construct the input control set in the proposed scheme.

Fig. 13 shows experimental results for both of the MPCC schemes when the amplitude of the reference current instantly changes from 2A to 4A. It can be clearly seen that the dynamic performances of both schemes are similar. However, the proposed scheme provides lower current ripples. Furthermore, a computational cost comparison of two schemes is provided

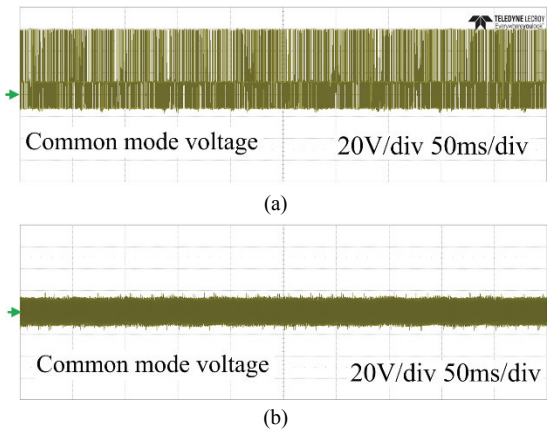

Fig. 12. CMV waveform experiment of: (a) Conventional scheme, (b) Proposed scheme.

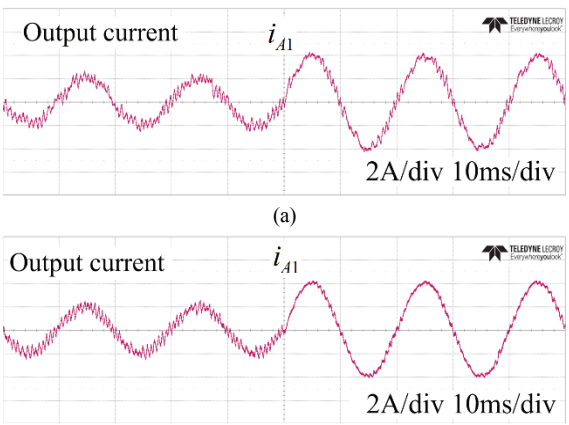

Fig. 13. Dynamic performance experiment of: (a) Conventional scheme, (b) Proposed scheme.

TABLE III
COMPUTATIONAL COST COMPARISON

Parameters	Conventional scheme	Proposed scheme
Number of voltage vectors	*11*	*10*
Number of current predictions calculations	44(44=11*4)	0
Number of voltage reference calculations	0	2(2=1*2)
Number of cost function calculations	11	2
Computation time (us)	31.5	22.4

in Table III. Since the proposed scheme eliminates current predictions and the duration times of selected virtual voltage vectors are determined according to their cost function values, the computation time is significantly reduced when compared to that of the conventional scheme, as presented in Table III.

VI. CONCLUSION

This paper proposed an effective MPCC scheme to reduce the current harmonics and common-mode voltage (CMV) for

a two-level five-phase voltage source inverter (VSI) without using a weighting factor. Since 10 virtual voltage vectors synthesized from the voltage vectors of the LV group are employed as the input control set of the proposed scheme, the absolute peak value of the CMV with the proposed scheme is reduced by 80% when compared to that of the conventional scheme. In the proposed scheme, two of the 10 virtual voltage vectors are selected based on location information of the reference voltage vector and are used to drive five-phase VSI. In addition, their duration times are calculated according to their cost function values. Therefore, the current harmonics and computational burden are considerably reduced. The effectiveness of the proposed scheme has been verified by the simulation and experimental results. When compared to the conventional scheme, the proposed scheme shows the same dynamic performance along with reductions in the current harmonics and computation time.

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