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Implementation of Cuckoo Search Optimized Firing Scheme in 5-Level Cascaded H-Bridge Multilevel Inverter for Power Quality Improvement

Deepshikha Singla* and P.R.Sharma†

†,*Department of Electrical Engineering, YMCA University of Science and Technology, Faridabad, India

Abstract

Multilevel inverters have appeared as a successful and utilitarian solution in many power applications. The prime objective of an inverter is to keep the fundamental component of the output voltage of a multilevel inverter at a preferred value. Equally important is the need to keep the harmonic components in the output voltage within stated harmonic limits. Therefore, the basis of this research is to develop a harmonic minimization function that optimizes the switching angles of cascaded H-bridge multilevel inverter. Due to benefits of the Cuckoo Search (CS) algorithm, it is applied to determine the switching angles, which are further used to generate the switching pattern for firing the H-bridges of multilevel inverter. Simulation results are compared with SPWM based firing scheme. The switching frequency for SPWM firing scheme is taken as 200 Hz since the switching losses are increased when switching frequency is high. To validate the ability of Cuckoo Search optimized firing scheme in minimization of harmonics, experimental results obtained from hardware prototype of Five Level Cascaded H-Bridge Multilevel Inverter equipped with a FPGA controller are presented to verify the simulation results.

Key words: Cascaded H-Bridge multilevel inverters, Cuckoo Search (CS) algorithm, Harmonic minimization, Power quality, Sinusoidal Pulse Width Modulation (SPWM)

I. INTRODUCTION

Nowadays, almost every domestic and industrial load is sensitive to power quality problems. Thus, there is an increased need for a low harmonics source. Multilevel inverters [1], [2] have appeared as a successful and pragmatic solution in the various power applications. Among the existing multilevel inverter topologies, the Cascaded H-bridge Multilevel Inverter (CHMLI) [3], [4] has caught the most attention due to its characteristic feature of producing a staircase voltage output with 'M' steps from an arrangement association of (M-1)/2 control units provided from separate dc inputs. With an increase in the number of units of multilevel inverter, the output resembles a near sinusoidal output voltage. This impressive feature results in better power quality, reduced dv/dt stresses, minimum total harmonic distortion (THD), improved electromagnetic compatibility (EMC), reduced switching losses, and higher-voltage capability. It can also lead to elimination of the coupling transformer, which results in a reduction in costs. However, the performance of multilevel inverters depends on the firing scheme employed for creating the switching pattern for its H-bridges so the harmonics are reduced and power quality of the system is enhanced.

Sinusoidal-PWM (SPWM) [5]-[7] methods are the most commonly used methods for generating a switching pattern by employing a switching frequency in the order of kHz. However, the higher the switching frequency, the greater the switching loss. Selective Harmonic Elimination [8]-[10] technique has replaced the traditional PWM technique to a great extent in harmonic minimization problems. It refers to choosing switching angles so that the specific higher order harmonics such as the 5th, 7th, 11th and 13th are minimized from the output voltage of the inverter. Optimal Minimization of THD (OMTHD) [11] is another well-known method that focuses on minimization of THD. However, the prime objective of an inverter is to keep the fundamental component of the output voltage of multilevel inverter at a desired value.

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†Corresponding Author: deepshikha_16s@yahoo.com
Tel: +917988720847, YMCA University of Science and Technology
*Dept. of Electr. Eng., YMCA Univ. of Science and Technology, India

Equally important, is the need to keep the harmonic components in the output voltage within specified harmonic limits. Therefore, the basic idea of this study is to develop a harmonic minimization function that optimizes the switching angles of a multilevel inverter. Afterwards, choosing an appropriate optimization search algorithm is as important as framing a well-defined optimization problem.

Nowadays, various optimization algorithms are being explored to solve the harmonic minimization problem. A number of research papers discuss the application of Genetic Algorithm (GA) [12], [13], Particle Swarming Optimization (PSO) [14]-[16], Simulated Annealing (SA) [17], and numerous other algorithms [18]-[20]. The benefits of these optimization algorithms are utilized in solving different harmonic minimization problems to obtain a particular switching pattern for the H-bridges of multilevel inverter. This is done in a manner to achieve a minimum THD and a better quality waveform. Each of these algorithms has its own pros and cons and area of application where it benefits the most. However, GA seems to be the most explored optimization technique, in spite of the fact that it involves multiple operations such as crossover, mutation, etc. for a single iteration, which makes it one of the longest techniques. Moreover, most optimization algorithms require tuning of their internal parameters to achieve good performance, which adds to their simulation times. Thus, considering the simplicity and efficiency of the Cuckoo Search [21]-[25] algorithm for solving highly non-linear optimization problems in real-world engineering applications, this research study utilized Cuckoo Search optimization for the power quality improvement of multilevel inverter. Simulation results of a Cuckoo Search optimization based firing scheme employed to a five level cascaded H-bridge multilevel inverter are compared with results obtained using a SPWM based firing scheme. This study implements a hardware prototype of a FPGA controlled five level cascaded H-bridge multilevel inverter for validation of these simulation results.

II. Harmonic Minimization in Cascaded H-Bridge Multilevel Inverters

In this paper, a three-phase cascaded H-bridge configuration of multilevel inverter is used to evaluate the effectiveness of the proposed method. An m-level cascaded H-bridge inverter comprises of a series combination of five H-bridges with separate dc inputs as V_{dc1}, V_{dc2}, V_{dc3}, ….V_{dcm}. If the H-bridges of multilevel inverter are fired by the switching pattern generated using the switching angles α_1, α_2, α_3, ….α_m, the output voltage of multilevel inverter [8] can be expressed in terms of Fourier series expansion as follows:

$$V(t) = \sum_{n=1,3,5}^{\infty} \frac{4V_{dc}}{n\pi} (\cos n\alpha_1 + \cos n\alpha_2 + \ \dots + \cos n\alpha_m) \sin n\alpha_n \quad (1)$$

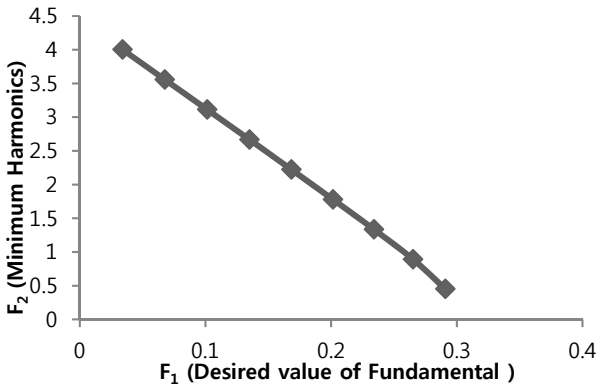


Fig. 1. Graphical representation of two objective functions.

Due to the odd quarter-wave symmetric characteristic, even order harmonics become zero. Meanwhile, considering the line voltage, triplen harmonics do not need to be considered.

Therefore, the THD [8] of the line voltage can be expressed as follows:

$$\text{Line Voltage THD} = \frac{\sqrt{\sum_{n=5,7,11,13,\dots}^{\infty} V_n^2}}{V_1} * 100 \quad (2)$$

where n^{th} component can be written as:

$$V_n = \frac{4V_{dc}}{n\pi} (\cos n\alpha_1 + \cos n\alpha_2 + \ \dots + \cos n\alpha_m)$$

The prime objective of an inverter is to keep the fundamental component of the output voltage of multilevel inverter at a desired value. However, equally important is the need to keep the harmonic components in the output voltage within specified harmonic limits. Therefore, a minimization function is developed to obtain the optimized switching angles for generating a switching pattern for firing the H-bridges of multilevel inverter so that both the objectives are achieved.

The objective function to be minimized is framed as follows:

$$F(\alpha_1, \alpha_2, \dots, \alpha_m) = W_1 \times \left(1 - \frac{V_1}{V_{1max}}\right)^4 + W_2 \times \sum_{n=5,7,11,\dots}^{49} \left(\frac{V_n}{V_{1max}}\right)^2 \quad (3)$$

The condition to obtain a staircase waveform is that the switching angles should be within zero and $\pi/2$ ($0 < \alpha_1 < \alpha_2 < \dots < \alpha_m < \pi/2$). The weights W_1 and W_2 are set so that their sum is unity. To determine the optimum weights W_1 and W_2, two-objective functions are geometrically represented for different combinations of weights as given in Fig. 1. Then a set of weights is chosen so that the minimum value of the objective function, as sum of two functions, is found.

There is a wide range of algorithms available for resolving different types of optimization problems. Therefore, after selecting the optimum weights, the function is optimized using an optimization algorithm. There are many limitations

to commonly used swarm intelligence techniques such as getting trapped at local mid-optimum points. In addition, GA requires selection of too many parameters. So, there is a need for an optimization algorithm that works efficiently with a minimum of parameters.

III. Cuckoo Search Optimization Based Switching Scheme

Cuckoo search is a heuristic approach, proposed in 2009 by Xin-she Yang and Suash Deb [20], used for solving optimization problems in different fields of engineering. The number of parameters to be tuned is much smaller than other algorithms such as GA and PSO. Hence, it is possibly more capable for a wide class of the optimization procedures. The algorithm is inspired by the behavior of cuckoo birds, also known as brood parasites, that never build their own nest and lays their eggs in the nests of other host birds (of different species). Eggs in a nest represent solutions, whereas an egg of a cuckoo bird is a new solution. Normally, a cuckoo lays one egg at a time in a randomly chosen nest. The number of host nests is fixed. So, each nest has one cuckoo bird egg and remaining eggs are from the host bird. Sometimes, host birds get involved into direct conflicts with intruding cuckoos. If the host bird recognizes an egg as someone else's, they either throw it out of the nest or move to build a new nest. The probability of cuckoo's egg being recognized is p_a, and is generally fixed at 25% [21], [24]. However, if a cuckoo's egg matures, it moves to the next generation. The ability of the algorithm to maintain a balance between local and global random walks using switching parameter makes it suitable for global optimization problems. A flowchart for the optimizing switching angles being used to generate a switching pattern using Cuckoo Search is given in Fig. 2.

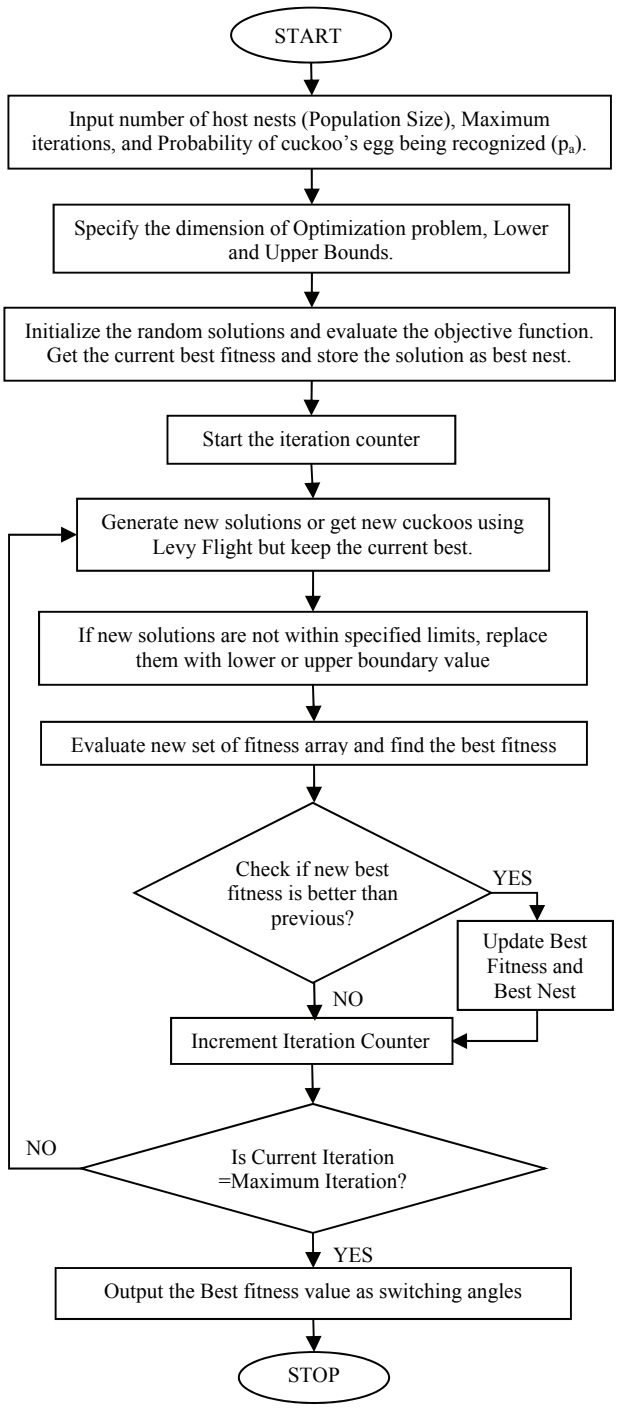


Fig. 2. Algorithm for Cuckoo Search Optimized Switching Scheme.

IV. Experimental Results and Discussion

In this paper, Cuckoo Search Algorithm is employed for the optimization of switching angles to obtain minimum harmonics and better power quality. The proposed method is implemented by developing code in the MATLAB programming environment. The obtained results are further used in SIMULINK model to observe various power quality related parameters and FFT analysis. The simulation results are validated experimentally with Five-Level CHMLI setup equipped with a FPGA controller. Different case studies are performed to substantiate the effectiveness of the Cuckoo Search Algorithm for the power quality improvement of CHMLIs.

A. Implementation and Performance of Cuckoo Search Optimization for Harmonic Minimization

A model of Five-Level CHMLI is developed in MATLAB/ Simulink software and the switching angles to fire the H-bridges of Inverter are acquired using the developed harmonic minimization function. The objective function is minimized by applying Cuckoo Search Optimization algorithm. The parameters for the population size, maximum iterations and number of runs are taken as 25, 100 and 10. The angles are found to be same, i.e. α_1=7.63 and α_2=24.52 in every run.

The value of minimization function and the optimized switching angles of five-level inverter are plotted with

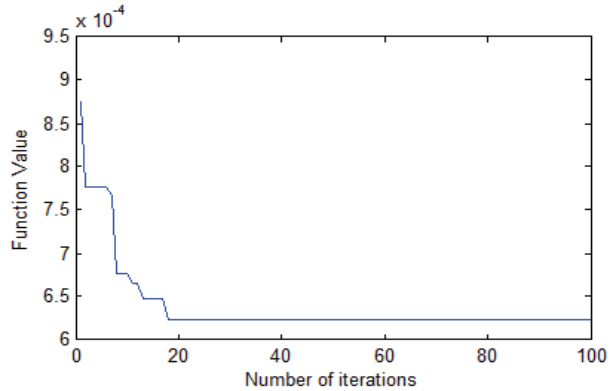


Fig. 3. Value of the minimization function with different iterations.

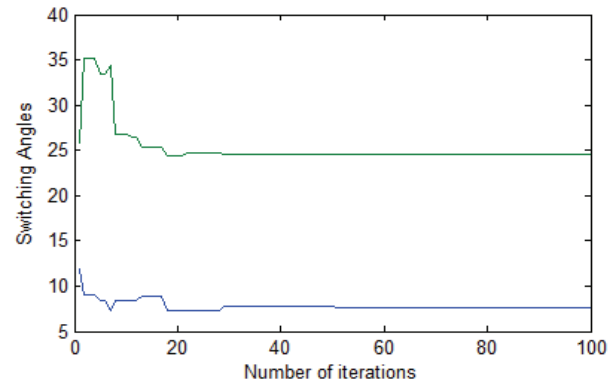


Fig. 4. Value of the Switching Angles of Five-Level Inverter with different numbers of iterations.

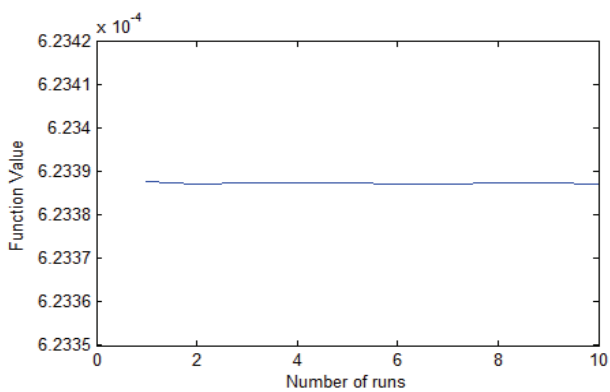


Fig. 5. Optimized Function value at different runs.

different numbers of iterations in Fig. 3 and Fig. 4, respectively. The function value during each run is same as shown in Fig. 5, therefore, the effectiveness of this algorithm is confirmed. The computational time taken by the algorithm to determine results, i.e. the switching angles is 0.7~0.9s only for 100 iterations in one run.

B. Simulation and Analysis of Five-Level Cascaded H-Bridge Inverter using SPWM Firing Scheme and Cuckoo Search Optimized Firing Scheme

Since the results of Cuckoo Search Optimization algorithm

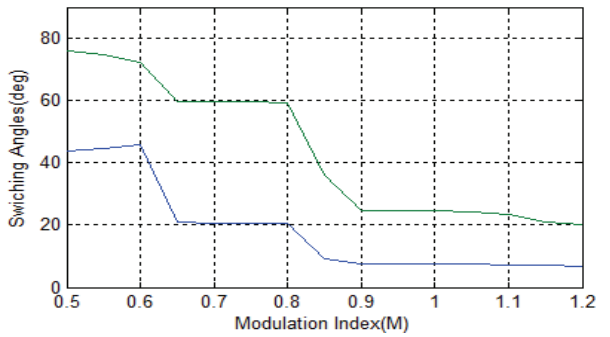


Fig. 6. Optimized value of Switching Angles at different values of the modulation index.

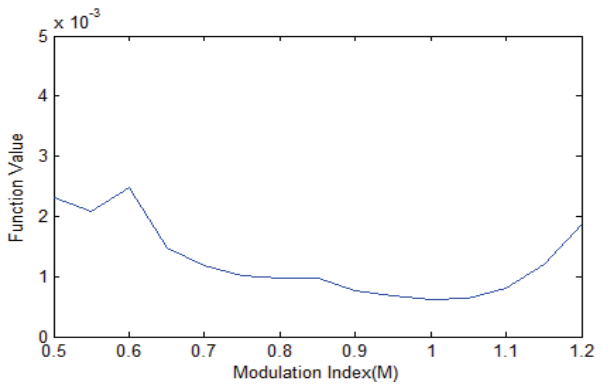


Fig. 7. Optimized Function Value at different value of Modulation Index.

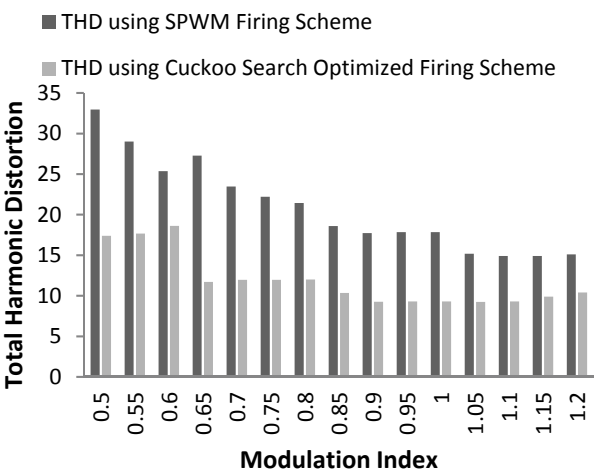


Fig. 8. Line Voltage THD using two firing schemes at different values of Modulation Index.

are same on every run, only a single run is considered for further study. The program is executed for different modulation indexes, and the optimum values of switching angles for five-level inverter are obtained and plotted in Fig. 6.

In addition, the function value with respect to the modulation index is shown in Fig. 7. The step size here is taken as 0.05. From this figure, it can be seen that the function value at every modulation index lies within 10^{-3} to 10^{-4}. Thus, the algorithm is efficient in optimizing the

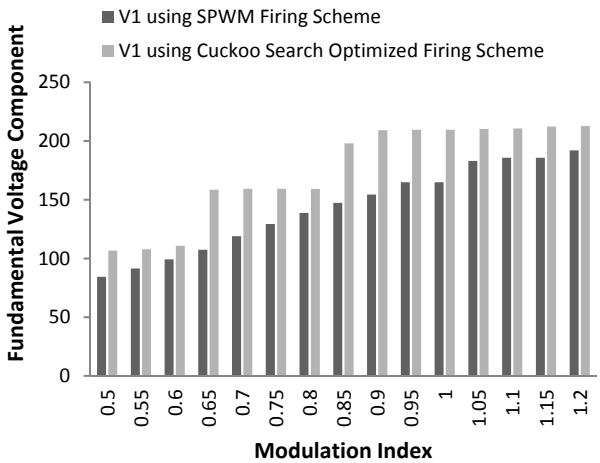


Fig. 9. Fundamental Voltage using two firing schemes at different values of Modulation Index.

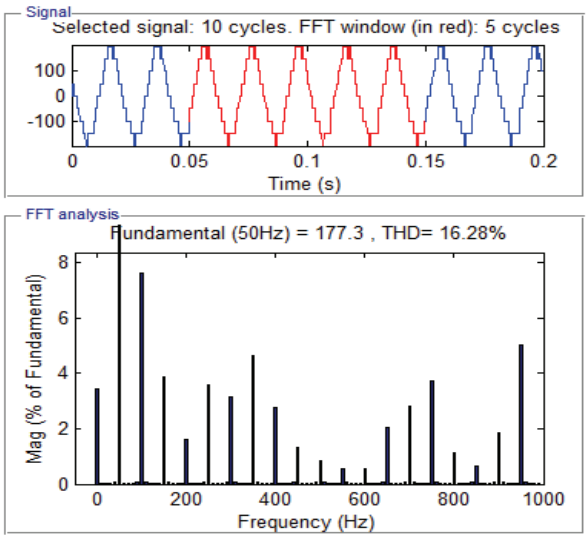


Fig. 10. FFT Analysis of Five-Level Inverter using SPWM Firing Scheme.

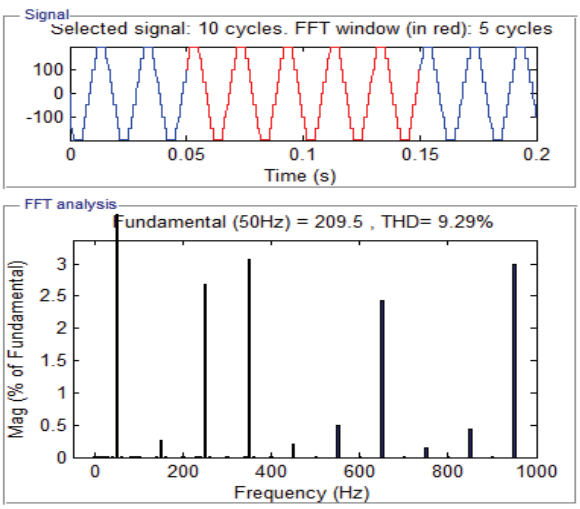


Fig. 11. FFT Analysis of Five –Level Inverter using Cuckoo Search Optimized Firing Scheme.

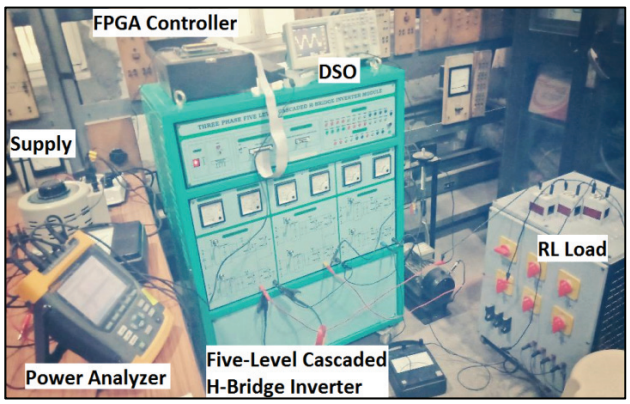


Fig. 12. Hardware prototype of FPGA Controlled Five –Level Cascaded H-Bridge Inverter.

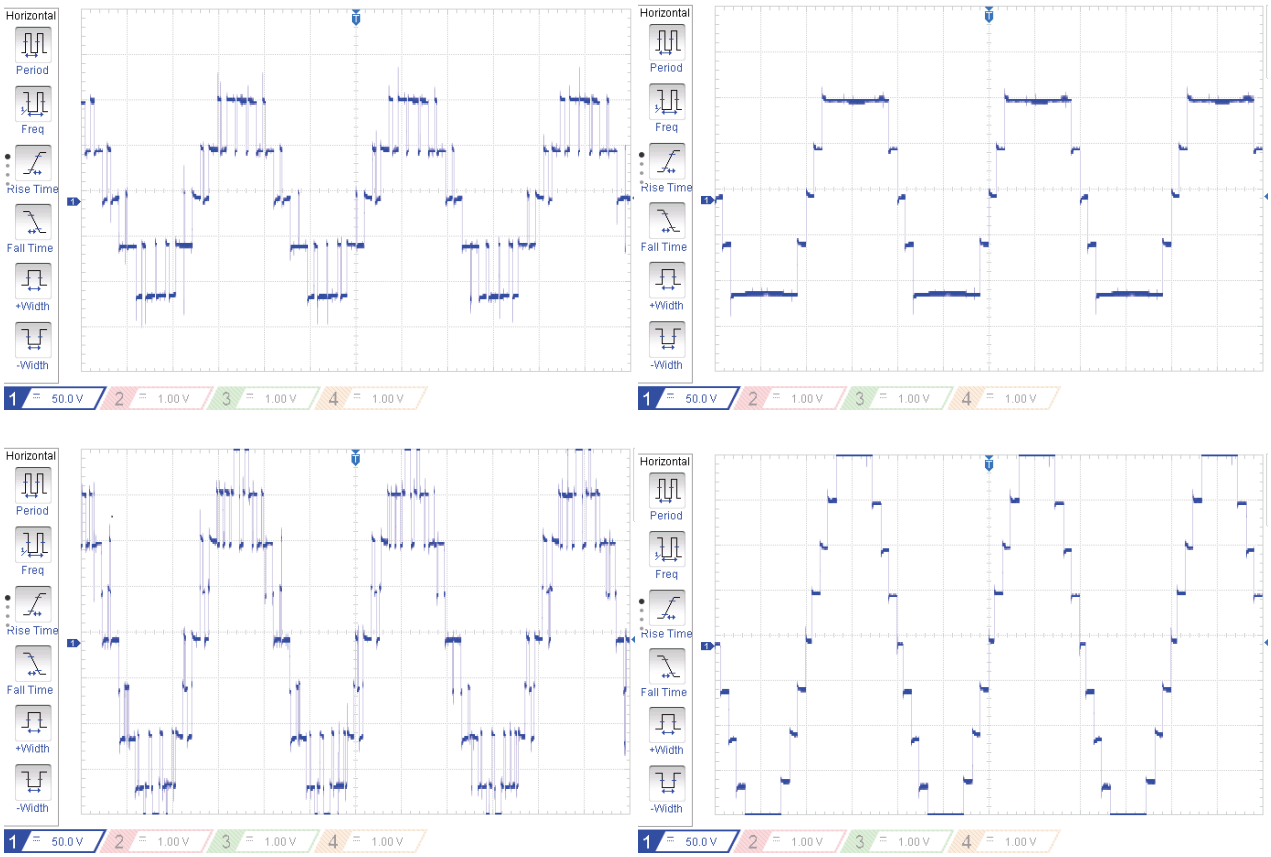
switching angles for minimum harmonics.

Different power quality related parameters such as THD and fundamental voltage values are observed. A comparison between Cuckoo Search optimized firing scheme and SPWM firing scheme is made based on these parameters. Graphical representations shown in Fig. 8 and Fig. 9 summarizes the comparison and verify the effectiveness of Cuckoo Search as THD is minimized and the fundamental voltage component is enhanced near the desired value for all of the values of modulation index. The model of Five-level inverter is simulated at m=1 using both schemes and FFT analysis is presented in Fig. 10 and 11. It can be clearly seen from the FFT analysis that THD is minimized from 16.28% with SPWM Firing Scheme and 9.29% with Cuckoo Search Optimized Firing Scheme. Also, the even-order and other inadequate harmonics are minimized.

C. Experimental Validation of FPGA Controlled Five-Level Cascaded H-Bridge Inverter

For the validation of simulation results, a hardware prototype of FPGA controller based three-phase five-level cascaded H-bridge inverter has been setup as shown in Fig. 12. A single-phase autotransformer is connected to six separate isolation transformers and rectifiers to generate six isolated DC supply for six H-bridges in the three phases of inverter. A Xilinx Spartan-6 FPGA controller is programmed to drive the gates of H-bridges using switching pattern obtained from both of the firing schemes. As switching losses are more when the switching frequency is high, and the major focus of this research is on power quality improvement, so the switching frequency for SPWM firing scheme is taken as 200Hz. A non-linear star-connected load with 300Ω, 40mH in each phase is connected to the inverter.

All the simulations and implementations are done at m=1. Experimental results of the output phase and line voltages for SPWM firing scheme and Cuckoo Search optimization based firing scheme are obtained from DSO and are shown in Fig. 13. It can be clearly seen from these figures that the waveforms obtained using Cuckoo Search optimization based firing scheme



(a) (b)

Fig. 13. Hardware output phase voltage and line voltage for two firing schemes. (a) SPWM. (b) Cuckoo Search.

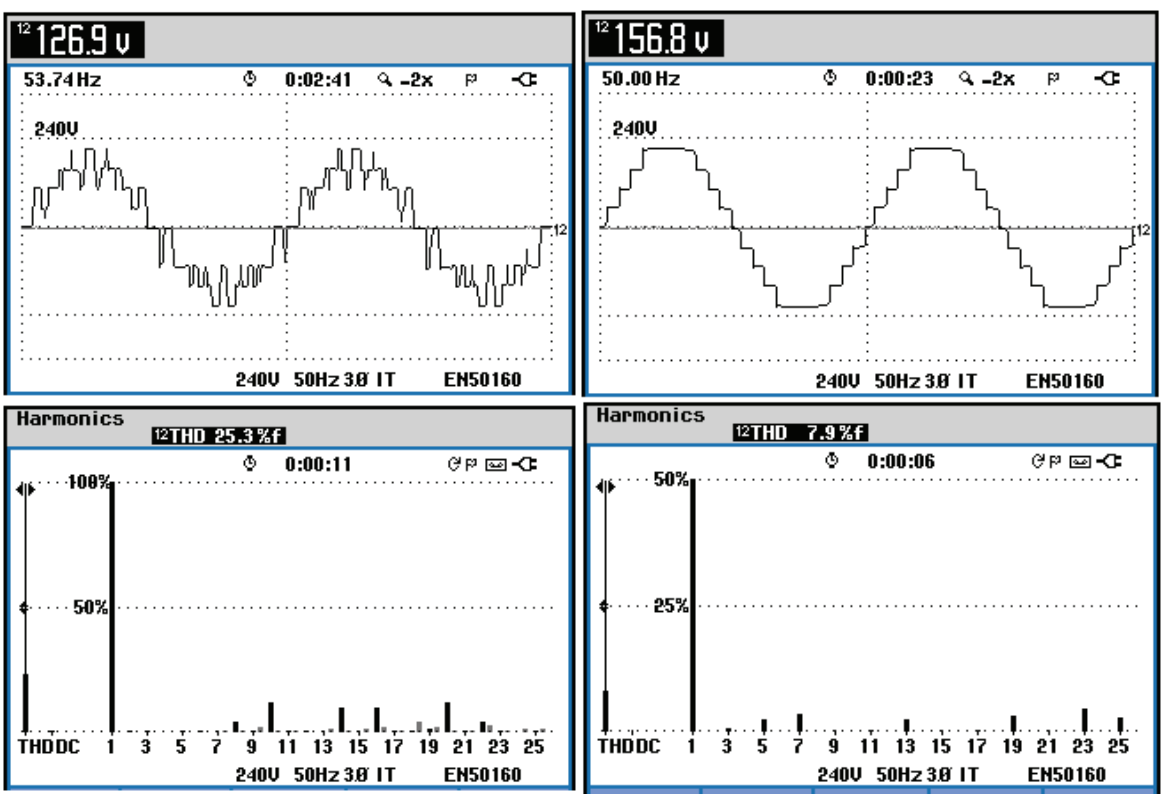


Fig. 14. Voltage and Harmonic graphs obtained from Hardware using SPWM and Cuckoo Search optimization based firing schemes.

TABLE I
VOLTAGE, CURRENT AND POWER AT THE INPUT AND OUTPUT

		SPWM Scheme	Proposed Scheme
Input Side Readings	V_{RMS} (V)	85	85
	I_{RMS} (A)	1.2	1.6
	P_{IN} (W)	65	90
Output Side Readings / phase	V_{RMS} (V)	74	85
	I_{RMS} (A)	0.2	0.3
	P_{IN} (W)	13.5	25
Total Output P_{OUT} (W)		40.5	75
Apparent Power (VA)		44.4	76.5
Reactive Power (VAR)		6.06	5.07

TABLE II
COMPARISON BETWEEN HARDWARE RESULTS OBTAINED USING SPWM AND CS OPTIMIZED FIRING SCHEMES

S.No.	Factors that assess Power Quality	Measured Parameters	SPWM Based Firing Scheme	Cuckoo Search based Optimization Scheme
1	THD	Phase Voltage THD	27.5%	23.1%
		Current THD	22.1%	21.7%
		Line Voltage THD	25.3%	7.9%
2	RMS Value	RMS Value of Fundamental	123.2 V	156.0 V
3	Peak Value	Peak value of Line Voltage	210.1 V	214 V
4	Crest Factor	CF	1.70	1.37
5	Even Order Harmonics	2^{nd} Harmonic	0.6%	0
		4^{th} Harmonic	0.3%	0
		6^{th} Harmonic	0.3%	0
		8^{th} Harmonic	0.4%	0
		10^{th} Harmonic	0.6%	0
		12^{th} Harmonic	0.5%	0
		14^{th} Harmonic	0.3%	0
		16^{th} Harmonic	0.7%	0
		18^{th} Harmonic	0.5%	0
6	Lower Order Harmonics or Distortion Factor	3^{rd} Harmonic	0.5%	0.6
		5^{th} Harmonic	0.5%	2.1
		7^{th} Harmonic	3.9%	3.4
		9^{th} Harmonic	12.1%	0
		11^{th} Harmonic	0.3%	0.4
		13^{th} Harmonic	9.7%	2.4
		15^{th} Harmonic	9.8%	0
		17^{th} Harmonic	0.5%	0.3
		19^{th} Harmonic	1.3%	3.1
7	Reactive Power	Q (VAR)	6.06	5.07
8	Power Factor	PF	0.91	0.98
9	Power Loss	Input-Output (W)	24.5	15
10	Efficiency	η (%)	62.3	83.3

are much better than those obtained with SPWM firing scheme. A THD analysis is done using power analyzer, line voltage waveforms and Harmonic graphs for both the firing schemes are shown in Fig. 14. The obtained experimental results support the simulation since they are found to be comparable to the simulated results shown in Fig. 11. To provide a clear vision of the power quality, a detailed analysis and comparison of the power quality assessment of SPWM and proposed CS Optimized firing scheme is done.

Observations made using an ammeter, voltmeter and wattmeter connected to the hardware setup are shown in Table I. These values are further used to calculate active power, apparent power, reactive power, power factor, power loss, and efficiency. For better understanding, a comparison between experimental results obtained using SPWM Firing Scheme and CS Optimized Firing Scheme is presented in

Table II.

From the tabulated results, it can be seen that THD of the line voltage is measured as 7.9% using CS optimization based firing scheme whereas it is 25.3% using SPWM firing scheme. Also, all the power quality parameters, other than harmonics, such as the reactive power drawn by the circuit, power factor, and efficiency of multilevel inverter have improved. Thus, it is obvious that the proposed method is efficient in improving the power quality and minimizing the harmonics.

V. CONCLUSIONS

In this paper, a minimization function is developed as the weighted sum of two main objectives, i.e. minimum harmonics and desired value of fundamental voltage output, so as to obtain the optimized switching angles for generating the switching pattern for firing H-bridges of multilevel inverter. The observed results verify the efficiency of Cuckoo Search algorithm based optimization in determining the optimum switching angles. Since there is only a single parameter ρ_a required in Cuckoo Search, apart from the population size, it is easy to implement. This paper presents a SPWM based firing scheme with a reduced switching frequency equal to 200Hz and Cuckoo Search optimization based firing scheme, to generate switching pattern for firing the H-bridges of five-level cascaded H-bridge inverter. Simulations have been carried out in MATLAB/Simulink with a nonlinear load, and a comparison on the basis of different performance parameters has been done. At all of the values of modulation index, THD and fundamental voltage component are observed to be better with CS optimized firing scheme. A FFT analysis confirms that the even order harmonics are zero and that the other lower order harmonics are controlled within allowable limits to comply with IEEE 519-1992 harmonic guidelines. The computational time required for determining the switching angles is only 0.7~ 0.9s. The algorithm can be easily implemented for an inverter with any number of levels. Experimental results obtained with hardware prototype are presented for validation of simulation results. The two firing schemes are implemented experimentally and the obtained voltage waveform and THD analysis results are found to be similar to the simulation results in both cases. The power factor has been increased from 0.91 to 0.98 and the efficiency has improved by 20%. Hence, it is confirmed that CS optimized switching scheme provides a better switching pattern to achieve the minimum THD and a better quality voltage output.

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Deepshikha Singla was born in India, in 1986. She received her Degree of Bachelor of Engineering in Electronics and Instrumentation Engineering in 2007. and her Master of Technology in Electrical Engineering (Power System and Drives) from the YMCA University of Science and Technology (YMCAUST), Faridabad, India, in 2011, where she is presently working towards her Ph.D. degree. She has five years of teaching experience at the Manav Rachna International University (MRIU), Faridabad, India. She is presently working as an Assistant Professor in the Department of Electrical Engineering, YMCAUST. Her current research interests include power quality improvements in multilevel inverters.

P.R. Sharma was born in India, in 1966. He received his Degree of Bachelor of Engineering in Electrical Engineering from Punjab University, Chandigarh, India, in 1988; Degree of Master of Technology in Electrical Engineering (Power System) from Regional Engineering College, Kurukshetra, India, in 1990; and his Ph.D. degree from Maharshi Dayanand University, Rohtak, India in 2005. He began his carrier in industry. He has a great deal of experience both in industry and teaching. He is presently working as Professor of Electrical Engineering in Department of Electrical and Electronics Engineering in YMCA University of Science and Technology, Faridabad, India. His current research interests include Optimal Location and Coordinated Control of FACTS Devices in Power System. He has over 92 publications in international journals and conference proceedings. He is a reviewer of IET, IE (INDIA), TUBITAK, IJEST and IEEE International conferences.