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Load and Capacitor Stacking Topologies for DC-DC Step Down Conversion

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Abstract

This paper presents two voltage domain stacking topologies for powering integrated digital loads such as multiprocessors or 3D integrated circuits. Pairs of loads and capacitors are connected in series to form a stack of voltage domains. The voltage is balanced by switching the position of the capacitors in one case and the position of the loads in the other case. This method makes the voltage regulation robust to large differential load power consumption. The first configuration can be named the load stacking topology. The second configuration can be named the capacitor stacking topology. This paper aims at proposing and comparing these two topologies. Models of both topologies and a switching scheme are presented. The behavior, control scheme, losses and overall performance are analyzed and compared theoretically in simulation and experiments. Experimental results show that the capacitor stacking topology has better performance with a 30% voltage ripple reduction.

Key words: Stacked voltage domains, Switched-capacitor converter

I. INTRODUCTION

Integrated circuits are becoming smaller and smaller while hosting ever increasing digital circuitry in one chip, which reduces both the cost and size of the chip. The limited power ratings of a chip make the power management challenging, which leads to adding complex cooling systems [1] or clamping the computational capability of the digital load. Taking into consideration the desired cost and performance, another solution is a reduction of the power supply voltage, with the digital load power consumption being a function of the square of the voltage. One of the International Technology Roadmap for Semiconductors (ITRS) targets is to achieve a 0.6V voltage supply by 2024. Furthermore, other trends include the increase of digital loads, processors becoming multicore [2] for an increased computing capability and data centers using thousands of those digital loads [3]. Finally, the recent development of 3D integrated circuits is resulting in new challenges in power management [4].

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This represents a very large challenge for power supply architectures designed for a very small voltage and a very high current. The overall efficiency of the power conversion stage is decreased. First of all, a higher current can lead to higher losses across the distribution lines. Secondly, from the AC line to the processor, a large number of power conversion stages must be installed to cope with the required very high conversion ratio [6].

A solution is to put digital loads in series and was first introduced in [5]. Fig. 1 shows both cases where the loads are put in parallel and in series. In the case of series load stacking, one to several power conversion stages can be removed. For the upstream converter, the advantage is a reduced output current, which reduces the conduction and switching losses [6]. This leads to a more efficient power stage. This method is called the stacked voltage domains technique. However, an uncontrolled current leads to a highly unregulated voltage across the loads. Two solutions exist to control this current [6].

The first solution is to control the overall load behavior. Several load management techniques exist at the software and firmware levels [2], [6], [7]. The use of a scheduler and clock rates are two common methods of dealing with this issue. The second solution is at the hardware and voltage regulator level. A regulator at each level regulates the voltage difference due to mismatched current consumption. These regulators, called

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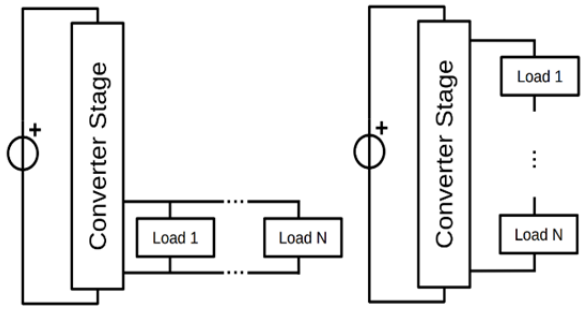
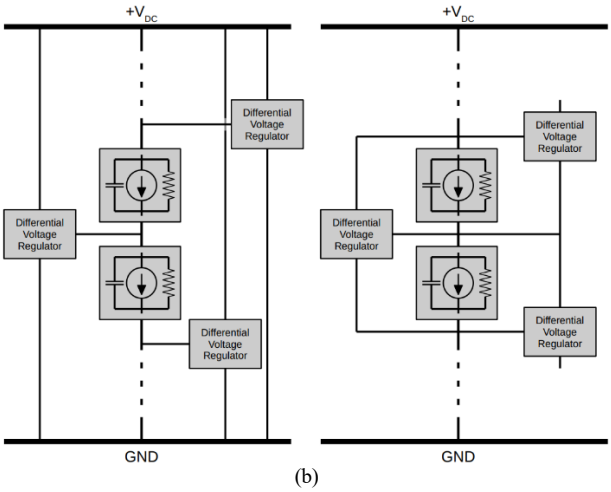


(a) (b)

Fig. 1. Load stacking. (a) Parallel. (b) Series.



(b)

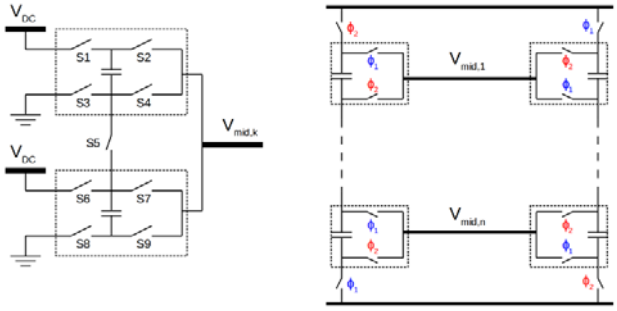
Fig. 2. Stacked loads with a differential voltage regulator. (a) Power line connections of the inputs. (b) Nearest voltage points connection of the inputs.

differential voltage regulators in [6] can be designed using topologies developed for photovoltaic and batteries applications [8]. Since they only regulate a portion of the overall power, an integration should be considered for a better performance.

Two configurations are possible, as presented in Fig. 2. The difference lies in the voltage inputs. They are either connected to the power lines or to the nearest upper and lower voltage points. Both technologies are considered in [6], [9].

For the differential voltage regulator, three technologies are possible [6]. The first one is a linear regulator. However, its efficiency at high current does not makes it an optimal design solution. The second one is an inductive step-down converter topology such as a buck converter, flying capacitor [11] or ladder type topologies [12]. However, the inductance is very difficult to integrate. The third one, the switched-capacitor converter type, can be integrated. Among the existing switched-capacitor converter topologies, the flying capacitor converter [10] and the switched-capacitor ladder type [9] have been considered.

In this paper, two new switched-capacitor converter topologies are proposed. They are compared with each other and evaluated in comparison to existing topologies. In section 2, the existing topologies are reviewed and the new topology is introduced. Two models are presented and a switching scheme is described at the end of the section. Section 3 focuses on the simulation results. Finally, section 4 presents some conclusions.



(a) (b)

Fig. 3. Existing topologies. (a) Flying capacitor. (b) Switched-capacitor ladder converter.

II. Stacking Topologies

A. Existing Topologies

The first topology, the flying capacitor converter topology was proposed in [10], and one leg is shown in Fig 3(a). Each flying capacitor converter acts as a voltage regulator as in Fig. 2(a). Therefore, the voltage rating of the switches must be large enough to withstand the voltage mismatch between the power lines and the output node. Another problem is that the conversion ratio is limited to fixed values i.e. ½, ⅓ and ⅔ limiting the number of stacked voltage domains to 3.

The second topology, the ladder converter was presented in [9]. It is combined with the flying capacitor topology to cope with the potentially high current mismatch, and is pictured in Fig 3(b). The control process is to alternate between two phases, two switch configurations, in order to maintain the voltage level. However, this technique leads to significant capacitive losses in case of a large voltage mismatch between the left-side and right-side capacitors. Furthermore, voltage control is not independent due to the fixed load and capacitor positions.

B. Proposed Topology

In the proposed topologies, capacitors and loads are connected in series in pairs, one being the moving part and the other being the fixed part. At each switching period, the moving parts are reshuffled according to a switching scheme. As shown in Fig. 4, when the fixed parts are the capacitors, the topology is named the capacitor stacking topology; and when the loads are the fixed parts, the topology is named the load stacking topology.

In terms of the number of elements, for N voltage domains, N capacitors and $2xN^2$ switches are needed. Between the capacitor and the switch, at the same voltage ratings, the

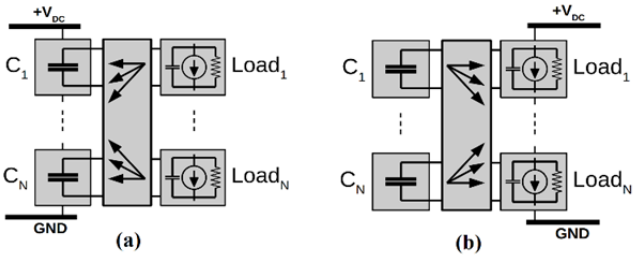


Fig. 4. Proposed topologies. (a) Capacitor stacking. (b) Load stacking.

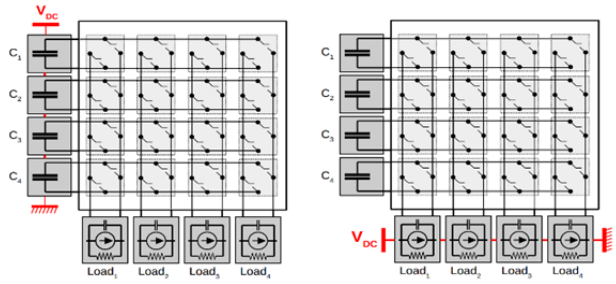


Fig. 5. Topology implementations. (a) Capacitor stacking topology for 4 voltage domains. (b) Load stacking topology for 4 voltage domains.

TABLE I
COMPARISON BETWEEN STACKED VOLTAGE DOMAINS TOPOLOGIES

Topology	Flying Capacitor [10]	Ladder Converter [9]	Proposed Topology
Number of transistors	9xN	4xN+4	$2xN^2$
Number of Capacitors	2xN	2xN	N
Voltage Rating of Transistors	High	Low	Low
Voltage Rating of Capacitors	High	Low	Low
Voltage domains	≤ 3	∞	∞
Voltage Conversion ratio	{½, ⅓, ⅔ }	$\{\frac{1}{N}, \dots, \frac{1-N}{N}\}$	$\{\frac{1}{N}, \dots, \frac{1-N}{N}\}$

hardest part to integrate is the capacitor. Therefore, this topology may have a significant advantage for integration when compared to [9], which uses at least 2xN capacitors for each ladder converter unit. In addition, the required power rating of the capacitor is very small since it switches at a very low voltage, ensuring an even easier integration. Secondly, with N! possible switch combinations, the ability to freely place the moving part in each period is another advantage of this topology. This ensures independence in the control of the voltage domains. Their implementation is presented in Fig. 5 with the use of a matrix of bidirectional switches to connect the capacitors and loads. Table I summarizes the advantages and drawbacks of the existing and proposed topologies.

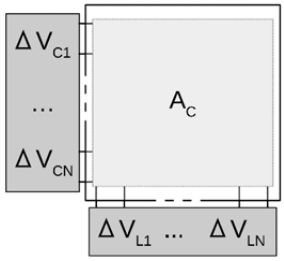


Fig. 6. Matrix model of the converter.

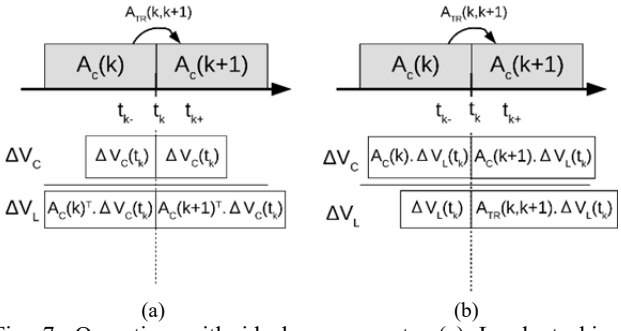


Fig. 7. Operation with ideal components. (a) Load stacking topology. (b) Capacitor stacking topology.

C. Model I - Basic Model

To introduce the converter, the simple, idealized model shown in Fig. 6 is used to link the load and capacitor voltages following Eq. (1).

$$\begin{cases}\Delta V_C = A_C \cdot \Delta V_L \\ \Delta V_L = {A_C}^{-1} \cdot \Delta V_C = {A_C}^{T} \cdot \Delta V_C\end{cases} \quad (1)$$

where ΔV_C is the vector of the $\Delta V_{c,j}$ differential capacitor voltages, ΔV_L is the vector of the $\Delta V_{L,j}$ differential load voltages, and A_C is the configuration matrix. Note that A_C is orthogonal.

The ideal case for the topology should be considered, where the capacitors have no equivalent series resistance and the load is an ideal current source. In each time period, the configuration matrix A_C changes. This can be described by the Eq. (2).

$$\begin{cases}\Delta V_C(k-1) = A_C(k-1) \cdot \Delta V_L(k-1) \\ \Delta V_C(k) = A_C(k) \cdot \Delta V_L(k)\end{cases} \quad (2)$$

The operation of the voltage variation at the transition is described in Fig. 7 for both topologies. For the load stacking topology, as presented in Fig. 7(a), the load voltage is sensed. At the transition, the capacitor voltage is maintained. The following equation is obtained:

$$\begin{cases}\Delta V_L(t_{k-}) = \Delta V_L(k) = A_C(k-1)^T \cdot \Delta V_C(t_{k-}) \\ \Delta V_L(t_{k+}) = A_C(k)^T \cdot \Delta V_C(t_{k+}) \\ \Delta V_C(t_{k+}) = \Delta V_C(t_{k-}) = \Delta V_C(k) = A_C(k-1) \cdot \Delta V_L(k)\end{cases} \quad (3)$$

which leads to a better definition of $V_L(t_{k+})$:

$$\begin{aligned}\Delta V_L(t_{k+}) &= A_C(k)^T \cdot A_C(k-1) \cdot \Delta V_L(k) \\ &= A_{TR}(k-1,k) \cdot \Delta V_L(k)\end{aligned} \quad (4)$$

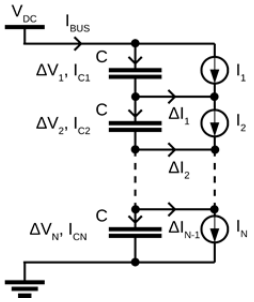


Fig. 8. Electric diagram for model I.

where A_{TR} is called the transition matrix.

For the capacitor stacking topology shown in Fig. 7(b), before the commutation, as shown in Eq. (5), the capacitor voltage vector is equal to its sensed value and the load voltage vector is a reconfiguration of the capacitor voltage vector as in Eq. (2). At the transition, the capacitor voltages and load voltages are reconfigured. After the transition, the new load voltages are a reconfigured version of the loads. The new vectors are presented in Eq. (5).

$$\begin{cases} \Delta V_L(t_{k-}) = A_C(k-1)^T \cdot \Delta V_C(k) \\ \Delta V_L(t_{k+}) = A_C(k)^T \cdot \Delta V_C(k) \\ \Delta V_C(t_{k+}) = \Delta V_C(t_{k-}) = \Delta V_C(k) \end{cases} \tag{5}$$

When the system is in a specific configuration, it can be represented by the diagram in Fig. 8. It is possible to compute the voltage deviation based on the load currents. First, Eq. 6 can be written as follows:

$$\begin{cases} I_{C1} - I_{C2} = C \cdot \dfrac{d\Delta V_1}{dt} - C \cdot \dfrac{d\Delta V_2}{dt} = I_2 - I_1 \\ I_{C2} - I_{C3} = C \cdot \dfrac{d\Delta V_2}{dt} - C \cdot \dfrac{d\Delta V_3}{dt} = I_3 - I_2 \\ \cdots \\ I_{C,n-1} - I_{C,n} = C \cdot \dfrac{d\Delta V_{n-1}}{dt} - C \cdot \dfrac{d\Delta V_n}{dt} = I_n - I_{n-1} \end{cases} \tag{6}$$

which can also be represented as:

$$\begin{cases} \mathrm{C} \cdot \mathrm{A} \cdot \dfrac{\mathrm{d}\Delta V}{\mathrm{dt}} = \begin{bmatrix} \Delta I \\ 0 \end{bmatrix} with\ A = \begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & 1 & -1 \\ 1 & \cdots & \cdots & \cdots & 1 \end{bmatrix} \\ \Delta I = B \cdot I \end{cases} \tag{7}$$

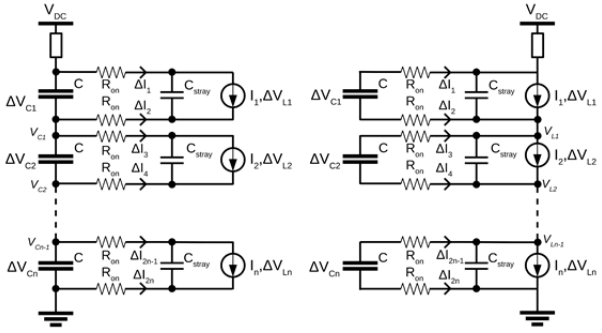
$$\text{and } \mathrm{B} = \begin{bmatrix} -1 & 1 & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & -1 & 1 \end{bmatrix}$$

where $\frac{d\Delta V}{dt}$ is the differential voltage derivative vector of the fixed part ΔV_C or ΔV_L, and ΔI is the current difference vector.

Thus, from Eq. 7, the voltage deviation can be represented by the following equation.

$$\frac{\mathrm{d}\Delta \mathrm{V}}{\mathrm{dt}} = \frac{1}{C} \cdot A^{-1} \cdot \begin{bmatrix} B \\ 0 \end{bmatrix} \cdot I = -\frac{1}{C} \cdot \frac{1}{n} \cdot \begin{bmatrix} n-1 & -1 & \cdots & -1 \\ -1 & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & -1 \\ -1 & \cdots & -1 & n-1 \end{bmatrix} \cdot I \tag{8}$$

If the configuration matrix is included, the following final equations for the system can be obtained.



(a) (b)

Fig. 9. Electric diagrams for model II. (a) Capacitor stacking topology. (b) Load stacking topology.

For the capacitor stacking topology:

$$\begin{cases} \Delta V_C(t) = \Delta V_C(t_k) + \dfrac{1}{C} \cdot A^{-1} \cdot \begin{bmatrix} B \\ 0 \end{bmatrix} \cdot A_C(k) \cdot I \cdot (t - t_k) \\ \Delta V_L(t) = \mathrm{A_C(k)^T} \cdot \Delta V_C(t) \end{cases} \tag{9}$$

For the load stacking topology:

$$\begin{cases} \Delta V_C(t) = A_C(\mathrm{k}) \cdot \Delta V_L(t) \\ \Delta V_L(t) = A_{TR}(k-1,k) \cdot \Delta V_L(t_k) \\ \qquad + \dfrac{1}{C} \cdot A^{-1} \cdot \begin{bmatrix} B \\ 0 \end{bmatrix} \cdot I \cdot (t - t_k) \end{cases} \tag{10}$$

D. Model II - Improved Model

The topology contains elements that are non-ideal and they will modify the voltage time transients. The real switches used have a time delay in the commutation. In such a case, a larger time delay, $t_{deadtime}$, time during which the load and capacitor are disconnected, should be defined to prevent short-circuits. They also have an on-resistance R_{ON}. The load can be modeled with a small stray capacitor C_{stray}. The previous conversion stage can be represented by a constant voltage source connected to the system via an inductive bus L_{BUS}.

Thus, the electric diagram is different from model I, and is represented in Fig. 9. It can be observed that there is a different time transient at the commutation than for the ideal case of Fig. 7. The operations for the load stacking topology and the voltage stacking topology are presented in the Fig. 10 and Fig. 11, respectively.

At t_k, the load voltages are sensed in the load stacking topology case, and capacitor voltages are sensed in the capacitor stacking topology case.

During phase I – $[t_k;t_k+t_{deadtime}]$, the capacitors and loads are disconnected. In the case of the load stacking topology, the capacitor voltage is maintained at its t_k value. However, the load and its stray capacitor in parallel follow Eq. (8), C_{stray} replacing C. Therefore, the voltage derivative is much larger creating a non-neglectable voltage drop or spike. In the capacitor stacking topology, the stray capacitor is the source for the totality of the load current. Thus, the voltage drop

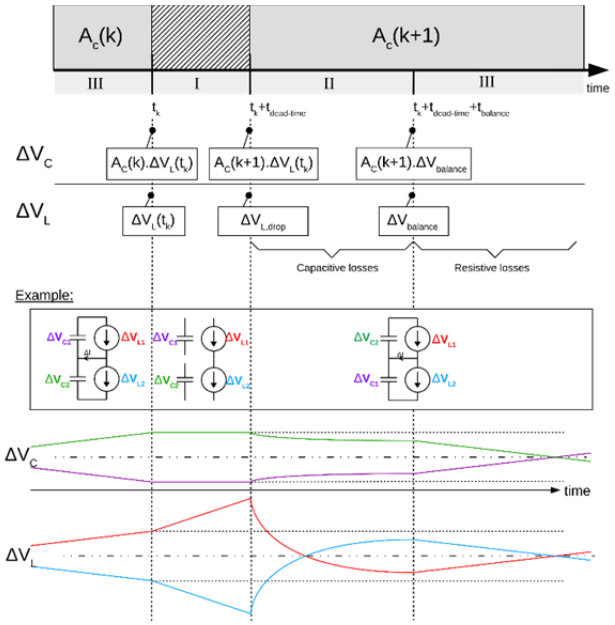


Fig. 10. Operation for the load stacking topology.

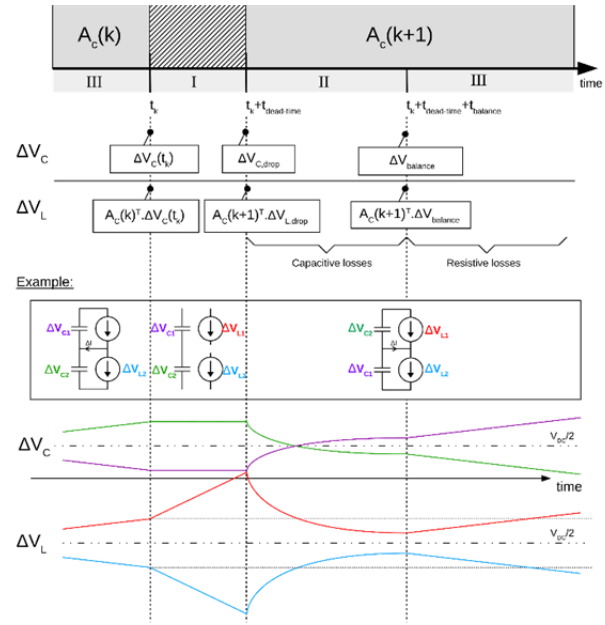


Fig. 11. Operation for the capacitor stacking topology.

might be much bigger than that for the load stacking topology. Meanwhile, the capacitor voltages are steady.

During phase II – $[t_k+t_{deadtime};t_k+t_{deadtime}+t_{balance}]$, the loads and capacitors are reconnected. In both topologies, the capacitors and loads are first rebalancing due to the C_{stray} and C voltage differences. The balancing time $t_{balance}$ is approximately 3 times the time constant $\tau = R_{ON}.(C+C_{stray})/N$ and the balanced voltage is given by Eq. (9).

$$\Delta V_{balance} = \frac{C \cdot \Delta V_C(\mathrm{t_{deadtime}}) + C_{stray} \cdot \Delta V_L(t_{deadtime})}{C + C_{stray}} \quad (11)$$

During phase III – $[t_k+t_{deadtime}+t_{balance};t_{k+1}]$, the loads and capacitor voltages are equal. In addition, the load voltages change constantly following Eq. (8). The dominating losses are then the resistive losses inside the switches.

Two main sources of losses have to be considered in the topology: the capacitive and the resistive losses. The capacitive losses occur in phase II and the resistive losses occur in phase III.

The capacitive losses occur when two capacitors with unequal voltages are connected together. They occur during the phase II – $[t_k+t_{deadtime};t_k+t_{deadtime}+t_{balance}]$ period, between the interconnected stray and main capacitors.

In the case of the load stacking topology, the losses are:

$$P_{losses,cap} = \frac{1}{2} \cdot \frac{C \cdot C_{stray}}{C + C_{stray}} \cdot \left(\mathrm{A_C}(k).V_L(k) - V_{L,drop}\right)^T \cdot \left(\mathrm{A_C}(k).V_L(k) - V_{L,drop}\right) \quad (12)$$

In the case of the capacitor stacking topology, the losses are:

$$P_{losses,cap} = \frac{1}{2} \cdot \frac{C \cdot C_{stray}}{C + C_{stray}} \cdot \left(\Delta V_C(k) - A_C(k)^T \cdot \Delta V_{L,drop}\right)^T \cdot \left(\Delta V_C(k) - A_C(k)^T \cdot \Delta V_{L,drop}\right) \quad (13)$$

During phase III – $[t_k+t_{deadtime}+t_{balance};\ t_{k+1}]$, resistive losses occur since the switches are not ideal. Fig. 9 can be used as a model. In such a case the losses are:

$$P_{losses,res} = \sum_{j=1}^{N-1} R_{ON} \cdot \Delta I_j(k)^2 = R_{ON} \cdot \Delta I(k)^T \cdot \Delta I(k) \quad (14)$$

E. Switching Schemes

To regulate the intermediate voltages, it is important to change the configuration following a stabilizing commutation strategy. These strategies are called switching schemes.

A simple and stable scheme period is composed of N phases for N voltage domains, where each phase is associated with a matrix configuration. The rolling scheme is a simple and effective switching strategy. At the switching time, the moving part associated to the j^{th} fixed unit is associated to the $(j\text{-}1)^{th}$ or $(j\text{+}1)^{th}$ fixed unit for the negative or positive rolling, respectively.

Therefore, $A_{TR}(k-1,k)$ is fixed, which makes the transition simple. In addition, its value can be found in Table II. To obtain the following $A_C(k)$, based on the previous configuration matrix $A_C(k\text{-}1)$:

$$\begin{aligned} A_{TR}(k,k-1) &= A_C(k)^T \cdot A_C(k-1) \\ A_C(k) &= (A_{TR}(k,k-1) \cdot A_C(k-1)^T)^T \\ &= A_C(\mathrm{k}-1) \cdot A_{TR}(k,k-1)^T \end{aligned} \quad (15)$$

This new configuration matrix can be applied to both of the proposed topologies.

TABLE II
A_{TR}(K-1,K) FOR THE ROLLING SCHEME

	Positive rolling	Negative Rolling
$A_{TR}(k-1,k)$	$\begin{bmatrix} 0 & \cdots & 0 & 1 \\ 1 & 0 & \cdots & 0 \\ 0 & \ddots & \ddots & \vdots \\ \vdots & \ddots & 1 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 1 & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & 1 \\ 1 & 0 & \cdots & 0 \end{bmatrix}$

TABLE III
SIMULATION VALUES

Element	Value
$+V_{DC}$	3.3V
f_{sw}	10kHz and 100kHz
$t_{deadtime}$	200ns
R_{ON}	120mΩ
C	47μF
C_{stray}	4.7μF
L_{bus}	1nH

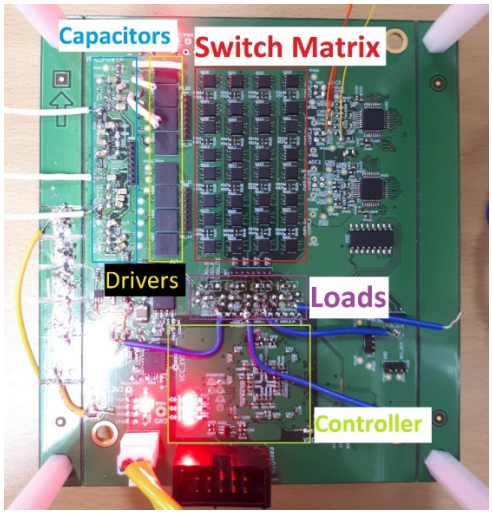


Fig. 12. Control Board for 4 voltage domains.

III. SIMULATION AND EXPERIMENTAL RESULTS

In order to properly observe the behavior of the loads, simulations and experiments are conducted with 4 voltage domains, and the bus voltage is 3.3V. The switching frequency f_{sw} is set to 10kHz and 100kHz to observe various transients. Based on the experimental setup components, the deadtime $t_{deadtime}$ is set as 200ns. The on-resistance R_{ON} is 120mΩ. In addtion, the capacitor C and stray the capacitors C_{stray} are set as 47 and 4.7μF, with the main capacitor capacitance being much larger than the stray capacitor capacitance to maintain a voltage for large current differentials. Considering that the previous stage output impedance is small with regard to the line inductance, L_{bus}, the output impedance is mainly inductive. In addition, the line inductance between the previous conversion stage and the system is set as 1nF. They can be found in Table III.

The simulations are done with PLECS and the experiments are done with the board shown in Fig. 12.

TABLE IV
SIMULATION CURRENT SETS

$I_{POSITION}$	Set A	Set B	Set C	Set D
I_1	0.176A	0.176	0.083	0.083
I_2	0.375A	0.200	0.176	0.11
I_3	0.121A	0.137	0.055	0.075
I_4	0.176A	0.176	0.083	0.083
ΔI_{MIN}	0.055	0.024	0.028	0.007
ΔI_{MAX}	0.200	0.060	0.121	0.035

For the choice of currents, defined in Table IV, the experiments show that the system starts to become unstable at a few hundreds of milli amperes due to limitations in the experimental equipment. Thus, the currents sets are chosen at the limit. The base currents are fixed for all sets and are arbitrary attributed to I_1 and I_4. Sets A and B have large base currents while sets C and D have a 50% smaller base current. In Set A and Set C, it is chosen to have a very large current difference of more than two times the minimum current. For instance, if the highest current difference is 0.176A-0.055A= 0.121A, that is around 2.2 times the I_3, Set A current (0.055A). Set B and Set D are chosen to have a limited current difference. The maximum current difference is only 40% of the base current.

A. Load Stacking Topology

The load stacking topology model is tested using simulation and experimental setups with the rolling switching scheme presented in the section 2.E, and the Table III set of currents. Plots of the simulations for the 4 load voltages and the 4 capacitor voltages can be seen in Fig. 13 and Fig. 14. A plot of the experimental results for the 4 load voltages can be seen in Fig. 17.

Phase I occurs during [340μs; 340.2μs] with the load voltage increasing during the [t_k; t_k+$t_{deadtime}$] period and the capacitor voltage staying constant. Then, phase II of capacitor balancing is seen during the [t_k+$t_{deadtime}$; t_k+$t_{deadtime}$+$t_{balancing}$] period. In the simulation [340.2μs; 343μs], and in the experiments [-0.50μs; 3.1μs]. $t_{balancing}$ is around 2.8μs for the simulation and 2.6μs and the constant time τ=2.R_{ON}.C//C_{stray}=1.025μs. Thus, the theoretical $t_{balancing}$ ≈3.τ=3.1μs is similar to both the simulated and the experimental ones. In phase III, the linear voltage deviation can be clearly seen. Therefore, the model defined in Section 2.D. is validated.

B. Capacitor Stacking Topology

The topology model is validated using the simulation setup previously described, the rolling switching scheme presented in section 2.E. and the Table III set of currents. Plots of the 4 load voltages and the 4 capacitor voltages can be seen in Fig. 13 and Fig. 14, respectively. A plot of the experimental results for the 4 load voltages can be seen in Fig. 18.

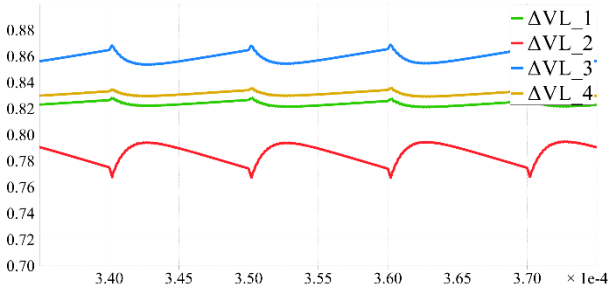


Fig. 13. Differential load voltages of a 4 load system simulation in the load stacking topology using the rolling scheme at 100kHz with the Table III Set A currents.

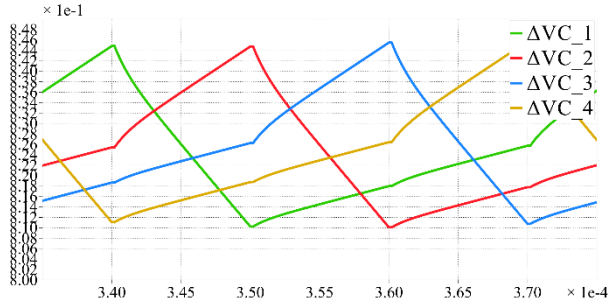


Fig. 14. Differential capacitor voltages of a 4 load system simulation in the load stacking topology using the rolling scheme at 100kHz with the Table III Set A currents.

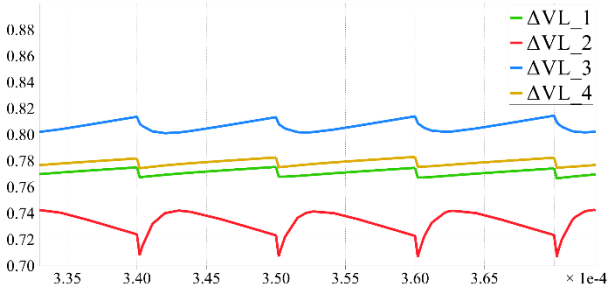


Fig. 15. Differential load voltages of a 4 load system simulation in the capacitor stacking topology using the rolling scheme at 100kHz with the Table III Set A currents.

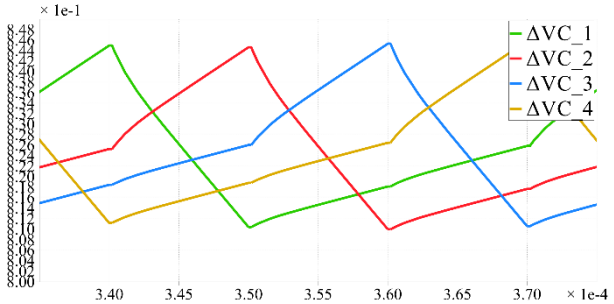


Fig. 16. Differential capacitor voltages of a 4 load system simulation in the capacitor stacking topology using the rolling scheme at 100kHz with the Table III Set A currents.

In phase I at [340µs; 340.2µs], the voltage in the loads drops but the voltage in the capacitor is changed. Phase II occurs at

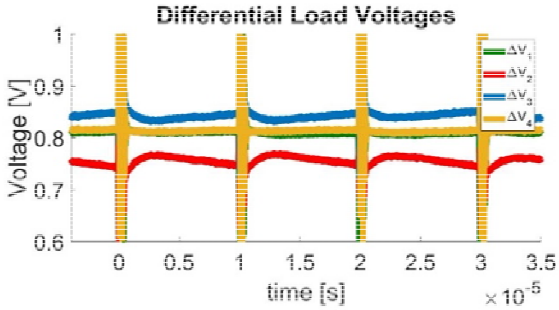


Fig. 17. Differential load voltage waveforms of a 4 loads system in a load stacking topology using the rolling scheme at 100kHz with Table III Set A of currents.

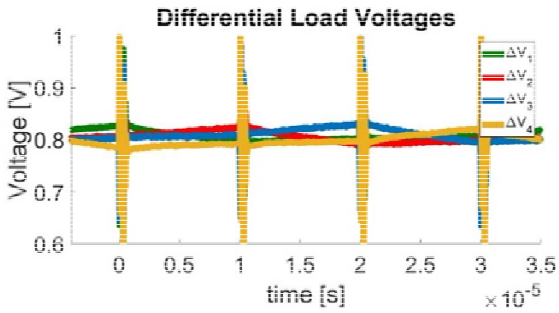


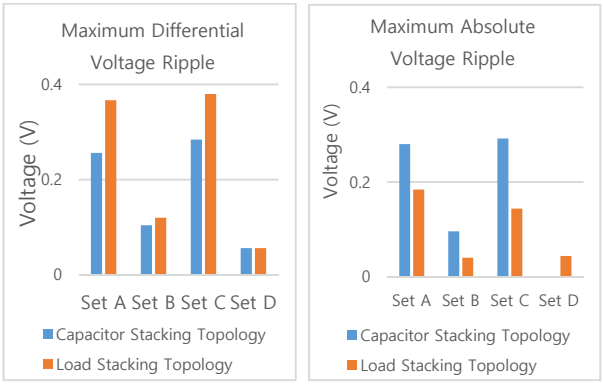
Fig. 18. Differential capacitor voltage waveforms of a 4 load system in the capacitor stacking topology using the rolling scheme at 100kHz with the Table III Set A currents.

[340.2µs; 343µs]. $t_{balance}$=3µs is the same as in the load stacking topology and it is also around 3 times the time constant τ=2.R_{ON}.C//C_{stray}. Phase III is also clearly defined.

C. Performance Criteria

To compare the performances of the topologies and the stability of the system, the differential voltage at the load point should be sensed. However, in the case of an integrated circuit, complex differential voltage sensors cannot be embedded. Only the fixed part node voltages can be measured. Based on these measurements, two criteria are investigated. Firstly, the differential voltage ripple, which is the difference between the highest and the lowest differential voltages measured at the fixed part points. It is the most accurate, and does a good job of reflecting the differential load voltage. However, it requires some computations and the error might be increased. Secondly, the node voltage ripple can be measured. It is the maximum voltage ripple between the three intermediate voltage points of the fixed parts.

Looking at Fig. 19, it can be seen that the differential voltage ripple is smaller in the capacitor stacking topology than in the load stacking topology. This shows that the capacitor stacking topology is more performant than the load stacking topology. However, the node voltage ripple is bigger in the capacitor stacking topology. Therefore, the node voltage ripple should not be considered as a performance criterion even though it is simpler to implement and less noisy.



(a) (b)

Fig. 19. Various sets of currents for the capacitor and load stacking topologies using the rolling scheme at 10kHz with the Table II component values. (a) Differential. (b) Node voltage ripples.

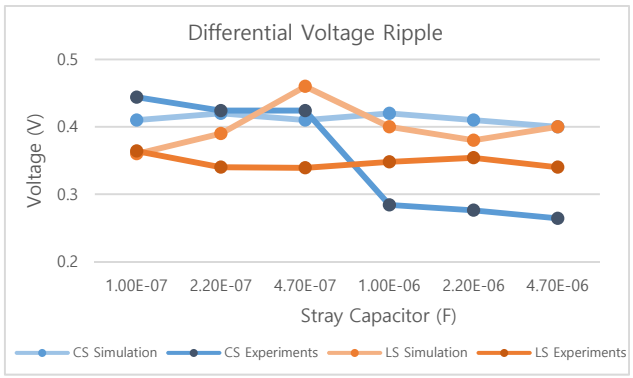


Fig. 20. Differential and node voltage ripples depending on the C_{stray} capacitance in the capacitor and load stacking topologies using the rolling scheme, the Table III Set A currents, and the Table II component values at 10kHz.

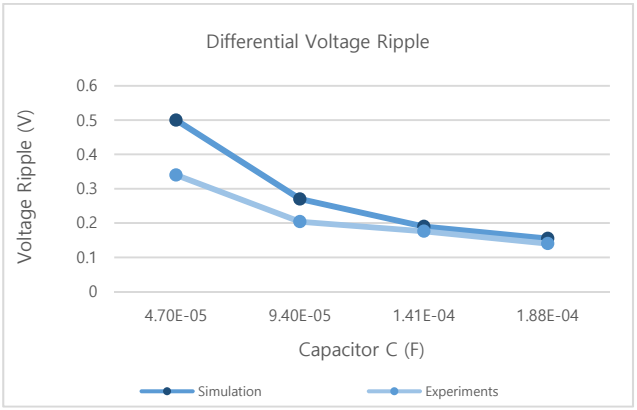


Fig. 21. Differential and node voltage ripples depending on the C capacitance in the capacitor stacking topology using the rolling scheme, the Table III Set A currents, and the Table II component values at 10kHz.

Based on the experimental results in Fig. 19, it can be seen that the capacitor stacking topology has a better performance for all of the current sets with a differential voltage ripple that is up to 111mV smaller than for the load stacking topology for set A and up to a 30% reduction (Set A).

Based on Fig. 19, it can be noticed that differential current values have the most significant impact on the ripple. For set A and set C with large differential current of up to 200mA, the voltage ripple can reach 250 to 350mA depending on the topology. Meanwhile, in the case of small differential currents sets (set B and set D), the voltage ripple has a maximum of 0.120mA.

It can also be observed that the capacitor C has a very large impact on the voltage ripple. Therefore, the performance of the system is as predicted in Eq. (9) and Eq. (10). Indeed, as shown in Fig. 21, multiplying the capacitor four times, from 47μF to 188μF, reduces the differential voltage ripple by 3.22 times for the simulation and 2.42 times for the experiments.

D. EMI Considerations

When there are very large current or voltage slopes in the transients of an electrical circuit, electromagnetic interference (EMI) emissions are generated. Very high frequency noise is then conducted through the line or radiated in the surrounding environment. This EMI issue is a very serious problem that voltage regulator designers must take into account across all of the design stages and especially when choosing a topology.

The stray capacitors can have a significant impact on the EMI produced since its small value results in large voltage slopes during deadtime. The switches can also cause large spikes since they are based on MOSFETs. However, fast switching is desired to reduce the switching losses.

Experiments show that the spikes are mainly caused by the switches, as observed in Fig. 17 and 18. Therefore, from an EMI point of view, the choice of the stray capacitor is not very important. Furthermore, as seen in Fig. 20, the stray capacitor has only a minor impact on the differential voltage ripple.

IV. CONCLUSIONS

In this paper, two new switched-capacitor converter topologies – a load stacking topology and a capacitor stacking topology – have been presented for the control of stacked voltage domains architecture voltages. Since they are easily integrable, these topologies can be used for powering digital loads such as multicore processors or 3D ICs. The main application for the new topologies would be for stacked digital loads. A voltage transient model for each of them has been presented as well as a loss model. A control scheme has been presented for the topologies. This control scheme is a rolling scheme. Finally, simulation and experiments allow for an evaluation of the two topologies to compare their performances.

The capacitor stacking topology has a smaller voltage ripple with a 30% reduction when compared to the load stacking topology. This makes it a better choice for stacked load

architectures.

The choice of the component values is very important for proper voltage regulation. An increased main capacitance significantly improves the voltage regulation. However, this is done at the cost of the size of the regulator. The stray capacitor has a minor impact on the differential voltage ripple. The EMI is mainly generated by the switch commutation.

Therefore, the capacitor stacking topology should be chosen since it generates less voltage ripple. This topology can be applied to digital loads including 2D and 3D integrated circuits.

ACKNOWLEDGMENT

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