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Design and Verification of Improved Cascaded Multilevel Inverter Topology with Asymmetric DC Sources

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Abstract

This paper presents the design and implementation of an improved cascaded multilevel inverter topology with asymmetric DC sources. This experimental inverter topology is a stand-alone system with simulations and experiments performed using resistance loads. The topology uses four asymmetric binary DC sources that are independent from each other and one H-bridge. The topology was simulated using PSIM software before an actual prototype circuit was tested. The proposed topology was shown to be very efficient. It was able to generate a smooth output waveform up to 31 levels with only eight switches. The obtained simulation and experimental results are almost identical. In a 1,200W (48.3Ω) resistive load application, the THDv and efficiency of the topology were found to be 1.7% and 97%, respectively. In inductive load applications, the THDv values were 1.1% and 1.3% for an inductive load (R=54Ω dan L=146mH**)** and a 36W fluorescent lamp load with a capacitor connected at the dc bus.

Key words: Asymmetric source, Degree switching, Generation level, H-bridge, Multilevel inverter

I. INTRODUCTION

There are many types of inverter technologies available, such as the voltage source inverter (VSI) and the current source inverter (CSI), depending on the DC-link energy storage component. VSIs are classified into two-level inverters and multilevel inverters (MLI) [1]. The first MLI was introduced in 1981 by Nabae. It was a three-level inverter using the neutral point of the DC line. This topology is referred to as Neutral-Point-Clamped (NPC) [2]. Furthermore, the MLI fly capacitor topology [3]-[6] and the cascaded H-bridge [5]-[8] topology were proposed in the nineties.

In addition, some modulation and switching control techniques as well as those in two-level inverters are used by MLIs such as multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM). The MLI type inverter is gaining popularity due to its better harmonic performance, high efficiency, lower electromagnetic interference, lower voltage stress and lower dv/dt ratio [9]-[16].

The cascaded H-bridge (CHB) is a recent MLI variant. With this topology, a higher number of output voltage levels can be achieved with fewer switches. The use of an H-bridge makes the circuit easy to modulate and easy to pack (making them faster and cheaper to build). However, the main disadvantage of the CHB-MLI is that a separate DC source is required [17]. The CHB-MLI is suitable for energy applications such as multi-panels PV systems, where the panels are connected as separate sources of the configuration.

Recently, there have been many proposed designs for reduced device count multilevel inverters (RDC-MLIs), especially H-bridge inverters such as the cascaded half-bridge-based multilevel DC-link (MLDCL) inverter, switched series/parallel sources (SSPS)-based MLI, series-connected switched sources (SCSS)-based MLI, multilevel module (MLM)-based MLI, reversing voltage (RV) topology, two-switch enabled level-generation (2SELG) based MLI and cascaded multilevel inverter minimum number of switches (MLI-MNS) [18], [19].

The MLDCL topology uses six symmetric DC sources, 12

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switches at the generation level and 4 switches on the H-bridge sections. This topology obtained a result wave of 13 output levels, and harmonics (THDv) below 5% after using a low pass filter (LPF) [20], [21]. The MLI-MNS has the same topology as the MLDCL. The difference is in the number of DC sources and the number of switches at the generation level. It uses five symmetric DC sources and 10 switch sources on the generation level portion. The number of output wave levels is lower at only 11 levels [19].

A single-phase multilevel inverter using switched series/ parallel DC voltage sources has been presented [22], [23]. In this topology, the switch is operated in series and parallel to the DC source. In practice, with three symmetrical DC sources and 12 switches, 11-levels of output voltage waveform were obtained. The drawback of this topology is that it required a low pass filter to keep harmonics below 5%.

A new multilevel inverter topology has been presented in [24], [25], which is called reversing voltage (RV). This topology uses symmetrical DC sources, where 10 switches are required to obtain 7 levels of output voltage. The disadvantages of this topology include the use of PWM switching and a low pass filter to keep the THD below 5%.

A new cascaded multilevel inverter topology with a minimum number of switching has been described in [26]. In this topology, the number of switches is the number of DC sources plus five for resistive loads. For 41 levels of output voltage, 25 switches were used for resistive loads with 20 DC sources, where a THD*v* of 2% was obtained. However, it was found that a high number of sources and DC switches were required.

CHB type inverters can be operated as symmetric and asymmetric DC sources. In asymmetrical operation, the configuration ratios of the DC source voltages for each H-bridge are not equal. The first asymmetric CHB topology was proposed by Manjrekar. A DC input source that is not equal as a 1: 2 ratio that reaches $2^{n+1}-1$ is called an asymmetric binary configuration [27], [28]. Lai and Shu proposed a symmetrical topology with a DC ratio of a 1:3 input source, which is referred to as a trinary asymmetric configuration [29].

The topology in this paper is based on [16]-[18]. It uses an asymmetric DC source with a reduced number of switches. The topology proposed in this paper subtracts the switch at the generation level (eliminating the reverse switch) and uses an asymmetry DC source.

The proposed topology was first simulated using PSIM followed by a prototype circuit. Verification of the topology was conducted through laboratory experiments on resistive loads. Experiments were performed at a maximum power of 1,200W.

The contribution of this study is a comparison with papers [16]-[18]. For the same number of sources, the output wave level is higher and the THD is lower without using a low pass filter (LPF). The number of switches is lower so that the conduction loss and switching power loss are lower. Thus, a higher efficiency can be obtained. A lower the number of switches means lower manufacturing costs.

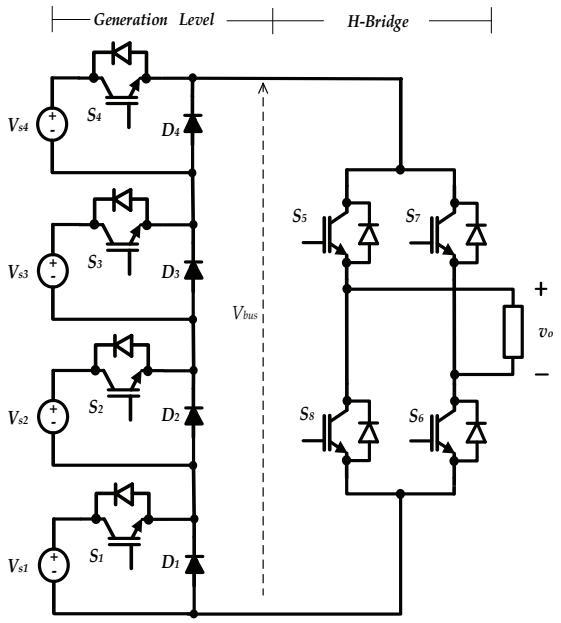


Fig. 1. Proposed multilevel inverter with a reduced number of switches.

II. Topology, Principle of Operation and Degree Switching

A. Topology

This MLI topology reduces the number of switches used and four DC sources are asymmetric (not equal) voltage levels. The topology of the proposed multilevel inverter is shown in Fig. 1, which shows the number of switches used, four asymmetric DC sources voltage levels, generation levels (S_1-S_4 & D_1-D_4) and H-bridges (S_5-S_8). Level generation produces a multilevel wave of a half wave during a positive period and the H-bridge inverts the waveform for a complete one period waveform (positive and negative period).

The V_{S1}-V_{S4} source voltages are asymmetric binary, where V_{S1} is the least significant bit and V_{S4} is the most significant bit. Then the values V_{S1} $2^0=1$, V_{S2} $2^1=2$, V_{S3} $2^2=4$ and V_{S4} $2^3=8$. Therefore. the ratio of the source voltage is V_{S1}: V_{S2}: V_{S3}: V_{S4} = V_{S1}: $2V_{S1}$: $4V_{S1}$: $8V_{S1}$.

The number of DC sources and switches at the generation level will determine the waveform output level. This can be calculated according to the equation below:

$$L_{vo} = 2n^2 - 1 \quad (1)$$

Where L_{vo} is output level voltage and n is the number of DC sources. Based on equation (1) this multilevel inverter topology produces 31 levels.

TABLE I
SWITCH CONDUCTION DURING HALF A PERIOD AND VOLTAGE AT V_{BUS}

Mod Operation	*Time Conduction*	*Switch Conduction*	*Voltage at $V_{bus(max)}$*	*Voltage Drop in Switch (V_{SW})*
1	t_0-t_1	D_1,D_2,D_3,D_4,S_5,S_6	$V_0=0$	$4V_{F(diode)}+2V_{CE(ON)}$
2	t_1-t_2	S_1,D_2,D_3,D_4,S_5,S_6	$V_1=V_{S1}$	$3V_{F(diode)}+3V_{CE(ON)}$
3	t_2-t_3	D_1,S_2,D_3,D_4,S_5,S_6	$V_2=V_{S2}$	$3V_{F(diode)}+3V_{CE(ON)}$
4	t_3-t_4	S_1,S_2,D_3,D_4,S_5,S_6	$V_3=V_{S1}+V_{S2}$	$2V_{F(diode)}+4V_{CE(ON)}$
5	t_4-t_5	D_1,D_2,S_3,D_4,S_5,S_6	$V_4=V_{S3}$	$3V_{F(diode)}+3V_{CE(ON)}$
6	t_5-t_6	S_1,D_2,S_3,D_4,S_5,S_6	$V_5=V_{S1}+V_{S3}$	$2V_{F(diode)}+4V_{CE(ON)}$
7	t_6-t_7	D_1,S_2,S_3,D_4,S_5,S_6	$V_6=V_{S2}+V_{S3}$	$2V_{F(diode)}+4V_{CE(ON)}$
8	t_7-t_8	S_1,S_2,S_3,D_4,S_5,S_6	$V_7=V_{S1}+V_{S2}+V_{S3}$	$1V_{F(diode)}+5V_{CE(ON)}$
9	t_8-t_9	D_1,D_2,D_3,S_4,S_5,S_6	$V_8=V_{S4}$	$3V_{F(diode)}+3V_{CE(ON)}$
10	t_9-t_{10}	S_1,D_2,D_3,S_4,S_5,S_6	$V_9=V_{S1}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
11	t_{10}-t_{11}	D_1,S_2,D_3,S_4,S_5,S_6	$V_{10}=V_{S2}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
12	t_{11}-t_{12}	S_1,S_2,D_3,S_4,S_5,S_6	$V_{11}=V_{S1}+V_{S2}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
13	t_{12}-t_{13}	D_1,D_2,S_3,S_4,S_5,S_6	$V_{12}=V_{S3}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
14	t_{13}-t_{14}	S_1,D_2,S_3,S_4,S_5,S_6	$V_{13}=V_{S1}+V_{S3}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
15	t_{14}-t_{15}	D_1,S_2,S_3,S_4,S_5,S_6	$V_{14}=V_{S2}+V_{S3}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
16	t_{15}-t_{16}	S_1,S_2,S_3,S_4,S_5,S_6	$V_{15}=V_{S1}+V_{S2}+V_{S3}+V_{S4}$	$6V_{CE(ON)}$
17	t_{16}-t_{17}	D_1,S_2,S_3,S_4,S_5,S_6	$V_{16}=V_{S2}+V_{S3}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
18	t_{17}-t_{18}	S_1,D_2,S_3,S_4,S_5,S_6	$V_{17}=V_{S1}+V_{S3}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
19	t_{18}-t_{19}	D_1,D_2,S_3,S_4,S_5,S_6	$V_{18}=V_{S3}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
20	t_{20}-t_{21}	S_1,S_2,D_3,S_4,S_5,S_6	$V_{19}=V_{S1}+V_{S2}+V_{S4}$	$1V_{F(diode)}+5V_{CE(ON)}$
21	t_{21}-t_{22}	D_1,S_2,D_3,S_4,S_5,S_6	$V_{20}=V_{S2}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
22	t_{22}-t_{23}	D_1,S_2,D_3,S_4,S_5,S_6	$V_{21}=V_{S2}+V_{S4}$	$2V_{F(diode)}+4V_{CE(ON)}$
23	t_{23}-t_{24}	D_1,D_2,D_3,S_4,S_5,S_6	$V_{22}=V_{S4}$	$3V_{F(diode)}+3V_{CE(ON)}$
24	t_{24}-t_{25}	S_1,S_2,S_3,D_4,S_5,S_6	$V_{23}=V_{S1}+V_{S2}+V_{S3}$	$1V_{F(diode)}+5V_{CE(ON)}$
25	t_{25}-t_{26}	D_1,S_2,S_3,D_4,S_5,S_6	$V_{24}=V_{S2}+V_{S3}$	$2V_{F(diode)}+4V_{CE(ON)}$
26	t_{26}-t_{27}	S_1,D_2,S_3,D_4,S_5,S_6	$V_{25}=V_{S1}+V_{S3}$	$2V_{F(diode)}+4V_{CE(ON)}$
27	t_{27}-t_{28}	D_1,D_2,S_3,D_4,S_5,S_6	$V_{26}=V_{S3}$	$3V_{F(diode)}+3V_{CE(ON)}$
28	t_{28}-t_{29}	S_1,S_2,D_3,D_4,S_5,S_6	$V_{27}=V_{S1}+V_{S2}$	$2V_{F(diode)}+4V_{CE(ON)}$
29	t_{29}-t_{30}	D_1,S_2,D_3,D_4,S_5,S_6	$V_{28}=V_{S2}$	$3V_{F(diode)}+3V_{CE(ON)}$
30	t_{30}-t_{31}	S_1,D_2,D_3,D_4,S_5,S_6	$V_{29}=V_{S1}$	$3V_{F(diode)}+3V_{CE(ON)}$
31	t_{31}-t_{32}	D_1,D_2,D_3,D_4,S_5,S_6	$V_{30}=0$	$4V_{F(diode)}+2V_{CE(ON)}$

The sequence for the switches S_1-S_8 for half of a period (t_0-t_{31}/mode operation 1-31), the instantaneous voltage at the output generation level (V_{bus}) and voltage drop in the switch (V_{SW}) are shown in Table I.

The S_5-S_6 switches are ON for half a period, for the next half S_7-S_8 are ON so that the flow is opposite the load.

The maximum voltage at V_{bus} is calculated based on the following equation:

$$V_{bus(max)} = V_{S1} + V_{S2} + V_{S3} + V_{S4} \tag{2}$$

The output RMS voltage is given by:

$$V_{o(rms)} = \frac{V_{bus(max)}}{\sqrt{2}} \tag{3}$$

The voltage sources V_{S1}-V_{s4} are each calculated by the following equations:

$$V_{S1} = \frac{\left(V_{O(rms)} \times \sqrt{2}\right) + V_{SW(tot)}}{15} \tag{4}$$

$$V_{S2} = \frac{2\left(V_{O(rms)} \times \sqrt{2}\right) + V_{SW(tot)}}{15} = 2V_{S1} \tag{5}$$

$$V_{S3} = \frac{4\left(V_{O(rms)} \times \sqrt{2}\right) + V_{SW(tot)}}{15} = 4V_{S1} \tag{6}$$

$$V_{S4} = \frac{8\left(V_{O(rms)} x \sqrt{2}\right) + V_{SW(tot)}}{15} = 8V_{S1} \tag{7}$$

where $V_{O(rms)}$ is the RMS output voltage, and $V_{SW(tot)}$ is the total voltage drop during switching. Based on Table I, $V_{SW(tot)}$ can be calculated as follows:

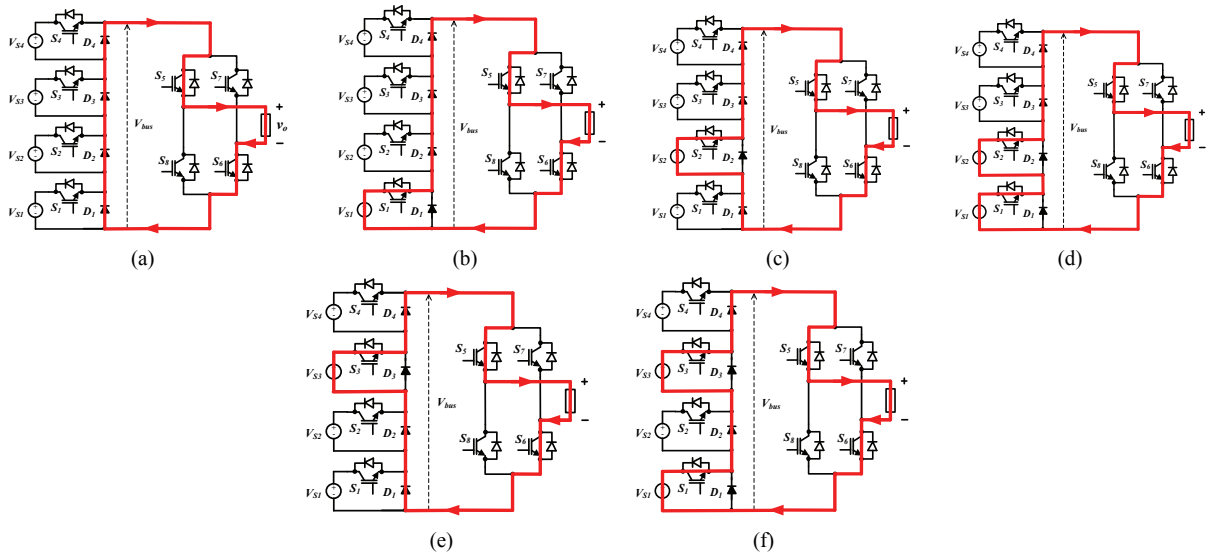


Fig. 2. Operation modes 1 to 6. (a) Mode 1 conduction period t_0-t_1. (b) Mode 2 conduction period t_1-t_2. (c) Mode 3 conduction period t_2-t_3. (d) Mode 4 conduction period t_3-t_4. (e) Mode 5 conduction period t_4-t_5. (f) Mode 6 conduction period t_5-t_6.

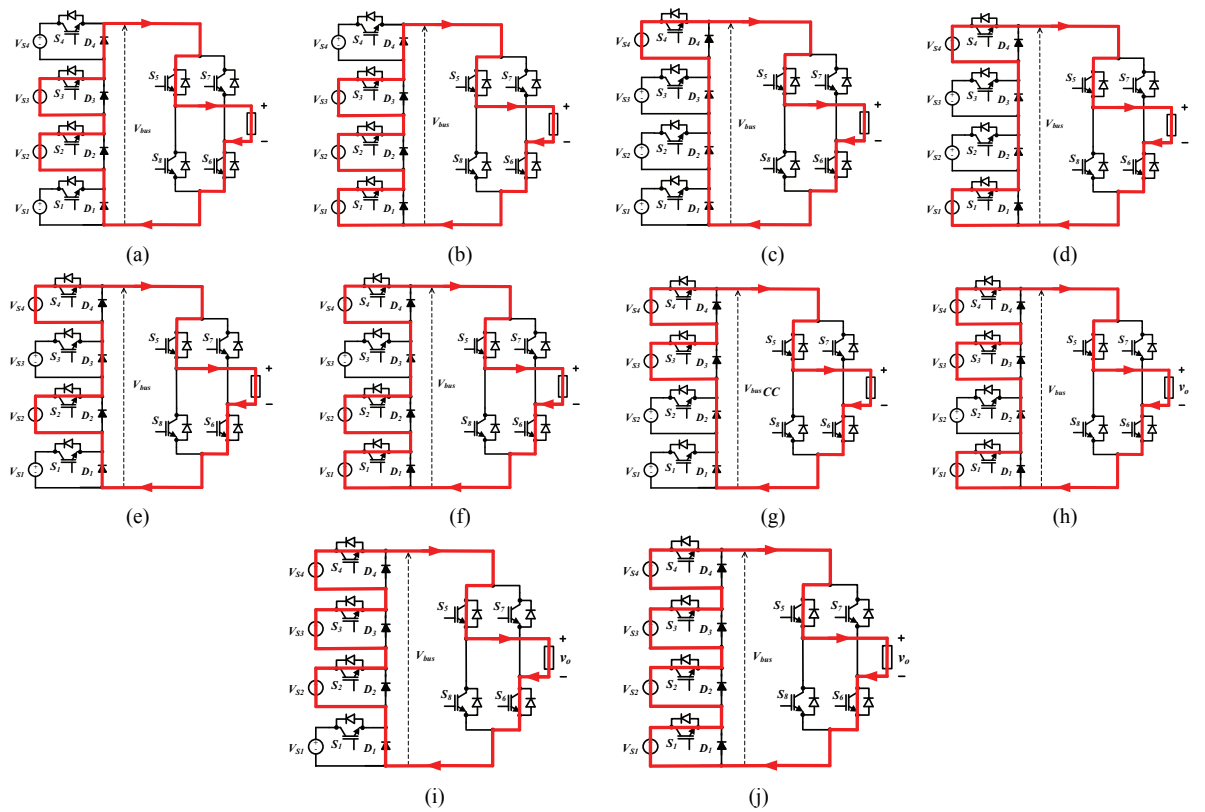


Fig. 3. Operation modes 7 to 16. (a) Mode 7 conduction period t_6-t_7. (b) Mode 8 conduction period t_7-t_8. (c) Mode 9 conduction period t_8-t_9. (d) Mode 10 conduction period t_9-t_{10}. (e) Mode 11 conduction period t_{10}-t_{11}. (f) Mode 12 conduction period t_{11}-t_{12}. (g) Mode 13 conduction period t_{12}-t_{13}. (h) Mode 14 conduction period t_{13}-t_{14}. (i) Mode 15 conduction period t_{14}-t_{15}. (j) Mode 16 conduction period t_{15}-t_{16}.

$$V_{SW(tot)} = \frac{\begin{array}{l} V_{SW(\mathrm{mod}1)}\left(t_1 - t_0\right) + V_{SW(\mathrm{mod}2)}\left(t_2 - t_1\right) + \\ V_{SW(\mathrm{mod}3)}\left(t_3 - t_2\right) + \ldots\ldots\ldots + V_{SW(\mathrm{mod}32)} \end{array}}{\left(t_{31} - t_{30}\right)} \qquad (8)$$

B. *Principle of Operation*

The principle of operation of the multilevel inverter in Fig. 1 is divided into 31 modes, where each mode forms one level. The operation modes from 1 to 31 half cycles starting at t_0 to t_{31} are shown in Fig. 2-5.

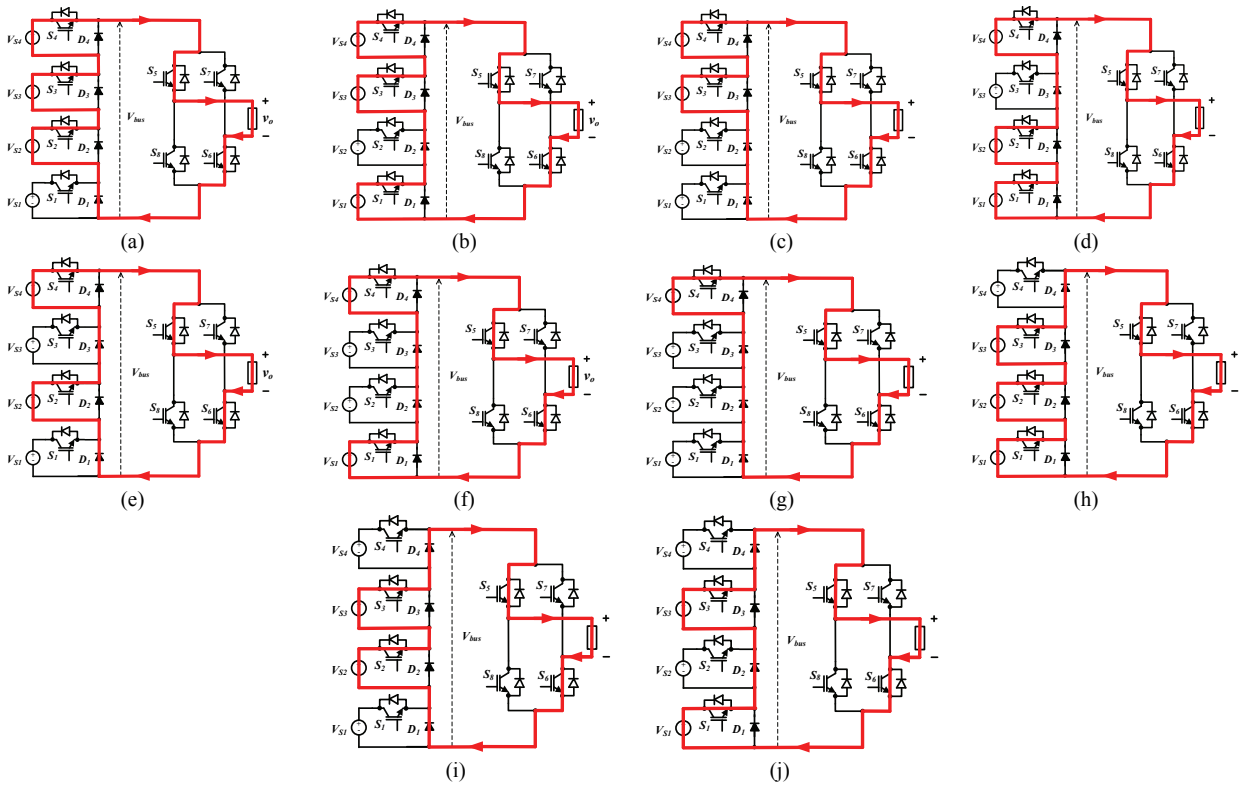


Fig. 4. Operation modes 17 to 26. (a) Mode 17 conduction period t_{16}-t_{17}. (b) Mode 18 conduction period t_{17}-t_{18}. (c) Mode 19 conduction period t_{18}-t_{19}. (d) Mode 20 conduction period t_{19}-t_{20}. (e) Mode 21 conduction period t_{20}-t_{21}. (f) Mode 22 conduction period t_{21}-t_{22}. (g) Mode 23 conduction period t_{22}-t_{23}. (h) Mode 24 conduction period t_{23}-t_{24}. (i) Mode 25 conduction period t_{24}-t_{25}. (j) Mode 26 conduction period t_{25}-t_{26}.

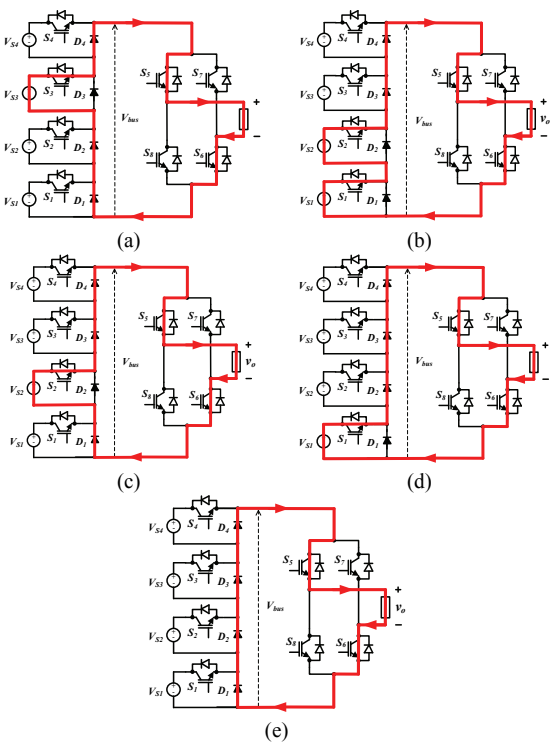


Fig. 5. Operation modes 27 to 31. (a) Mode 27 conduction period t_{26}-t_{27}. (b) Mode 28 conduction period t_{27}-t_{28}. (c) Mode 29 conduction period t_{28}-t_{29}. (d) Mode 30 conduction period t_{29}-t_{30}. (e) Mode 31 conduction period t_{30}-t_{31}.

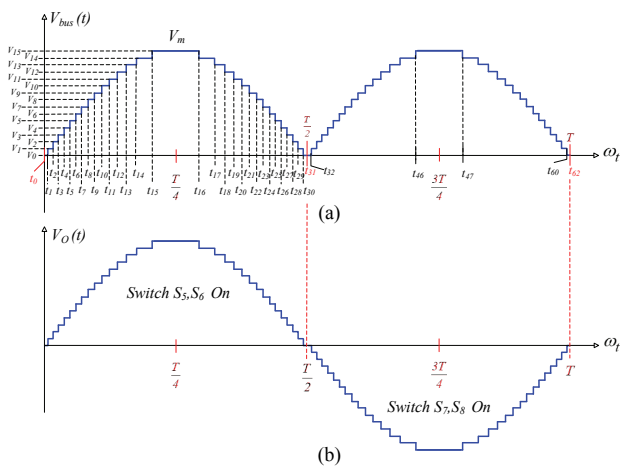


Fig. 6. Output waveforms. (a) Output level generation (V_{bus}). (b) Output of the inverter (V_o).

A waveform of V_{bus} for one period (t_0-t_{62}) is shown in Fig. 6(a) and an output waveform is shown in Fig. 6(b).

C. Switching Degree

The switching signal form for the generation level during t_0 - t_{31} (0 - T/2) is shown in Fig. 7. The switching signal repeats for half a period (T/2 - T, T-3T/2, 3T/2 - 2T, etc.).

The degree of the switching signal (α) is obtained using equations (9), (10) and (11).

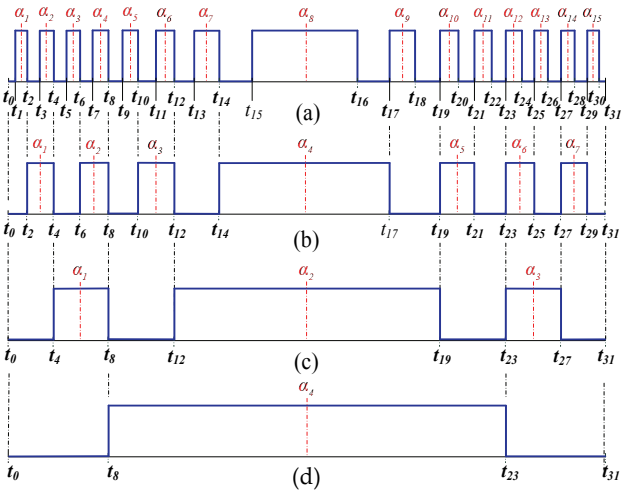


Fig. 7. Signal switching generation level. (a) Switch S_1. (b) Switch S_2. (c) Switch S_3. (d) Switch S_4.

$$\alpha_{(t_1 \sim t_{16})} = Sin^{-1}\left(\frac{V_{kp} L_{n\,(1,2,3\ldots16)}}{V_m}\right) \times 2 \tag{9}$$

$$\alpha_{(t_{17} \sim t_{31})} = 360 - Sin^{-1}\left(\frac{V_{kp} L_{n\,(17,18,19\ldots31)}}{V_m}\right) \times 2 \tag{10}$$

Here, V_m is the maximum voltage from the inverter output, which is 339.41V. In addition, L_n is the nth level, which is level 1 to 16, and V_{kp} is the voltage rise level, which is level 17 to 31. The value of V_{kp} is calculated using equation 11, and n_L is the number of levels of the output voltage, which is 31. Therefore, V_{kp} is 22.63V.

$$V_{kp} = \frac{V_m}{\left(\frac{n_L}{2} - 1\right)} \tag{11}$$

The middle values of the degree of signal switching (α) can be obtained from equations 9 and 10. For generating waves, as shown in Fig. 6 and Fig. 7, α starts from the rise time (rising time degree) and the fall time (falling time degrees). For the switch S_1; $\alpha_1=t_1-t_2$, $\alpha_2=t_3-t_4$, $\alpha_3=t_5-t_6$, $\alpha_4=t_7-t_8$, $\alpha_5=t_9-t_{10}$, $\alpha_6=t_{11}-t_{12}$, $\alpha_7=t_{13}-t_{14}$, $\alpha_8=t_{15}-t_{16}$, $\alpha_9=t_{17}-t_{18}$, $\alpha_{10}=t_{19}-t_{20}$, $\alpha_{11}=t_{21}-t_{22}$, $\alpha_{12}=t_{23}-t_{24}$, $\alpha_{13}=t_{25}-t_{26}$, $\alpha_{14}=t_{27}-t_{28}$ and $\alpha_{15}=t_{29}-t_{30}$. For the switch S_2; $\alpha_1=t_2-t_4$, $\alpha_2=t_6-t_8$, $\alpha_3=t_{10}-t_{12}$, $\alpha_4=t_{14}-t_{17}$, $\alpha_5=t_{19}-t_{21}$, $\alpha_6=t_{23}-t_{25}$ and $\alpha_7=t_{27}-t_{29}$. For the switch S_3; $\alpha_1=t_4-t_8$, $\alpha_2=t_{12}-t_{19}$ and $\alpha_3=t_{23}-t_{27}$. For the switch S_4; $\alpha_1=t_8-t_{23}$. The degrees of the rise time and the fall time can be calculated by equation 12.

$$da_n = \frac{dt_n + \left(dt_{n+1} - db_n\right)}{2} \tag{12}$$

Where:

da_n = Degree rises time to n
db_n = Degree down time to n
dt_n = Degree middle time to n
dt_{n+1} = Degree time middle to n + 1

TABLE II
SWITCHING DEGREE OF THE SWITCHES S_1-S_4 (LEVEL GENERATION)

No	Switch	Degree
1	S_1	α_1=3.8-11.5,α_2=19.2-27.0, α_3=19.2-27.0, α_4=51.4-60.0, α_5=69.1-78.7, α_6=89.0-100.3, α_7=113.2-129.0, α_8=159.0-201.0, α_9=231.0-246.8, α_{10}=259.7-271.0, α_{11}=281.3-290.9,α_{12}=300.0-308.6, α_{13}=317.0-325.1, α_{14}=333.0-340.8, α_{15}=348.5-356.2
2	S_2	α_1=11.5-27.0, α_2=43.0-60.0, α_3=78.7-100.3, α_4=159.0-231.0, α_5=259.7-281.3, α_6=300.0-317.0, α_7=333.0-348.5
3	S_3	α_1=27.0-60.0, α_2=100.3-259.7, α_3=300.0-333.0
4	S_4	α_1=60-300

TABLE III
VOLTAGE SOURCE V_{S1}-V_{S4}

Source	Comparison	Voltage (V)
V_{S1}	V_{S1}	22.63
V_{S2}	$2V_{S1}$	45.25
V_{S3}	$4V_{S1}$	90.51
V_{S4}	$8V_{S1}$	181.02

In the initial start, the lower degree value is 0 and the upper degree is 3.8. The value of the upper degree becomes the lower-grade in the 2nd degree. Then the degree value of the 2nd degree becomes the lower-grade on the 3rd degree and so on. From the width-degree calculation, the switching degrees for the S_1-S_4 switches are shown in Table II.

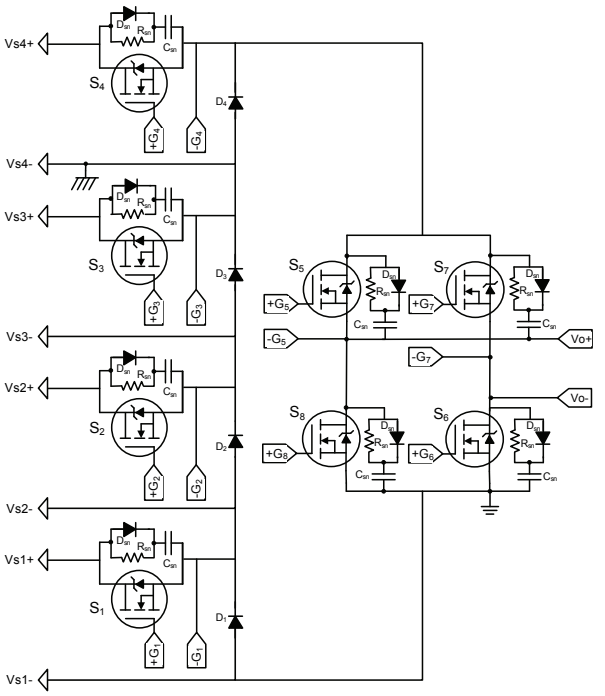
The source voltage Vs1-Vs4 is calculated based on the maximum voltage (V_m) of the output, namely:

$$\begin{aligned} V_m &= V_{S1} + V_{S2} + V_{S3} + V_{S4} \\ &= V_{S1} + 2V_{S1} + 4V_{S1} + 8V_{S1} \\ &= 15V_{S1} \end{aligned} \tag{13}$$

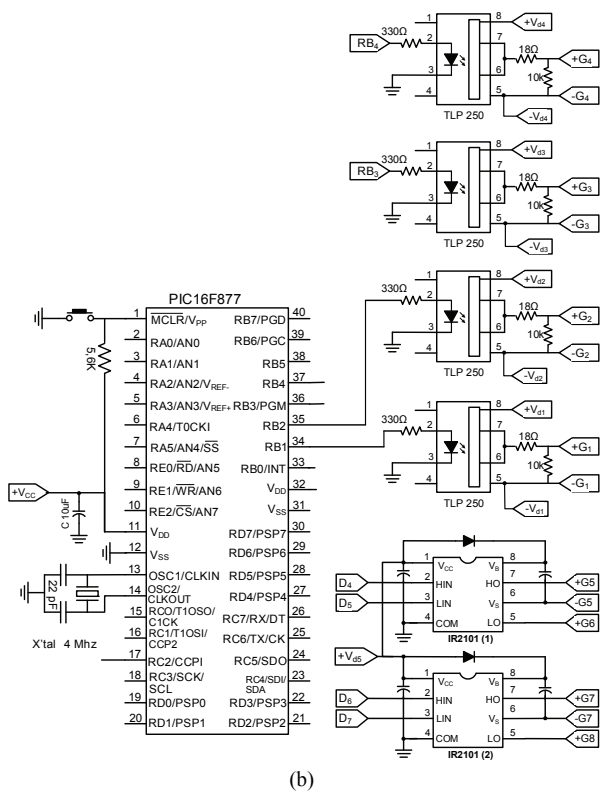
The effective voltage (V_{rms}) of the inverter output is 240V. Then V_m=339.41V. Based on equation 13, the voltage source V_{S1}-V_{S4} is given in Table III.

III. EXPERIMENTAL CIRCUIT

The experiment circuit is based on the topology in Fig. 1, as shown in Fig. 8, where Fig. 8(a) is a power circuit and Fig. 8(b) is a control circuit. The maximum current flow in the switching device can be calculated with equation 14 for the output power (P_O) 1200W, assuming an efficiency of η=0.94% and an output voltage of V_O = 240V. Then the following relationship is obtained:



(a)



(b)

Fig. 8. Experimental circuits. (a) Power circuit. (b) Drives and switching control circuit.

$$I_{suis} = \frac{\left(\frac{P_O}{\eta}\right)}{V_O} = \frac{\left(\frac{1200}{0,94}\right)}{240} = 5,3A \tag{14}$$

TABLE IV
COMPONENTS OF SNUBBER CIRCUITS

Snubber Switch	D_{sn}	C_{sn} *(nF)*	R_{sn} *(Ω)*
S_1	*MUR 410*	*1.2*	*330*
S_2	*MUR 420*	*1.1*	*330*
S_3	*MUR 430*	*1*	*330*
S_4	*MUR 440*	*0.9*	*330*
S_5-S_8	*MUR 460*	*12.9*	*470*

The output voltage is 240V. Therefore, the max voltage (V_{mak}) is 339.4V and the maximum switch current is 5.3A. Based on these parameters, the S_1-S_8 switches use the IRFP460 MOSFET, which has a specifications of V_{DS} 500 V, I_D 20 A, $R_{DS(on)}$ 0.27Ω, t_r 120ns and t_f 98ns.

The switching signal in Fig. 6 has the shortest time from t_1 to t_3, which are t_1 = 10.6μs and t_3 = 53.3μs. Then the reverse recovery time diode D_1-D_4 is:

$$\begin{aligned} t_{Suis} &= t_3 - t_1 \\ &= 53.3uS - 10.6uS = 42.7uS \end{aligned} \tag{15}$$

In this case, the fast recovery type diode D_1 - D_4 (MUR 1560) can be used for the diode D_1 - D_4. This diode has specifications of V_{RMS} 600 V, I_{FRMS} 25 A and t_{rr} 35ns.

The snubber circuit consists of diodes (D_{sn}), capacitors (C_{sn}) and resistors (R_{sn}). Their values are given in Table IV. The C_{sn} and R_{sn} values are calculated by the following equations:

$$C_{sn} = \frac{I_o t_s}{2V_s} \tag{16}$$

$$R_{sn} = \frac{2}{t_{on(min)} C_s} \tag{17}$$

The port V_{S1} + until V_{S4} + is a positive port voltage, while the port V_{S1}- until V_{S4}- refers to a negative port DC source. The port V_{S1}- until V_{S4} is separated from other ports (not unified). The port + G_1 to + G_8 and the port - G_1 to -G_8 make up the input switching signal from the circuit driver.

The drive circuit rated the generation of the S_1- S_4 switches using the TLP250 integrated circuit. These four integrated circuits use separate 18V power supplies. This is done so that the S_1 - S_4 switches become a floating earth point. The drive circuit for the H-bridge (S5-S8 switches) uses two IR210 integrated circuits. Both of these integrated circuits get an 18V supply. The switching control circuit for the switches S_1-S_8 uses a PIC 16F877 microcontroller and programming made using Basic Pro software. The power supply for this microcontroller circuit is from the same source as the H-bridge drive circuit. The experimental setup for the circuit in Fig. 8 is shown in Fig. 9.

IV. RESULTS AND DISCUSSION

This inverter topology is designed for stand-alone systems with resistive and inductive loads. Simulations were carried

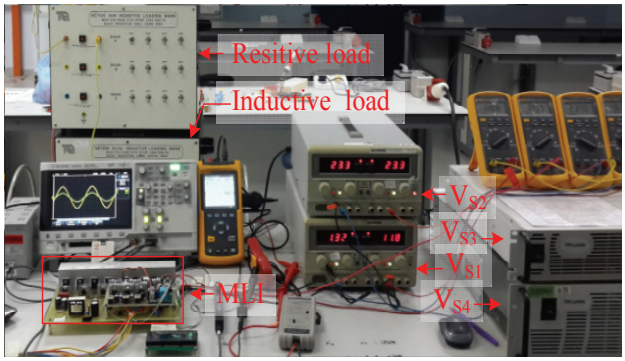
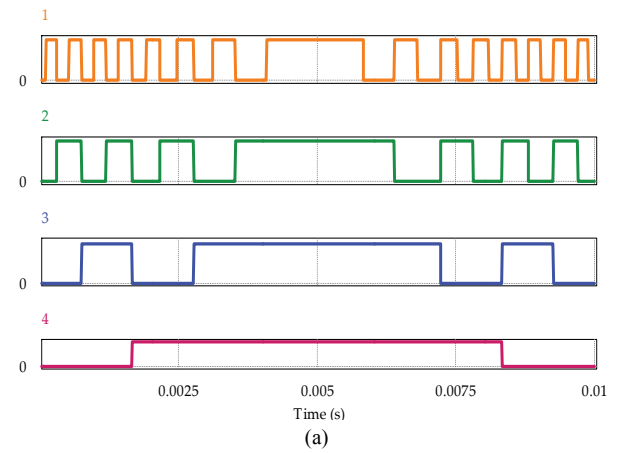
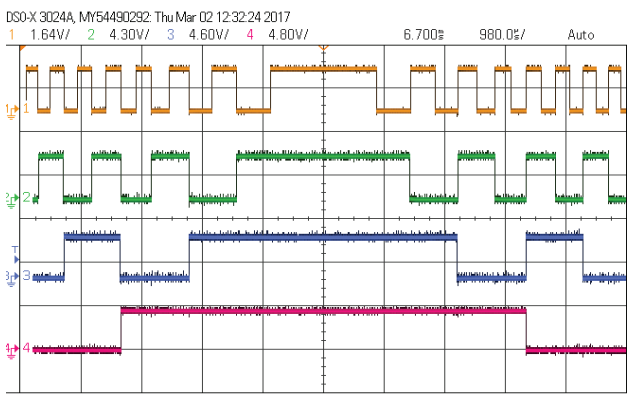


Fig. 9. Experimental setup for the proposed circuit.



(a)



(b)

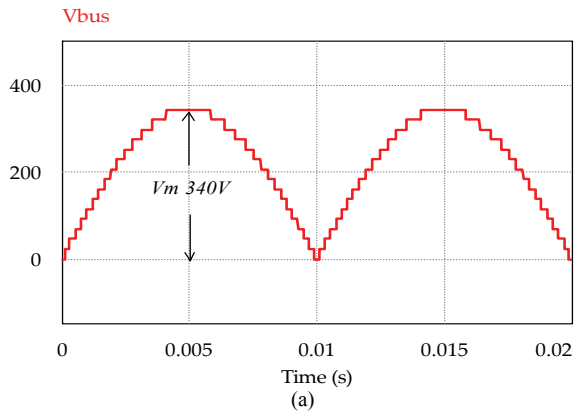
Fig. 10. Switching level generation. (a) Simulation. (b) Experiment.

out using PSIM software. For the prototype circuit, a fluke 43B dan scope Agilent DSOX 2012A was used for measurements.

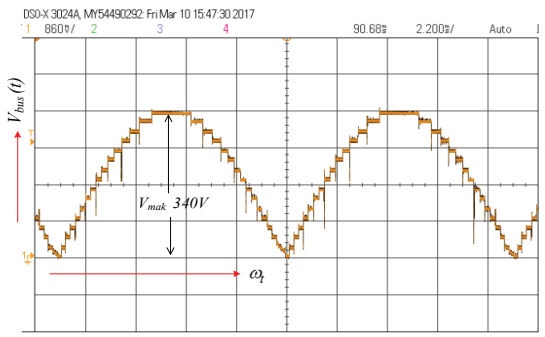
A. Switching and DC Bus Wave

Simulation and experimental results at the generation level (switches S_1, S_2, S_3, S_4) are shown in Fig. 10(a) (simulation) and Fig. 10(b) (experiment), respectively. The simulated and experimental signals have the same shape and the t_{on}-t_{off} degree period for each signal (switch S_1-S_4) is given in Table II. This switching signal determines the output waveform of the multilevel inverter.

Simulation and experimental results for output voltage



(a)



(b)

Fig 11. Output waveform at V_{bus}. (a) Simulation. (b) Experiment.

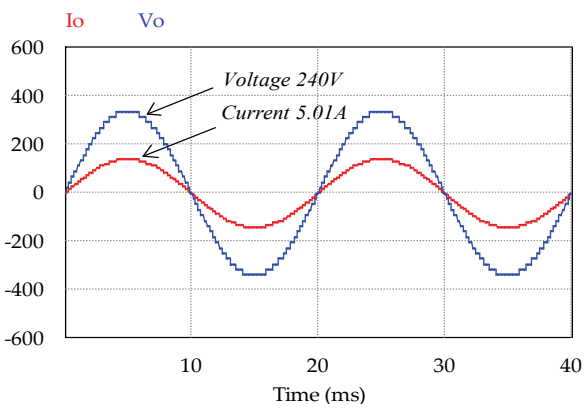


Fig. 12. Simulation output waveforms at a resistive load of 48.3Ω.

waveforms at the generation level (V_{bus}) are shown in Fig. 11(a) and Fig. 11(b), respectively. These simulated and experimental waveforms show a good agreement. This corresponds to the waveform in operation modes 1 to 62 (during the t_0-t_{62} interval) as shown in Fig. 6(a). The waveforms consist of 31 voltage levels from V_0 to V_{30}, as given in Table I.

B. Resistive Loads

Voltage and current output waveforms simulation results for load of R = 48.3Ω (1200 watts of output power) are shown in Fig. 12, where a 240Vrms voltage and a 5.01A rms current were obtained. For comparison, experimental results as shown in Fig. 13, where a 240Vrms voltage and a 4.95A rms current were obtained. The experiment results agreed with the

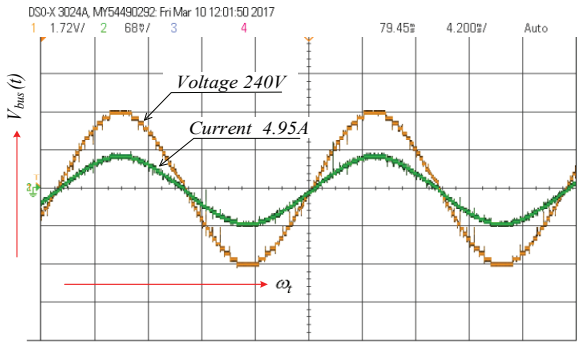
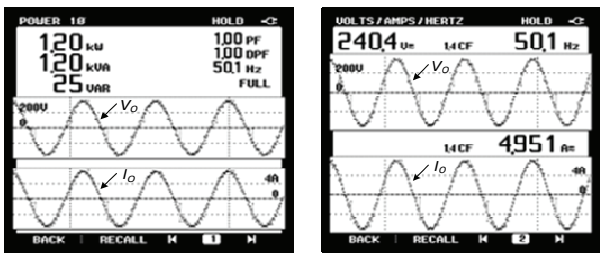
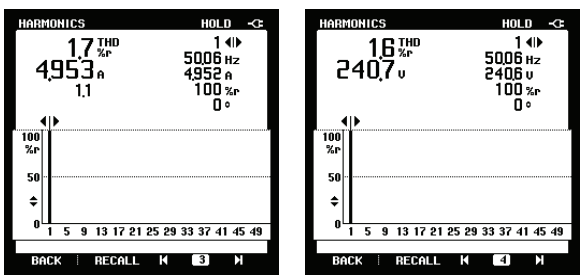


Fig. 13. Experiment output waveforms at a resistive load of 48.3Ω.



(a) (b)

Fig. 14. Output waveforms at a resistive load of 48.3Ω. (a) Power values. (b) Voltage and current values.



(a) (b)

Fig. 15. Harmonic spectrum at a resistive load of 48.3Ω. (a) THDi. (b) THDv.

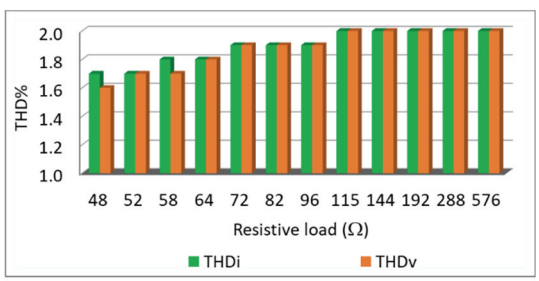


Fig. 16. Effect on THDv from changes in the load resistance from 48.3Ω to 576Ω.

simulation for the resistance load analysis.

Waveforms of the voltage and current at a 48.3Ω resistive load are then measured with a Fluke 34B Power Quality as shown in Fig. 14. Fig. 14(a) shows a voltage waveform, a current wave and a power value display of 1.20kW, with a power factor of 1.00PF and a frequency of 50Hz. Meanwhile, Fig. 14(b) is also a voltage waveform, current wave with a

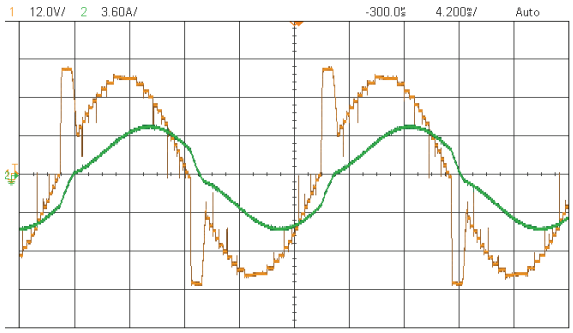


Fig. 17. Experimental output waveforms at an inductive load (R=54Ω dan L=146mH) without a capacitor.

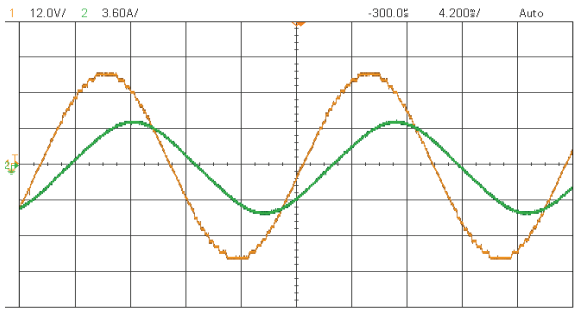


Fig. 18. Experimental output waveforms at an inductive load (R=54Ω dan L=146mH) using a capacitor 22uF.

240.4V voltage value display, a 4.951A current value and a 50 Hz frequency.

The harmonic spectrums of the THDi and THDv at a 48.3Ω resistive load are shown in Fig. 15(a) and 15(b), respectively. The values of the obtained THDi and THDv are 1.7% and 1.6%, respectively.

Experimental results for the effect of load changes from 48.3Ω to 576 Ω on the THDv are shown in Fig. 16, while the voltage is held constant at 240V.

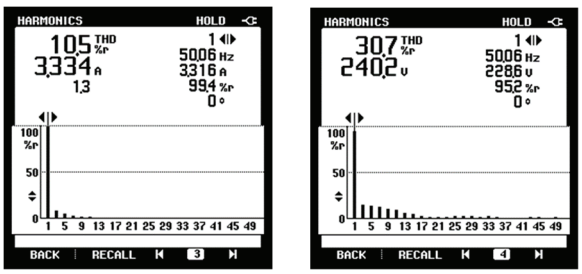
C. Inductive Load

In inductive loads, a spike voltage occurs due to self-induced emf (back emf). This spike voltage can be overcome (removed) by using a capacitor on the dc bus. The experimental voltage and output current R=54Ω and L= 146mH before the use of capacitors are shown in Fig. 17, and they are shown in Fig. 18 after the use of 22uF capacitors on the dc buses.

Harmonic spectrums of the THDi and THDv at an R=54Ω and L=146mH inductive load are shown in Fig. 19 and Fig. 20, respectively. The values of the THDi and THDv without a capacitor are 10.5% and 30.7% as shown in Fig. 19(a) and 19(b), respectively.

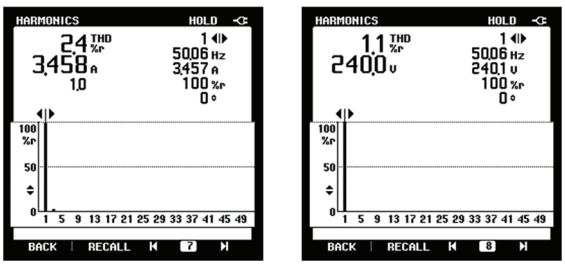
The values of the THDi and THDv using a capacitor 22uF on the dc bus are 2.4% and 1.1% as shown in Fig. 20(a) and 20(b), respectively.

The application of the inverter prototype on 36W fluorescent lamps is shown in Fig. 21-23. Current and voltage waveforms before and after the use of capacitors 3uF on the



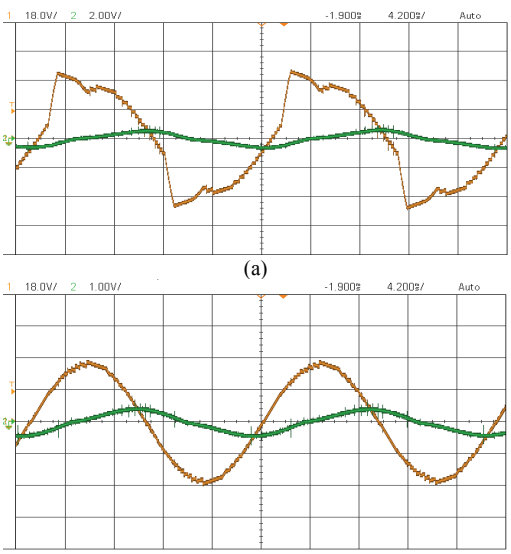
(a) (b)

Fig. 19. Harmonic spectrum at an inductive load (R=54Ω and L=146mH) without a capacitor. (a) THDi. (b) THDv.



(a) (b)

Fig. 20. Harmonic spectrum at an inductive load (R=54Ω and L=146mH) using a capacitor 22Uf. (a) THDi. (b) THDv.



(a)

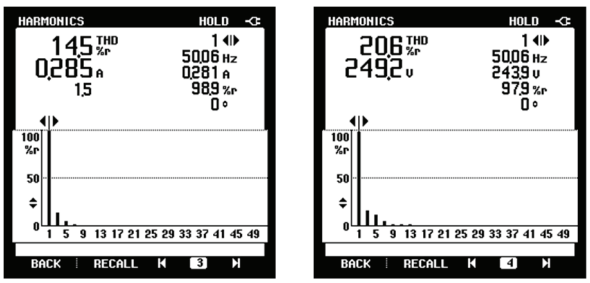
(b)

Fig. 21. Experimental output waveforms with a 36W fluorescent lamp. (a) Without a capacitor. (b) Using a capacitor 3uF.

dc bus are shown in Fig. 21(a) and in Fig. 21(b), respectively.

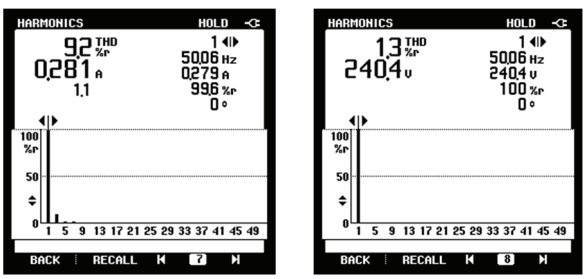
The harmonic spectrum of the THDi and THDv for a 36W fluorescent lamp are shown in Fig. 22 and 23, respectively. The values of the THDi and THDv are 10.5% and 30.7%, respectively. This can be seen in Fig. 22(a) and Fig. 22(b).

The values of the THDi and THDv using a capacitor 3uF on the dc bus obtained are 9.2% and 1.3% as shown in Fig. 23(a) and Fig. 23(b), respectively. Here, the THDi value does not fall below 9.2%. This is caused by harmonics rather than the fluorescent lights which have a natural harmonic content (THDi).



(a) (b)

Fig. 22. Harmonic spectrum with a 36W fluorescent lamp without capacitor. (a) THDi. (b) THDv.



(a) (b)

Fig. 23. Harmonic spectrum with a 36W fluorescent lamp using a capacitor 3uF. (a) THDi. (b) THDv.

The size of the capacitor value is determined based on the reactive power of the load produced by an inductive load. The capacitor value is calculated by the following equation:

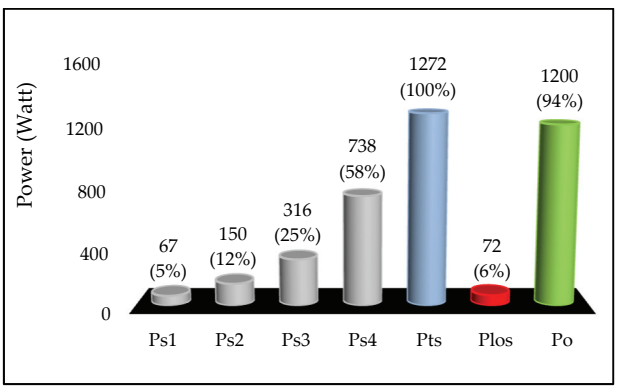
$$C_{(uF)} = \frac{Q_L}{2\pi f V^2} \times 10^6 \tag{18}$$

The power distributions at the P_{S1}-P_{S4} input are not the same. The highest power on V_{S4} flows through the S_4 switch and the lowest power on P_{S1} flows through the switch S_1. The power distribution at a 48.3Ω resistive load is shown in Fig. 24(a). The total input power (P_{ts}) of 1272W is distributed 67W (5%) on P_{S1}, 150W (12%) on P_{S2}, 316W (25%) on P_{S3} and 738W (58%) on P_{S4}. The power losses (P_{los}) are 72W (6%) and the output power (P_o) is 1200W (94%). The MLI efficiency that uses an IRFP460 MOSFET on the S_1-S_8 switches in the range from 100W to 1200W is shown in Fig. 24(b). The maximum efficiency was 97.02% at a 600W load, and it decreases to 94.37% at a 1200W load. Meanwhile, the optimum efficiency simulation result is 99.84%. This efficiency decrease was proportional to the load power increase of 97.28% at a 1200W load.

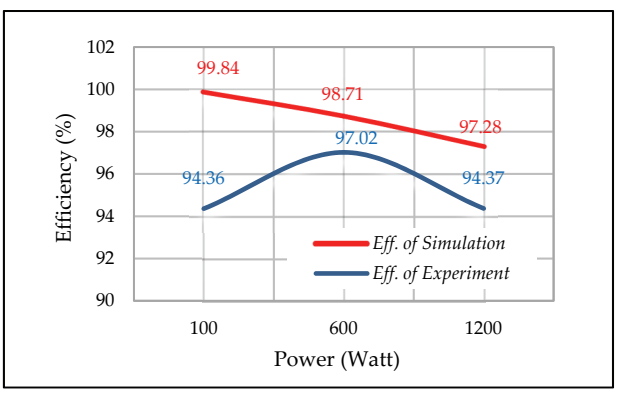
The THD value obtained from the proposed topology was better than that of the CMLI-RDC topology [19]-[26], [30]-[32]. The higher the number of output wave levels the lower the THD value. When compared with the CMLI-RDC inverter, the MSMLI topology has better performance based on the ratio of the output wave levels to the number of switches (L/NoS), as shown in Table V. The proposed MSMLI-CC topology has the highest L/NoS value of 3.87. In terms of the number of conduction switches, this topology is equivalent to

TABLE V
COMPARISON OF MSMLI AND CMLI-RDC RESULTS

Topology of RDC-MLI	DC Source	Switch		Output wave level	L/NoS
		Amount	Conduction		
MLI-DC Link [20, 21]	4	12	3-6	9	0.75
CMLI-MNS [19]	4	12	3-6	9	0.75
MLI-SSPS [22, 23]	4	13	3-6	9	0.69
MLI-SCSS [30]	4	12	3-6	9	0.75
MLM [31]	4	14	3-6	9	0.64
MLI-RV [24, 25]	4	12	4-7	9	0.75
MLI-2SELG [32]	4	12	4	9	0.75
CMLI-MNCS [26]	4	12	3	7	0.58
MSMLI *(proposed)*	**4**	**8**	**3-6**	**31**	**3.87**



(a)



(b)

Fig. 24. Characteristics at a resistive load of 48.3Ω. (a) Source power distribution. (b) Efficiency.

the CMLI-RDC topology, and the number of switches determines the efficiency of the inverter.

The use of a MLI with an asymmetric source is possible in PVs, especially in large power systems, due to the large number of PV panels that can be attached to asymmetric sources and the large number of sources for a MLI. While the number of switches used in a converter might be low, it should also be noted that some of the switches require a higher voltage rating in order to block the full DC link voltage. Thus, this should be taken into consideration when designing the converter.

V. CONCLUSION

The cascaded multilevel inverter proposed in this paper obtained fairly good results when compared with other topologies for certain power ranges. The proposed topology can generate 31 wave levels with only eight switches and four asymmetric DC sources. Results show that with a resistive load of 48.3Ω and an output power of 1200W, the total harmonic distortion THDv is 1.7%, the THDi is 1.6% and the efficiency is found to be 94.37%. In practice, a maximum efficiency of 97.02% was obtained at 600W of load power. One drawback of this topology is the occurrence of voltage surges in the inductive load due to the emf effect. However, by using capacitors on the dc bus, the emf effect can be minimized. The size of the capacitor used should be proportional to the reactive power of the load. Nevertheless, the proposed inverter can achieve high output levels with a minimal number of switches.

ACKNOWLEDGMENT

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