

Fault-Tolerant Control for 5L-HNPC Inverter-Fed Induction Motor Drives with Finite Control Set Model Predictive Control Based on Hierarchical Optimization

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Abstract

This paper proposes a fault-tolerant control strategy with finite control set model predictive control (FCS-MPC) based on hierarchical optimization for five-level H-bridge neutral-point-clamped (5L-HNPC) inverter-fed induction motor drives. Fault-tolerant operation is analyzed, and the fault-tolerant control algorithm is improved. Adopting FCS-MPC based on hierarchical optimization, where the voltage is used as the controlled objective, called model predictive voltage control (MPVC), the postfault controller is simplified as a two layer control. The first layer is the voltage jump limit, and the second layer is the voltage following control, which adopts the optimal control strategy to ensure the current following performance and uniqueness of the optimal solution. Finally, simulation and experimental results verify that 5L-HNPC inverter-fed induction motor drives have strong fault tolerant capability and that the FCS-MPVC based on hierarchical optimization is feasible.

Key words: Fault-tolerant capability, Finite control set model predictive control (FCS-MPC), Five-level H-bridge neutral-point-clamped (5L-HNPC) inverter, Hierarchical optimization

I. INTRODUCTION

Electric drive systems are exposed to rigorous operating conditions, which may lead to faults related to the induction motor and the inverter. A recent survey shows that about 38% of the faults in variable-speed drives are due to semiconductor power device failures [1]. Semiconductor power devices are considered to be the most fragile components of electric drives [2]. Fault-tolerant capability to improve reliability is effective for electric drives [3]-[5]. At present, inherent redundancy allowing for the fault-tolerant operation of drives with no additional hardware can be divided into two types of schemes. These schemes are multiphase machines [5]-[7] and multilevel inverters [8].

The multiphase machines with multiple sets of windings in

[5]-[7] have numerous advantageous features when compared to their three-phase counterparts. The number of phases decreases the stator current stress. These multiphase machines are used in applications that require lower noise and vibration. In addition, increasing the number of phases can offer stronger fault tolerance. However, these machines have higher manufacture costs and increased weight [3]. At present, multiphase drives are used for high-power low-voltage applications. Due to their mature motor body, three-phase motor drives are extensively utilized in modern industry. To improve output voltage levels and fault tolerance, multilevel converters (MCs) are an interesting technology for medium/high-voltage (MV/HV) and high-power applications [8]-[12]. The three-level neutral point clamped (3L-NPC) converter [13]-[15] with its good fault-tolerance, is still one of the most popular converter topologies for MV drive applications from 3kV to 4kV [14]. The five-level neutral point clamped (5L-NPC) converter in [10], [13]-[16] can realize an output voltage level of up to 6.6kV with standard semiconductors and no transformer. However, the 5L-NPC converter has difficulty in balancing the voltage of capacitors. A five-level H-bridge

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NPC (5L-HNPC) converter was presented in [17], [18]. When compared with the traditional 5L-NPC inverter, the output voltage amplitude of the 5L-HNPC inverter is double that of the traditional five-level inverter. In addition, when the power devices of the drive system break down, the reconfiguration inverter, due to its self-fault-tolerant function, becomes a 3L-NPC inverter.

Traditional modulation methods, such as sinusoidal modulation and space vector modulation, can be complex. During the last decade, model predictive control (MPC) has received a lot of attention [16]. MPC does not employ modulation. Instead, it relies on the switching state of power converters, where only a finite number of output states are available. These states are evaluated in order to select the optimal control objectives. This approach is known as finite-control-set MPC (FCS-MPC) [16]. The FCS-MPC strategy has been applied to a wide range of power converters [19]-[24], where it has several advantages such as a fast-transient response, simple implementation, and straightforward handling of nonlinearities and constraints [16]. Thus, fault-tolerant control with FCS-MPC is presented in [6], [20].

Since the conventional FCS model predictive current control (FCS-MPCC) [11] method selects optimal vectors as the next switching cycle through multiple current predictions, a novel FCS model-predictive voltage control (FCS-MPVC) method is realized by a single voltage prediction for the reference voltage, which can reduce the prediction algorithm.

There are many control objectives for multilevel inverters. These objectives include voltage jump limits, current following control, and switching frequency limits. When the traditional weighting factor method is used to optimize the performance function, multiple weighting factors need to be tuned [20]. Therefore, configuring a single weighting factor to meet the desired control objectives of a designer is difficult. Considering the conflict of each optimization performance index, when one performance indicator is over-optimized for a 5L-HNPC inverter, it is inevitable that the other performance indicators become worse. In addition, weighting factor tuning is difficult. At present, there is no uniform and effective solution. However, hierarchical control [25] can suppress the weighting factor and simplify the controller.

In this paper, the fault-tolerant operation of a 5L-HNPC inverter is analyzed, which has not yet been reported. A fault-tolerant control with FCS-MPVC based on hierarchical optimization for induction motor (IM) drives is proposed, which can reduce both the modulation algorithm and the MPC algorithm.

II. PROCEDURE ANALYSIS OF A 5L-HNPC CONVERTER

A. Structure Description

The 5L-HNPC converter topology is shown in Fig. 1 [19]. The rectifying part adopts three 12-pulse independent rectifiers,

which are formed by cascaded 6-pulse rectifiers whose AC input voltages have phase-difference of 30° . The inverter part is composed of three H-bridge NPC inverters. The mid-point of the 12-pulse rectifier can be connected with the neutral point of the DC-link capacitors. This can ensure the neutral point voltage balance and simplified control algorithm for the NPC inverter.

To avoid short circuits in one bridge arm, the drive signals of the upper and lower power devices are complementary. For example, the switches S_{a11} and S_{a13} , along with the switches S_{a12} and S_{a14} are controlled by complementary signals. Each H-bridge inverter consists of two three-level NPC half bridges to form a five-level H-bridge structure. Each of the three-level half bridges can output three levels ($V_{dc}/2$, 0 and $-V_{dc}/2$). Defining $E = V_{dc}/2$, one H-bridge inverter can output five levels (+2E, +E, 0, -E and -2E).

B. Operation Mode

Taking phase A as an example, in order to facilitate the presentation, the output voltage levels +2E, +E, 0, -E, -2E are numbered as the switching states $S_T = 2, 1, 0, -1, -2$, respectively. The operation modes corresponding to the switching states are given in Fig. 2. The analysis of the nine working modes is as follows.

Mode a ($S_T = 2, u_{a0} = +2E$): The power devices of $S_{11}, S_{12}, S_{23}, S_{24}$ are turned ON at the same time. Regardless of whether the output current i_a is positive or negative, both of the capacitors C_1 and C_2 can work. Thus, the capacitor voltages of C_1 and C_2 are equal.

Mode b ($S_T = 1, u_{a0} = +E$): The power devices of $S_{12}, S_{13}, S_{23}, S_{24}$ are turned ON at the same time. When the output current i_a is positive, the capacitor C_2 is discharged and the capacitor voltage u_{C2} decreases, and vice versa. Regardless of whether the output current i_a is positive or negative, the capacitor C_1 cannot work. Thus, the capacitor voltages of C_1 and C_2 are not equal.

Mode c ($S_T = 1, u_{a0} = +E$): The power devices of $S_{11}, S_{12}, S_{22}, S_{23}$ are turned ON at the same time. When the output current i_a is positive, the capacitor C_1 is discharged and the capacitor voltage u_{C1} drops, and vice versa. Regardless of whether the output current i_a is positive or negative, the capacitor C_2 cannot work. Thus, the capacitor voltages of C_1 and C_2 are not equal.

Modes d, e, f ($S_T = 0, u_{a0} = 0$): Both of the capacitors C_1 and C_2 cannot work. The capacitor voltages of C_1 and C_2 are not influenced by the output current.

Mode g ($S_T = -1, u_{a0} = -E$): The power devices of $S_{12}, S_{13}, S_{21}, S_{22}$ are turned ON at the same time. When the output current i_a is positive, the capacitor C_1 is discharged and the capacitor voltage u_{C1} decreases, and vice versa. Regardless of whether the output current i_a is positive or negative, the capacitor C_2 cannot work. Thus, the capacitor voltages of C_1 and C_2 are not equal.

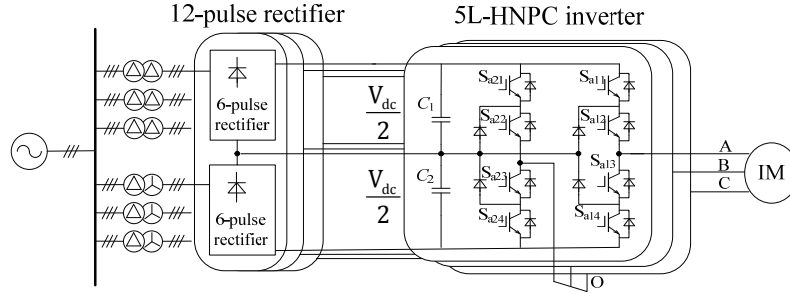


Fig. 1. 5L-HNPC inverter topology structure.

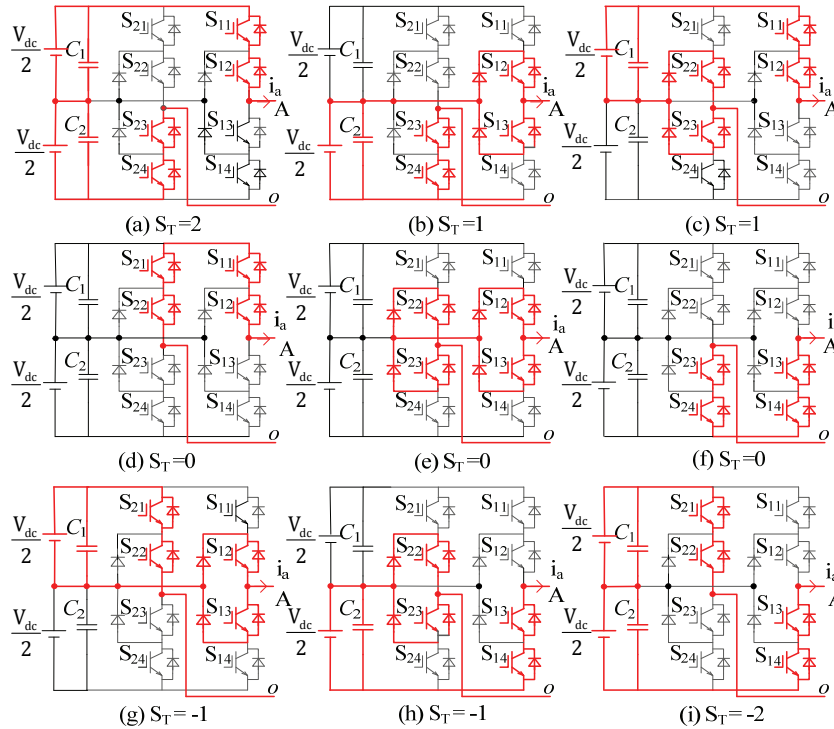


Fig. 2. Working modes of a 5L-HNPC inverter.

Mode h ($S_T = -1, u_{a0} = -E$): The power devices of $S_{13}, S_{14}, S_{22}, S_{23}$ are turned ON at the same time. When the output current i_a is positive, the capacitor C_2 is discharged and the capacitor voltage u_{C2} drops, and vice versa. Regardless of whether the output current i_a is positive or negative, the capacitor C_1 cannot work. Thus, the capacitor voltages of C_1 and C_2 are not equal.

Mode i ($S_T = -2, u_{a0} = -2E$): The power devices of $S_{13}, S_{14}, S_{21}, S_{22}$ are turned ON at the same time. Regardless of whether the output current i_a is positive or negative, both of the capacitors C_1 and C_2 can work. Thus, the capacitor voltages of C_1 and C_2 are equal.

To conclude, when $S_T = \pm 2$, there is only one operation mode. When $S_T = \pm 1$, there are two different working modes, whose working capacitors are different. To maintain the neutral-point voltage balance, the two different working modes must be reasonably chosen. When $S_T = 0$, there are three different working modes, where both C_1 and C_2

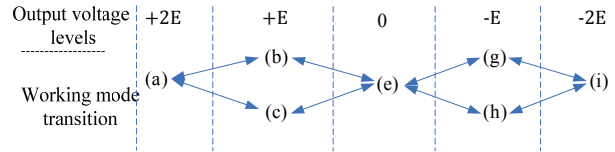


Fig. 3. Phase voltage and optimized transition for a 5L-HNPC converter.

work. Thus, there is no problem in terms of the neutral-point voltage balance. However, for reducing switching loss, the best choice is mode e.

The optimizing transition of the output states for a 5L-HNPC converter is shown in Fig. 3, which describes the transitions of the different modes and different voltage levels. Since each phase can output five levels for a three-phase 5L-HNPC converter, there are 125 kinds of space voltage vectors. A vector diagram of these space voltage vectors is presented in Fig. 4. One basic vector can correspond to a variety of switching combinations, which means that it possess

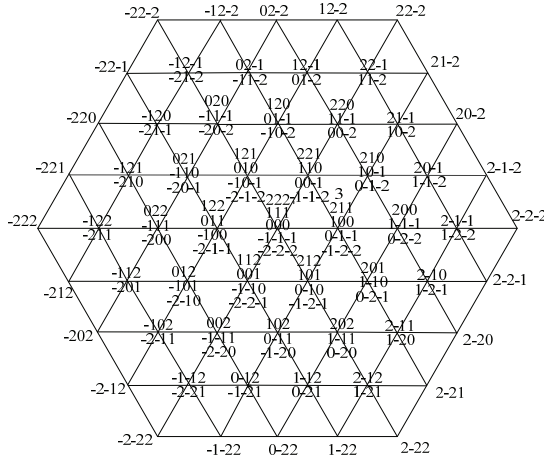


Fig. 4. Space vector distribution of a 5L-HNPC converter.

TABLE I
RELATIONSHIPS AMONG OPERATION MODE, WORKING BRIDGE ARM AND SWITCHING DEVICES

Operation mode	Working bridge arm			Switching device states		
	A	B	C	QS1	QS2	QS3
Normal mode	√	√	√	I	I	I
Fault-tolerant mode	Phase-A fault	×	√	√	II	I
	Phase-B fault	√	×	√	I	II
	Phase-C fault	√	√	×	I	I

state redundancy. After removing the redundant vectors, there are 61 kinds of basic space vectors.

III. FAULT-TOLERANT MODE ANALYSIS

A. Fault Tolerant Operation Analysis

There are two methods to realize the fault-tolerant operation of a 5L-HNPC inverter. These methods are adding switching devices and using power devices. The first method is shown in Fig. 5, where the switching devices QS1, QS2 and QS3 can disconnect a faulty phase to realize a fault-tolerant reconfiguration. The relationships among the operation mode, working bridge arm and switching devices are shown in Table I. For example, when a phase-C bridge fault occurs, the postfault inverter structure is presented in Fig. 6.

The second method is to realize fault-tolerance by controlling the power devices and ensuring that the fault phase outputs zero level, i.e. $S_T=0$ in Fig. 2, which means the 2-H bridge inverter is working. A detailed analysis is shown in Part B.

B. Fault-Tolerant Analysis

Taking phase-C as an example, the fault-tolerant working mode is analyzed. When the power device of S_{11} produces an open-fault, the inverter can choose from the working modes e or f in Fig. 7. When the power device of S_{11} produces a

TABLE II
RELATIONSHIP BETWEEN OPERATION MODE AND FAULT STATE

Fault devices	Fault states	Working modes
Power devices with tail 1 (S_{21}, S_{11})	Open fault	e, f
	Short circuit	d, f
Power devices with tail 2 (S_{22}, S_{12})	Open fault	f
	Short circuit	d, e
Power devices with tail 3 (S_{23}, S_{13})	Open fault	d
	Short circuit	e, f
Power devices with tail 2 (S_{24}, S_{14})	Open fault	d, e
	Short circuit	d, f

short-circuit fault, the inverter can choose from the working modes d or f in Fig. 7. When the power device of S_{12} produces an open fault, the inverter can choose the working mode f in Fig. 7. When a short-circuit fault of the power device of S_{12} occurs, the inverter can choose from the working modes d or e in Fig. 7.

The operational working modes corresponding to different switch faults are shown in Table II. From Table II, it can be inferred that the fault tolerant operation must satisfy a number of requirements. Both of the power devices with tail 1 and 3 cannot produce an open fault; both of the power devices with tail 2 and 3 cannot generate an open fault; both of the power devices with tail 2 and 4 cannot create an open fault. Otherwise, it cannot realize $S_T=0$. The self-fault-tolerance cannot add hardware, which increases the cost and weight. Therefore, the self-fault-tolerance of a 5L-HNPC inverter is researched in the paper.

For example, an open fault of power device S_{c21} emerges, from Table II, the open fault mode can choose from modes e and f. For mode e, its reconfiguration is shown in Fig. 8. It can be seen that the neutral point O is connected to the winding terminal C by controlling the rest of the power devices. The rest of the 2-H bridge NPC structure can output AC voltage with a mutual difference of 60° , which can produce a rotating magnetic field. Therefore, three-phase motor can realize fault-tolerant mode.

C. Vector Diagram Analysis

When a phase-C H-bridge arm breaks down, the fault tolerant topology is shown in Fig. 8, which can be redrawn as Fig. 9. From Fig. 9, it can be seen that the H-bridge inverter structure of phase-A and phase-B is not altered. However, the phase-C winding is connected with the neutral point O. Thus, the output voltage is changed from the motor phase-voltage under the normal operating mode and to the motor line-voltage under the fault-tolerant operation mode, which satisfies:

$$u_{ac} = u_{ao} = S_a E, \quad u_{bc} = u_{bo} = S_b E \quad S_a, S_b \in [-2 \ 2] \quad (1)$$

The motor winding voltages (u_{ac} and u_{bc}) have five-level changes. However, the line voltage u_{ab} is denoted as:

$$u_{ab} = u_{ac} - u_{bc} = (S_a - S_b) E \quad (S_a - S_b) \in [-4 \ 4] \quad (2)$$

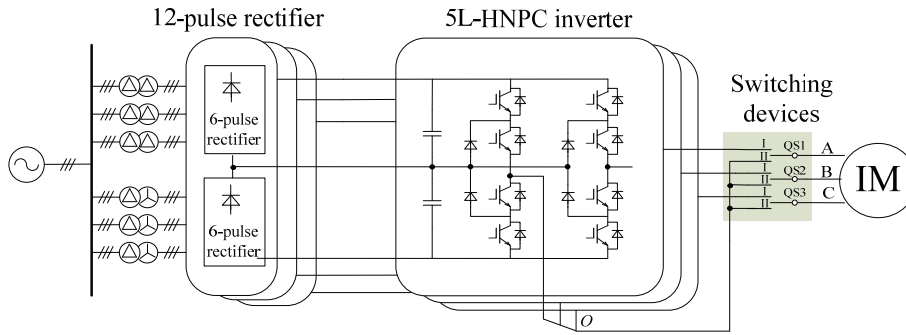


Fig. 5. Fault-tolerant reconfiguration by using an additional device.

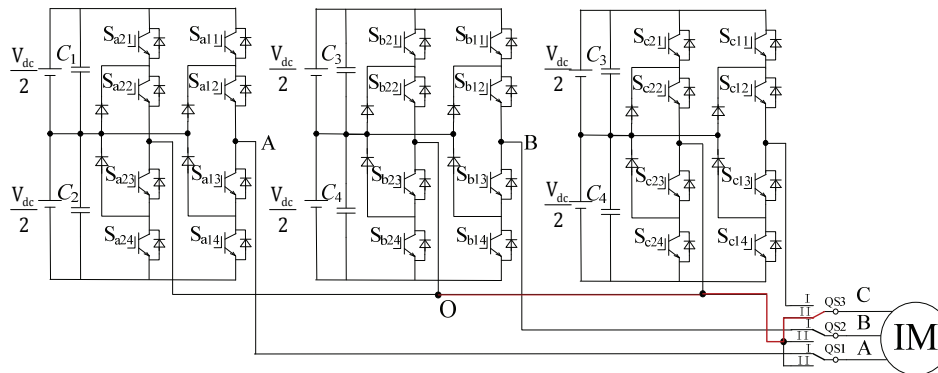


Fig. 6. Fault-tolerant reconfiguration of phase-A and phase-B through an additional device.

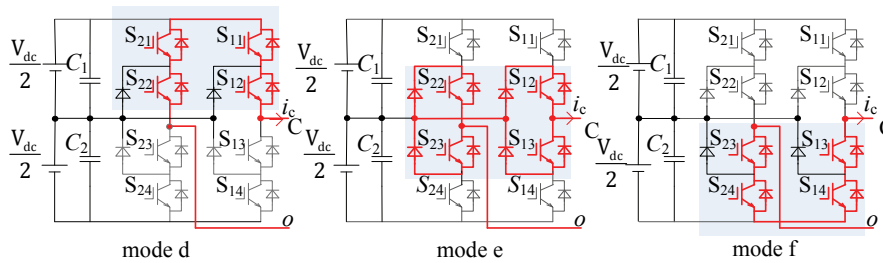


Fig. 7. Fault-tolerant reconfiguration mode.

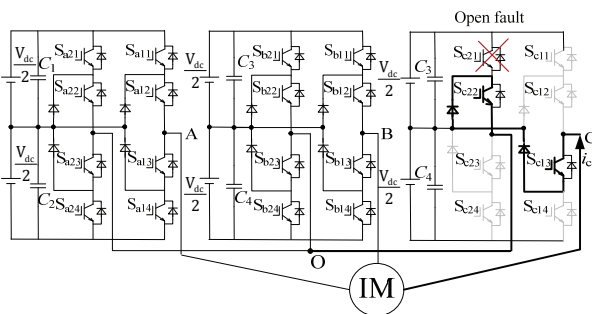


Fig. 8. Inverter reconfiguration under an open fault of phase-C.

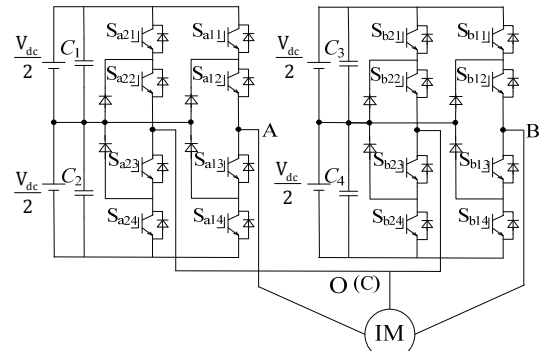


Fig. 9. Postfault reconfiguration of phase-A and phase-B.

From (2), it can be seen to realize nine levels.

A vector diagram of three-phase fault-tolerant operation in the $g-h$ coordinate system is shown in Fig. 10, where there are three fault-tolerant methods. These methods are AB fault tolerance, BC fault tolerance and AC fault tolerance. AB fault tolerance denotes when a fault of the phase-C H-bridge inverter

occurs, and the phase-A and phase-B H-bridge inverters drive the motor. BC fault tolerance describes when the phase-A H-bridge inverter breaks down, and the phase-B and phase-C H-bridge inverters drive the motor. AC fault tolerance is when the phase B H-bridge inverter generates fault, and the

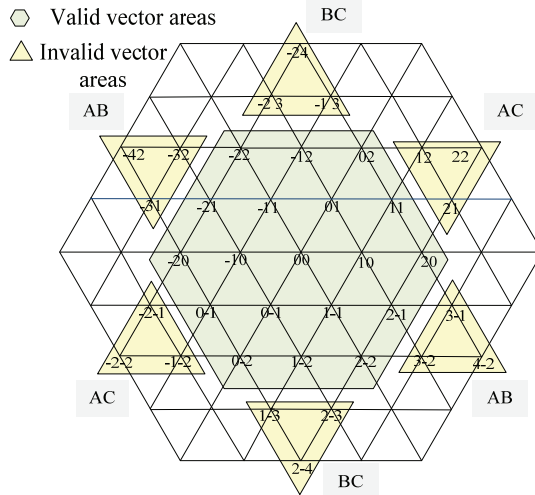


Fig. 10. Space vector distribution of a two-phase fault-tolerance inverter.

phase-A and phase-C H-bridge inverters drive the motor. From Fig. 10, it can be seen that valid vector distribution areas with 19 basic space vectors of the three fault-tolerant operation modes are consistent, and located in the three-level working areas. The invalid vectors are located in different five-level working areas with 25 space vectors.

The HNPC inverter only works in three-level areas under the fault-tolerant operation mode. The output-voltage amplitude of the postfault inverter is reduced to sixty percent of the normal mode. Thus, the running motor services in a de-rated capacity.

IV. ANALYSIS OF FAULT-TOLERANT CONTROL WITH FCS-MPVC BASED ON OPTIMIZATION FOR IM DRIVES

A. Prediction Model of the IM

Based on predictive current control and the voltage control principle, discrete-time models of the currents and voltages for induction motors are as follows.

The predictive current model is:

$$\begin{bmatrix} i_{s\alpha}(k+1) \\ i_{s\beta}(k+1) \\ \psi_{r\alpha}(k+1) \\ \psi_{r\beta}(k+1) \end{bmatrix} = (AT_s + I) \begin{bmatrix} i_{s\alpha}(k) \\ i_{s\beta}(k) \\ \psi_{r\alpha}(k) \\ \psi_{r\beta}(k) \end{bmatrix} + T_s BD \begin{bmatrix} S_a(k) \\ S_b(k) \\ S_c(k) \end{bmatrix} \quad (3)$$

where

$$A = \begin{bmatrix} -\frac{R'_s}{\sigma L_s} & 0 & \frac{k_r}{\sigma L_s T_r} & \frac{k_r \omega_r}{\sigma L_s T_r} \\ 0 & -\frac{R'_s}{\sigma L_s} & -\frac{k_r \omega_r}{\sigma L_s} & \frac{k_r}{\sigma L_s T_r} \\ \frac{L_m}{T_r} & 0 & -\frac{1}{T_r} & -\omega_r \\ 0 & \frac{L_m}{T_r} & \omega_r & -\frac{1}{T_r} \end{bmatrix},$$

$$B = \frac{1}{\sigma L_s} \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad D = \frac{2E}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix},$$

$$R'_s = R_s + R_r k_r^2, \quad k_r = L_m / L_r, \quad \sigma = 1 - L_m^2 / (L_s L_r),$$

$$T_r = L_r / R_r.$$

The meanings of the variables in matrix A and matrix B can be seen in [27].

The predictive voltage model can be written as:

$$\begin{cases} u_{s\alpha}^*(k) = \frac{\sigma L_s}{T_s} [i_{s\alpha}^*(k) - i_{s\alpha}(k)] - \frac{k_r}{T_r} \psi_{r\alpha}(k) - k_r \omega_r(k) \psi_{r\beta}(k) + r_o i_{s\alpha}(k) \\ u_{s\beta}^*(k) = \frac{\sigma L_s}{T_s} [i_{s\beta}^*(k) - i_{s\beta}(k)] - \frac{k_r}{T_r} \psi_{r\beta}(k) - k_r \omega_r(k) \psi_{r\alpha}(k) + r_o i_{s\beta}(k) \end{cases} \quad (4)$$

To compensate for the control system delay [26], the predictive voltage needs to push forward as follows:

$$\begin{cases} u_{s\alpha}^*(k+1) = \frac{\sigma L_s}{T_s} [i_{s\alpha}^*(k) - i_{s\alpha}(k+1)] - \frac{k_r}{T_r} \psi_{r\alpha}(k+1) - k_r \omega_r(k) \psi_{r\beta}(k+1) + r_o i_{s\alpha}(k+1) \\ u_{s\beta}^*(k+1) = \frac{\sigma L_s}{T_s} [i_{s\beta}^*(k) - i_{s\beta}(k+1)] - \frac{k_r}{T_r} \psi_{r\beta}(k+1) - k_r \omega_r(k) \psi_{r\alpha}(k+1) + r_o i_{s\beta}(k+1) \end{cases} \quad (5)$$

B. FCS-MPVC Based on Hierarchical Optimization

In order to avoid the problem of weighting factor tuning and reduce the computational burden of the system in the cost function, a FCS-MPVC based on hierarchical optimization is used in the paper.

To meet the requirement of low switching-frequency loss, there can be at most two vectors switching simultaneously between two-phase adjacent vectors. Based on the control method, the controller can be simplified to two layers of control. The first layer is the voltage jump limit that is realized by directly selecting the neighboring vectors. The second layer is the voltage following control to ensure the current following performance and the uniqueness of the optimal solution through an optimal control strategy.

The vector selection principle to meet the first layer voltage transition limit is analyzed as follows.

Assuming that the optimal switching vector is selected in the last period is denoted as $S(k) = (S_g(k) \ S_h(k))$. Then, the possible switching vector in the next period is indicated as $S(k+1) = (S_g(k+1) \ S_h(k+1))$.

All of the possible switching vectors are presented as follows.

$$\begin{cases} S(k+1)_1 = (S_g(k) \ S_h(k)) \\ S(k+1)_2 = (S_g(k)+1 \ S_h(k)) \\ S(k+1)_3 = (S_g(k)-1 \ S_h(k)) \\ S(k+1)_4 = (S_g(k) \ S_h(k)+1) \\ S(k+1)_5 = (S_g(k) \ S_h(k)-1) \\ S(k+1)_6 = (S_g(k)+1 \ S_h(k)-1) \\ S(k+1)_7 = (S_g(k)-1 \ S_h(k)+1) \end{cases} \quad (6)$$

And satisfying:

$$\begin{cases} S_g(k+1) \in [-2 \ 2] \\ S_h(k+1) \in [-2 \ 2] \\ |S_a(k+1)+S_b(k+1)| \leq 2 \end{cases} \quad (7)$$

For the three different fault-tolerant operations, AB fault-tolerant operation, BC fault-tolerant operation and AC fault-tolerant operation, the corresponding switch mapping formulas are as follows:

$$\begin{pmatrix} S_a(k+1) & S_b(k+1) & 0 \\ S_g(k+1)+S_h(k+1) & S_h(k+1) & 0 \end{pmatrix} \quad (8)$$

$$\begin{pmatrix} 0 & S_b(k+1) & S_c(k+1) \\ 0 & -S_g(k+1) & -(S_g(k+1)+S_h(k+1)) \end{pmatrix} \quad (9)$$

$$\begin{pmatrix} S_a(k+1) & 0 & S_c(k+1) \\ S_g(k+1) & 0 & -S_h(k+1) \end{pmatrix} \quad (10)$$

Define the cost function of the current as follows [19]:

$$g_i = |i_{\alpha}^* - i_{\alpha}^p(k+1)| + |i_{\beta}^* - i_{\beta}^p(k+1)| \quad (11)$$

Assuming that the current reference $i_{\alpha\beta}^*$ corresponds to the reference voltage prediction $v_{g,h}^*$ in the gh coordinate system, from (3) and (11), the following can be obtained [19]:

$$\begin{aligned} & |i_{\alpha}^* - i_{\alpha}^p(k+1)| + |i_{\beta}^* - i_{\beta}^p(k+1)| \\ &= \frac{T_s}{L} \left((v_g^* - v_g(k+1)) + \frac{1}{2}(v_h^* - v_h(k+1)) + \frac{\sqrt{3}}{2}|v_h^* - v_h(k+1)| \right) \end{aligned} \quad (12)$$

where $i_{\alpha\beta}^p(k+1)$ denotes the current prediction corresponding to the optimized switching vector $v_{g,h}(k+1)$.

From (12), the cost function of the voltage following can be described as:

$$g_v = \left| (v_g^* - v_g(k+1)) + \frac{1}{2}(v_h^* - v_h(k+1)) + \frac{\sqrt{3}}{2}|v_h^* - v_h(k+1)| \right| \quad (13)$$

From (13), it can be seen that the voltage following is equivalent to the current following.

The reference voltage predictions in the $\alpha\beta$ coordinate system can be used to directly obtain the voltage predictions of $u_{sg}^*(k+1)$, $u_{sh}^*(k+1)$ through the coordinate transformation. The predictive value of the reference voltage can be directly used in the $\alpha\beta$ coordinate system. From (7), (12) and (13), the voltage following optimization performance function can be redefined as:

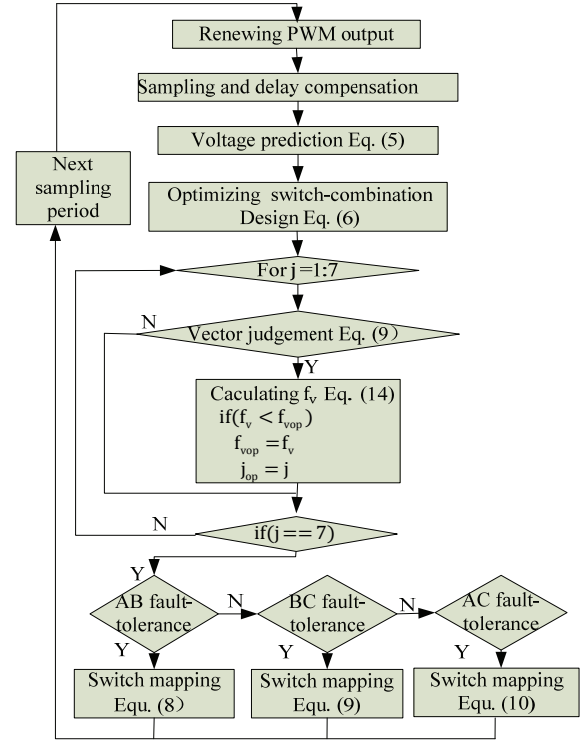


Fig. 11. Flow diagram of a fault-tolerant control algorithm with FCS-MPVC.

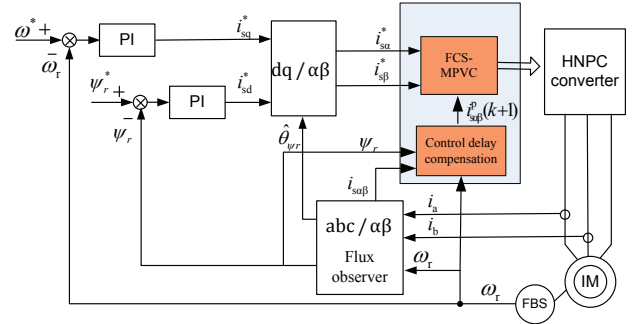


Fig. 12. Drive system structure diagram.

$$\begin{aligned} f_v = & \left| \frac{3}{2E} u_{sa}^*(k+1) - (S_g(k+1) + \frac{1}{2} S_h(k+1)) \right| + \\ & \left| \frac{3}{2E} u_{sb}^*(k+1) - \frac{\sqrt{3}}{2} S_h(k+1) \right| \end{aligned} \quad (14)$$

From the above analysis, a flow diagram of the fault tolerant control algorithm with FCS-MPVC is shown in Fig. 11. In the gh coordinate system, the FCS-MPVC strategy avoids a lot of repetitive prediction algorithms, which is reduced to 7 times.

C. Control Strategy of the Drive System

In order to realize decoupling control of the excitation component and the torque component, and to give full play to the advantages of FCS-MPC, an induction motor control system based on FCS-MPVC is built, as shown in Fig. 12. In

TABLE III
PARAMETERS OF THE INDUCTION MOTOR

Parameters	Value	Parameters	Value
Rated power (kW)	5.5	Stator resistance (Ω)	1.55
Rated voltage (V)	380	Rotor resistance (H)	0.692
Rated current (A)	11.5	Magnetic inductance (H)	0.133
Pole pairs	2	Stator leakage inductance (H)	0.0054
Rated torque (Nm)	35	Rotor leakage inductance (H)	0.0054

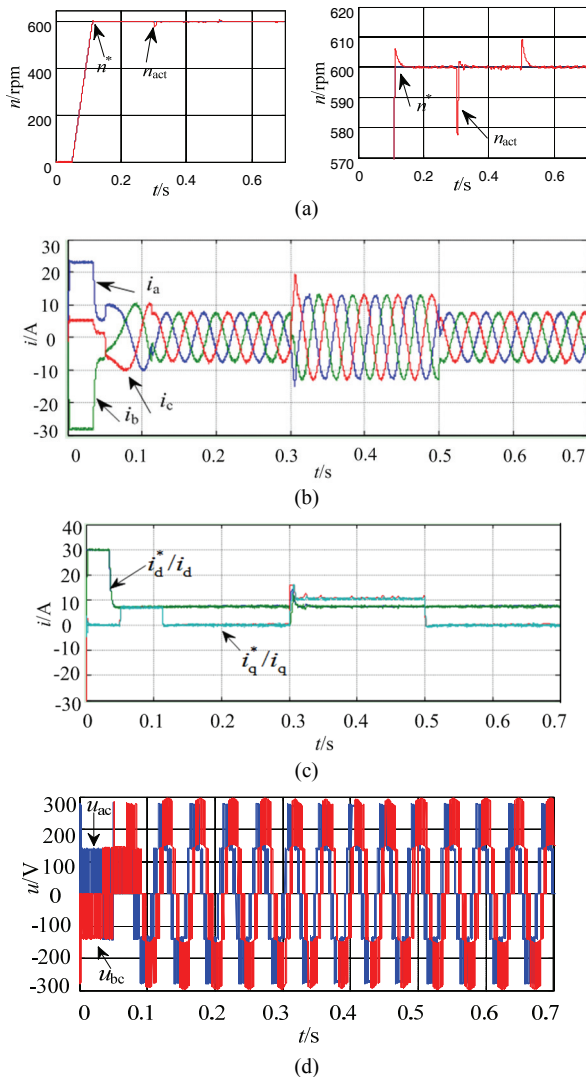


Fig. 13. Simulation results of the motor loading and unloading process under the fault-tolerant mode. (a) Reference speed n^* and actual speed n_{act} . (b) Three-phase stator current waveform. (c) Reference excitation current i_d^* , actual excitation current i_d , reference torque current i_q^* and actual torque current i_q . (d) Two-phase winding voltage.

the control strategy, the FCS-MPVC single-loop is used to replace the two inner current loops and PWM modulation in the traditional control system to greatly simplify the controller. The design of the outer loop and magnetic chain observer in

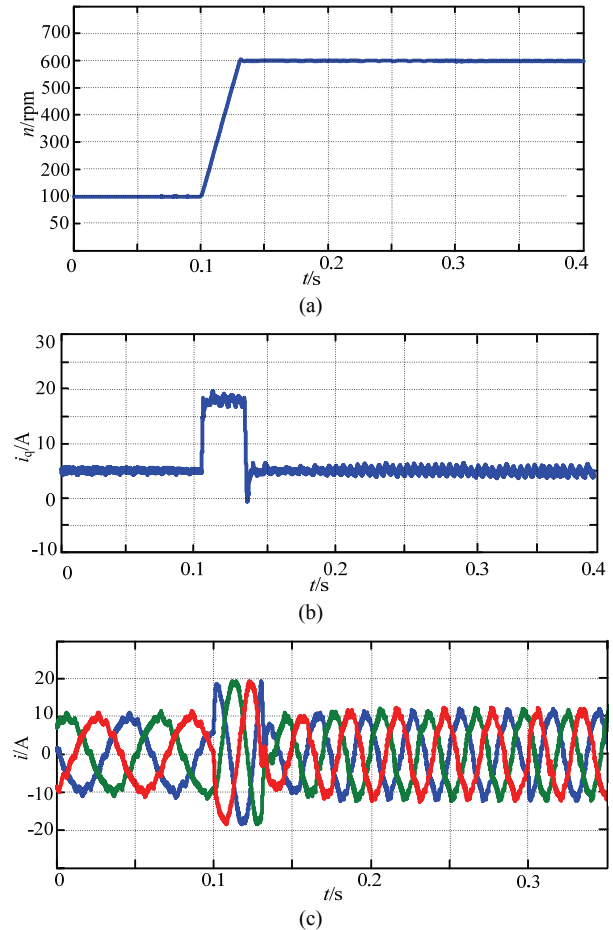


Fig. 14. Simulation results of motor acceleration under the fault-tolerant mode. (a) Waveform of the speed n from 100rpm to 600rpm. (b) Waveform of the torque current i_q . (c) Three-phase stator current waveform.

the system is consistent with the traditional FOC control system. In the control strategy, the key is the design of the FCS-MPVC controller.

V. SIMULATION AND EXPERIMENTAL RESULTS

When an open fault of the phase-C bridge occurs, the reconfiguration structure is shown in Fig. 8. Table III presents the parameters of the induction motor.

Simulation results of the drive system under the fault tolerant mode are presented and analyzed, as shown in Fig. 13 and Fig. 14.

When the reference speed is 600rpm, the sudden load torque is 30Nm when $t=0.3$ s. The load torque is suddenly reduced to zero when $t=0.5$ s. Simulation results are shown in Fig. 13. Fig. 13(a) presents the speed and its local amplification. From Fig. 13(a), it can be seen that the starting process has almost no overshoot and that the speed fluctuation is small. The three-phase stator current waveform is shown in Fig. 13(b), and it can be seen that the current is sinusoidal. Fig. 13(c) shows the good following performance of the excited

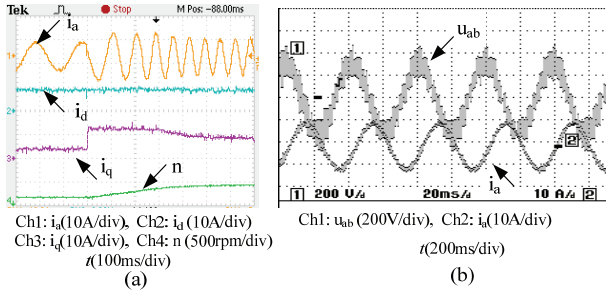


Fig. 15. Experimental waveforms of the drive system under normal operation. (a) Acceleration waveforms of the phase current i_a , d-q current and rotor speed n . (b) Steady waveforms of the winding line-voltage and current.

current and torque current. The two-phase winding voltage of the fault-tolerant structure is presented in Fig. 13(d). From Fig. 13(d), it can be seen that it operates in the 3-level region and that the two-phase voltages have a mutual difference of 60° in their phase. The simulation results reveal that the fault tolerance of the 5L-HNPC inverter is feasible and that the drive system has good performance.

Fig. 14 shows simulation results of motor acceleration when the load torque is 12Nm. Fig. 14(a) presents the speed from 100rpm to 600rpm. Fig. 14(b) shows a torque current waveform. It can be seen that the torque ripple is small. Fig. 14(c) presents stator currents. It can be seen that the three phase stator currents are spaced 120° apart and are sinusoidal.

A floating-point digital signal processor (DSP, TMS320 F28335) is used to select the optimal switching state and a field programmable gate array (FPGA) is used to generate an impulse to control the switches in the experimental platform built based on Fig. 12. Fig. 15 shows experimental waveforms of the drive system under normal operation from no load to load-on. Fig. 15(a) shows an acceleration waveform of the drive system under normal conditions. In the dynamic process, the load current i_a is seen to be sinusoidal, the excitation component i_d is kept constant, and the rotor speed n is non-overshoot. Steady state waveforms of the winding line-voltage and the winding current are presented in Fig. 15(b). It can be seen that the line-voltage has 9 levels and that the winding current is sinusoidal with low distortions. From Fig. 15, it can be seen that the drive system is feasible under normal operation.

When one power device of a phase-C H-inverter breaks down, fault-tolerant operation waveforms of phase A and phase B are shown in Fig. 16. Fig. 16(a) shows a dynamic process waveform of the motor speed from 100rpm to 600rpm. It can be seen that the sinusoidal degree of the winding current and the dynamic response of the rotor speed are better, and that the excitation component i_d is basically stable. Output voltage waveforms of phase-A and phase-B are shown in Fig. 16(b). The winding voltages have five levels. However, they correspond to the line voltages of phase-AC and phase-BC. The postfault reconfiguration can

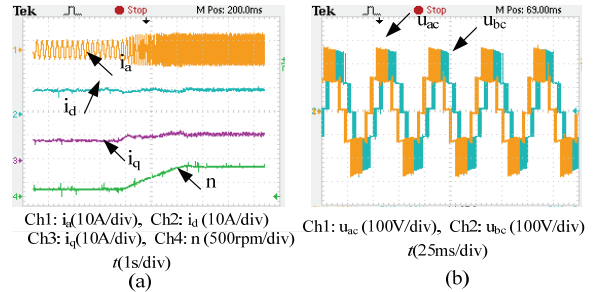


Fig. 16. Experimental waveforms of a drive under the fault tolerant mode. (a) Phase current i_a , d-q current and rotor speed n under the dynamic process. (b) Winding voltages u_{ac} and u_{bc} under the steady state.

be equivalent to a three-level inverter. Experimental results indicate that the two-phase fault tolerant drive can work steadily in the three-level region.

From the above statement, it can be seen that the proposed fault-tolerant control with FCS-MPVC based on hierarchical optimization is feasible.

VI. CONCLUSION

The fault-tolerant operation of a 5L-HNPC inverter is analyzed in detail, and a fault-tolerant control with FCS-MPVC based on hierarchical optimization is proposed. The fault-tolerant reconfiguration structure is realized by controlling the fault-bridge switch itself. The proposed fault-tolerant control strategy can simplify the mathematic calculations and resolve the problem of weighting-factor tuning. The fault tolerant mode cannot change the structure of a 5L-HNPC inverter or effect the dynamic performance of the drive system. The 5L-HNPC inverter can operate in the three-level area under the double bridge fault tolerant mode. Simulation and experimental results verify that the fault-tolerant operation of a 5L-HNPC inverter based on the proposed control strategy is feasible.

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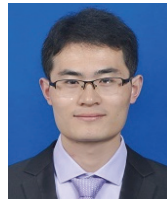
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