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Optimal Selection of Arm Inductance and Switching Modulation for Three-Phase Modular Multilevel Converters in Terms of DC Voltage Utilization, Harmonics and Efficiency

Ali Osman Arslan[†,*], Mehmet Kurtoğlu[*], Fatih Eroğlu[*], and Ahmet Mete Vural[*]

[†,*]Department of Electrical and Electronics Engineering, Gaziantep University, Gaziantep, Turkey

Abstract

The arm inductance (AI) of a modular multilevel converter (MMC) affects both the fault and circulating current magnitudes. In addition, it has an impact on the inverter efficiency and harmonic content. In this study, the AI of a three-phase MMC is optimized in a novel way in terms of DC voltage utilization, harmonics and efficiency. This MMC has 10 submodules (SM) per arm and the power circuit topology of the SM is a half-bridge. The optimum AI is adopted and verified in an MMC that has 100 SMs per arm. Then the phase shift (PS) and phase disposition (PD) pulse width modulation (PWM) methods are investigated for better DC voltage utilization, efficiency and harmonics. It is found that similar performances are obtained for both modulation techniques in terms of DC voltage utilization. However, the total harmonic distortion (THD) of the PS-PWM is found to be 0.02%, which is slightly lower than the THD of the PD-PWM at 0.16%. In efficiency calculations, the switching and conduction losses for all of the semiconductor are considered separately and the minimum efficiency of the 100-SM based MMC is found to be 99.62% for the PS-PWM and 99.64% for the PD-PWM with the optimal value of the AI. Simulation results are verified with an experimental prototype of a 6-SM based MMC.

Key words: Modular multilevel converter, Modulation techniques, Multi-level power converter, Optimal arm inductance selection

I. INTRODUCTION

High voltage direct current (HVDC) transmission is used to connect power station dispatches that are more than 800-km apart, offshore power plants to a main grid and systems that have several frequencies/voltage levels [1], [2]. Despite the limitations of semiconductor devices, modular (that allow series/parallel connection) type multilevel inverters are required for reliable HVDC systems. In the last decade, the MMC was proposed by A. Lesnicar and R. Marquardt to cope with the problems of HVDC systems [3]. Using a MMC, desired high voltage and power capabilities can be achieved thanks to modular and scalable nature of MMCs. They have high efficiency and low harmonics in middle/high voltage/power applications. They can be switched at low frequencies due to an increased number of SMs. In addition, they do not need a dc link capacitor, passive filter or step up transformer [4].

The application and study of the MMC are being continuously expanded [5]. Some of them are medium voltage motor drivers [6], STATCOMs [7]-[9], FACTS applications [10], power electronic transformers [11], HVDC applications [12], [13], multi terminal DC systems [14], PV systems [15], onshore and offshore wind energy systems [16], battery technologies [17], electrical vehicles [18], railway traction drives [19] and electric ship implementation [20].

The MMC contains N-SM which can be designed as a half-bridge or H-bridge connected in series with an AI in each arm of the MMC [21]. A half-bridge based SM is constructed with two semiconductor switches/diodes and a SM capacitor. The design of the MMC is critical to achieve the desired voltage, power, efficiency and harmonic performances.

The input DC link voltage, output AC voltage, output power, number of SMs in an arm, switching device, SM capacitor

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[†]Corresponding Author: aoarslan@gantep.edu.tr
Tel: +90-342-317-2149, Fax: +90-342-360-1103, Gaziantep University
[*]Department of Electrical and Electronics Engineering, Gaziantep University, Turkey

and AI can be listed as the designable parameters of the MMC power circuit. Studies usually focus on the key components of the MMC, which are the SM capacitor and the AI, to cope with the problems of MMCs.

The SM capacitance in the MMC is mainly selected according to the voltage fluctuation limit of the capacitor [22]. There are many capacitors in a single arm and they must be balanced. Unbalanced capacitor voltages result in the circulating current passing through an arm and extra losses. Many researchers have been trying to solve this problem by adding extra inner controllers and changing the applied PWM technique [23]-[27]. An interesting and effective solution is circulating current injection to decrease capacitor voltage fluctuations in low frequency motor drive applications [28].

AI is another key component of MMC power circuits. In many studies, the arm inductor has been used to limit the short circuit fault current and to minimize the circulating current [22], [29]. Circulating current contains a dominant second harmonic proportional to the amplitude of the output ac current [30]. Methods have been proposed to eliminate the second order harmonic of the circulating current. However, they are unable to prevent switching frequency harmonics and high frequency harmonic components of the circulating current. These components can only be restricted by using the AI [31]. On the other hand, many detailed fault current analyses are scheduled via several case studies and topologies in terms of the impact of the arm inductor. Fault current can be controlled by applying control engineering methods on H-bridge SM based MMCs [13], [32], [33]. However, there are no studies available on the impact of the arm inductor on the efficiency, THD and output power of MMCs in the literature.

The main contribution of this study is optimizing the AI by improving performance parameters of MMC such as the generated phase voltage, efficiency, and THD of the phase voltage. To that end, a 3-phase, wye-connected, 100 kV DC link input voltage, 100-SM based arm MMC is contemplated and operated in a simulation environment. First, the optimal solution step size is found by considering the accuracy and reliability of the simulation results by varying the step size. Then by considering the optimal values of the AI, dc voltage utilization and THD of phase voltage are demonstrated with respect to the modulation index (m-value) for both PS-PWM and PD-PWM. The switching and conduction losses of the semiconductors, output power, efficiency and harmonic performance of the MMC are compared by varying the load current at a unity power factor for the PS-PWM and PD-PWM. In the end, it is shown that the proposed methodology for choosing the optimal AI gives significant results in terms of power efficiency and THD. Simulation results are verified with experimental results on a 6-SM based prototype.

This paper is organized as follows. Section II introduces the general circuit topology of the MMC and the selection of the parameter design for the SM capacitor and AI. In section III, the semiconductor loss calculation is explained for the IGBTs, MOSFETs and diodes used in this study. The proposed AI selection method is explained in detail in section IV. Simulation results are given for various case studies in section V. Experimental results are given and compared to simulation results in Section VI. Finally, section VII some conclusions.

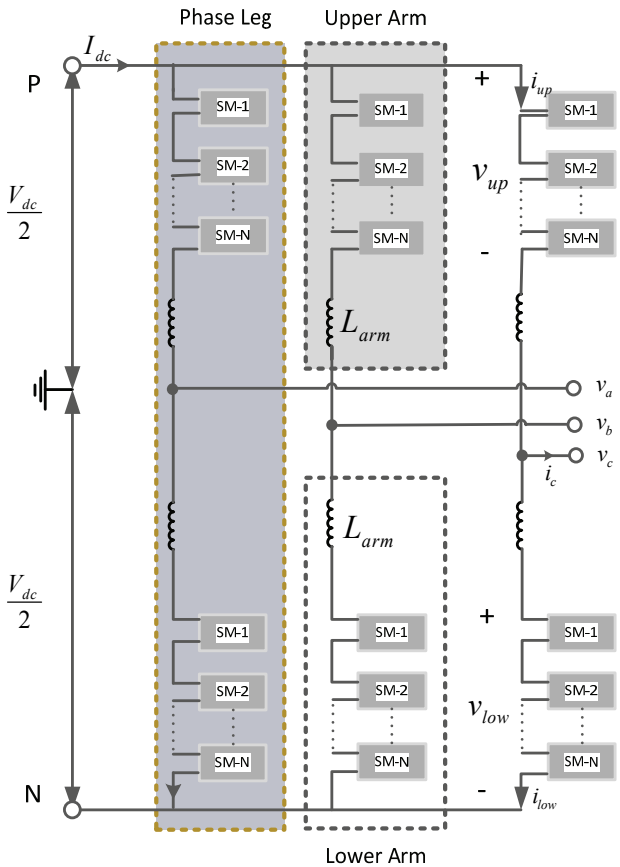


Fig. 1. General circuit topology of an MMC.

II. General Structure of the MMC

The general power circuit structure of a 3-phase MMC is shown in Fig. 1 [4]. There are two series connected DC voltage sources at the input side of the MMC. The connection point of the DC voltage sources is grounded. Each phase is called a phase leg that consists of an upper and a lower arm. There are cascaded N-SMs with an AI in an arm. The power circuit topology of the SMs can be half-bridge (HB) or full-bridge (FB). Consequently, 3-phase MMCs can be combined with 6N-SM in total. The output AC voltage terminals of the MMC are defined as va, vb and vc.

For the HB connection, there are two semiconductor switches, two inverse connected parallel diodes and a SM capacitor. If the SM is bypassed, the voltage out is zero or (+VC).

TABLE I
3-PHASE MMC DESIGN PARAMETERS

Name	SYMBOL	VALUE
DC voltage	V_{DC}	100-kV
Power	P_{out}	60-MW
Ac phase voltage in RMS	V_{phase}	35-kV
Fundamental frequency	f_f	50-Hz
Carrier frequency	f_c	150-Hz
Number of SM per arm	N	100-piece
SM capacitance	C_{SM}	1-mF
SM voltage	V_{SM}	1-kV
Optimum arm inductance	L_{arm}	10-mH
Quality factor of the AI	Q	7,85-H.Hz/Ω

The SM is charged in case of capacitor current entering the capacitor and discharged when the capacitor current exits the capacitor. Switch 1 or switch 2 must be in the off state to avoid a short circuit on the SM capacitor at any time.

The AI can suppress the circulating current and limit the short-circuit fault current filter of the output voltage when contemplated together via an internal resistor [34]. If the optimal value of the AI is used, the efficiency and THD performances of the inverter are maximized. The minimum AI value is calculated by considering the maximum current change in the phase by using Equ. (1) as:

$$\frac{di_{arm}}{dt} = \frac{V_{DC}}{2L_{arm}} \tag{1}$$

where i_{arm} is the arm current, and V_{DC} is the DC link voltage. This value is the minimum value of the AI. It may not be the optimum value for obtaining good performance for the THD and efficiency of the MMC. Its optimum value can be found by applying the given method in section 4.

The SM capacitor value can be calculated by taking into consideration the energy of the SM and DC link voltage in Equ. (2) [29].

$$C_{SM} = \frac{N.E_{C,\max}}{3V_{DC}{}^2} \tag{2}$$

where $E_{C,max}$ is the maximum stored energy in all of the capacitors, C_{SM} is the SM capacitance, and N is the number of SMs.

All of the design parameters of the three-phase 100-SM based MMC are given in Table I. Since a semiconductor switch DIM1200NSM17-E000 is selected, its forward current is 1200-A and its reverse blocking voltage is 1.7-kV. The module contains both an IGBT and an inverse parallel connected diode.

III. ESTIMATION OF THE SEMICONDUCTOR LOSSES

The overall efficiency of a system demonstrates the reliability and quality of the designed system. Power loss is the difference between the input power and the output power. Meanwhile, efficiency is the ratio of the output power to the input power. The power loss of the inverter can be calculated as switching losses and conduction losses. Snubber losses are neglected because they are not generally used with IGBTs [35]. Due to the low leakage current for the switching devices, the off-state losses are ignored [36]. The conduction loss of the diode, MOSFET and IGBT can be calculated by Equ. (3).

$$P_{con\_loss} = \frac{1}{T}\int_0^T (V_{on} + r_{on}i_F)i_F dt \tag{3}$$

where T is calculation period, V_{on} is the on-state voltage drop, r_{on} is the on-state resistance, and i_F is the forward current. In order to obtain reliable results, T is selected as 0.04 sec for a 50-Hz system. V_{on} is 1.0-V, 1.3-V and 0.8-V, and r_{on} is 0.007-Ω, 0.017-Ω and 0.01-Ω for the diode, MOSFET and IGBT, respectively [35].

The switching loss of the semiconductor devices is the sum of the rise and fall time losses of the diodes and MOSFET or IGBTs. For the 100-SM based MMC, a DIM1200NSM17-E000 is used as the switching device that contains two packs of a IGBT and a reverse parallel connected diode. The on-state, off-state and reverse recovery energy loss curves of the diode and IGBT are given in datasheets. The curves are approximated with second order polynomials [37]. The estimated equations are found as given in Eqns. (4)-(6).

$$E_{rise-IGBT} = 10^{-6}\left(\frac{V_{off}}{900}\right)(-0.048i_F^2 + 390i_F + 71.4) \tag{4}$$

$$E_{fall-IGBT} = 10^{-6}\left(\frac{V_{off}}{900}\right)(0.025i_F^2 + 318.7i_F + 595.2) \tag{5}$$

$$E_{fall-diode} = 10^{-6}\left(\frac{V_{off}}{900}\right)(-0.2i_F^2 + 490.2i_F + 16190.5) \tag{6}$$

where V_{off} is the off-state voltage of the semiconductor device at the rise and fall times [35]. $E_{rise\text{-}diode}$ is zero since the diode turns on instantly at zero voltage [38]. An IRFZ44N power MOSFET is used in the experimental prototype. The switching energy losses of the MOSFET are calculated using the datasheet of the device gives Eqns. (7), (8).

$$E_{rise-MOSFET} = V_{off}i_F\left(\frac{t_{rise}}{2}\right) \tag{7}$$

$$E_{fall-MOSFET} = V_{off}i_F\left(\frac{t_{fall}}{2}\right) \tag{8}$$

where t_{rise} and t_{fall} are the rising time and falling times of the MOSFET.

In PSCAD, by using the edge detector block, the rise and fall instants of the semiconductors are captured while configuring the rising and falling edge specification of the block [39]. As a result, the switching losses of the diode-IGBT based module can be obtained by summing up Eqns. (4)-(6) and dividing by T for all of the modules in the inverter given in Equ. (9).

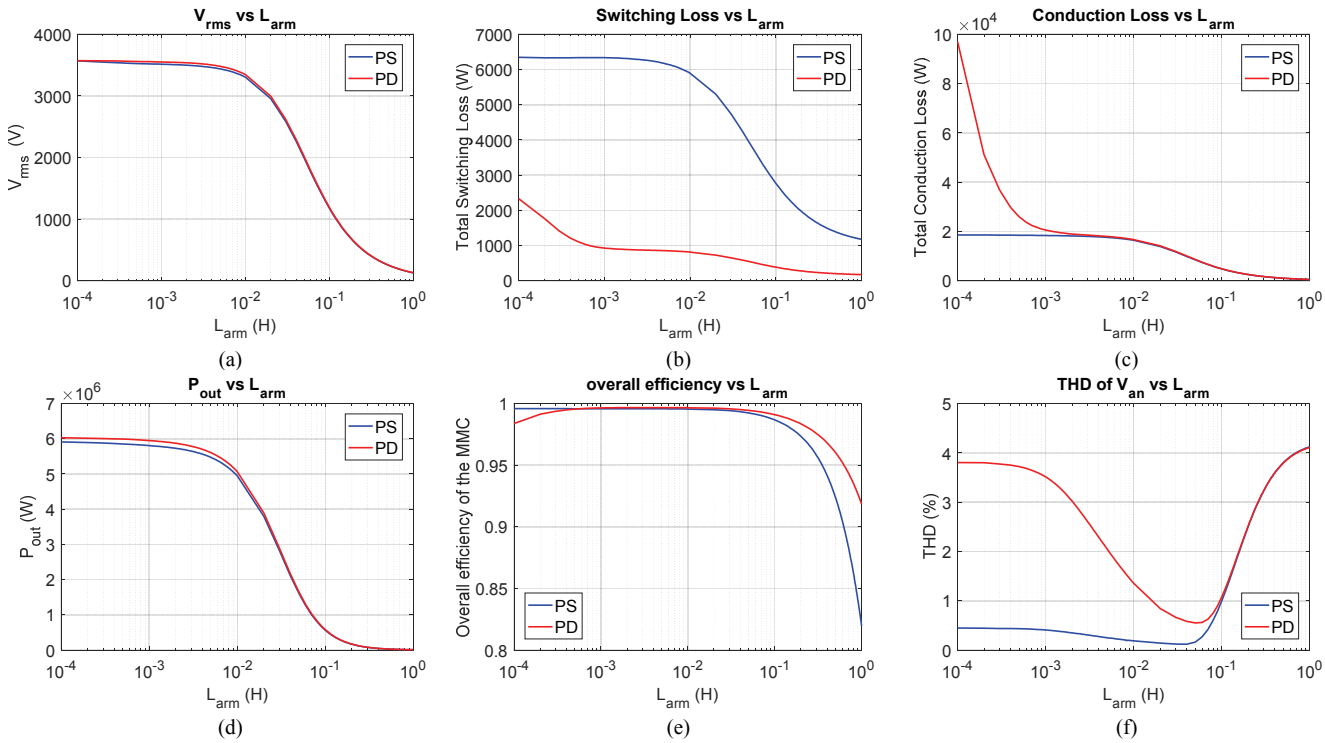


Fig. 2. Optimum AI selection for PS-PWM and PD-PWM considering the: (a) Phase voltage. (b) Switching loss. (c) Conduction loss. (d) Output power. (e) Overall efficiency. (f) THD of the phase voltage.

$$P_{sw\_loss} = \frac{1}{T}\sum_{n=1}^{K}(E_{rise-IGBT,n} + E_{fall-IGBT,n} + E_{fall-diode,n} \quad (9)$$

where K is the total number of switchings of the IGBT in a calculation period of 0.04 sec [39].

The switching loss of the diode-MOSFET based module is calculated by summing up Eqns. (6)-(8) and dividing by T for all of the modules in the inverters given in Equ. (10).

$$P_{sw\_loss} = \frac{1}{T}\sum_{n=1}^{K}(E_{rise-MF,n} + E_{fall-MF,n} + E_{fall-diode,n} \quad (10)$$

The total semiconductor losses are found by summing the conduction losses and switching losses for all of the semiconductor devices in the MMC given in Equ. (11).

$$P_{semiconductor\_loss} = P_{con\_loss} + P_{sw\_loss} \quad (11)$$

IV. Proposed Optimal ARM Inductance Selection Method for an MMC

Optimal selection of the AI by considering the efficiency and THD is the most critical part of MMC design. For this purpose, this work studies an MMC with 10-SM based arm since to the simulation of the designed MMC with 100-SM based arm takes so much time. For example, 2 periods of the simulation with one value of the AI takes about 1-day for the PS-PWM and 6-hours for the PD-PWM with a 2-micro second solution step for the MMC with a 100-SM based arm. In the novel method, 10-SM based MMC is operated with 10-kV input DC voltage. The value of the AI is changed from 10-4-mH 100-mH by increasing it by 10-4-mH to find its optimum value. The generated phase voltage, load current, switching and conduction losses of the semiconductor devices, output power, overall efficiency and THD results are plotted in log scale at a constant resistive load for PS-PWM and PD-PWM in Fig. 2.

When the AI is lower than 1-mH, the total loss of the semiconductor devices is high. Therefore, the overall efficiency is less than 99% and the THD of the generated voltage is high for the PD-PWM. When the AI is greater than the 10-mH, the generated phase voltage is gradually decreased. Then the overall efficiency and THD also decrease. When the AI is greater than the 100-mH, the THD increases rapidly and the overall efficiency is decreased from 98% to 82%. In addition, the generated active power is decreased to 15% of its rated value. The optimum value of the AI should be selected between 1-mH and 10-mH considering the following criteria; high voltage generation, high output power supplying, high efficiency and low THD. The optimal value of the AI is selected as 10-mH for a 10-SM based MMC with a 10-kV input. This value can also be used for a 100-SM based MMC with a 100-kV input.

V. Simulation Studies

The hardware and software programs that are used for the simulation studies are explained in this section. The computer

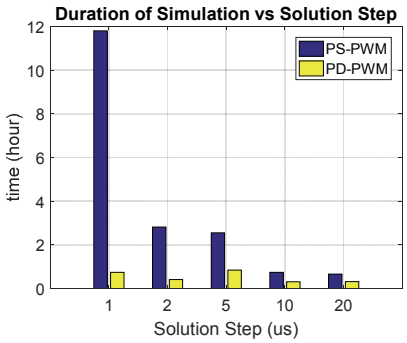


Fig. 3. Duration of the simulation with respect to the solution step.

TABLE II
ACCURACY OF THE OUTPUT PARAMETERS AND SIMULATION DURATION WITH RESPECT TO THE SOLUTION STEP, PS-PWM

Δt (us)	Duration(time)	THD(%)	V_{an} (V)
1	11:48:03	0.021607	35372.95
2	02:49:01	0.022199	35339.00
5	02:32:56	0.056767	35371.70
10	00:44:25	0.108950	35303.55
20	00:39:36	0.183761	35352.65

TABLE III
ACCURACY OF THE OUTPUT PARAMETERS AND SIMULATION DURATION WITH RESPECT TO THE SOLUTION STEP, PD-PWM

Δt (us)	Duration(time)	THD (%)	V_{an} (V)
1	00:44:15	0.132460	35471.15
2	00:24:52	0.132724	35461.85
5	00:50:26	0.130405	35406.35
10	00:18:18	0.137890	35354.85
20	00:18:49	0.162703	35349.55

has an Intel i7-4700 HQ @2.4-GHZ CPU running a 64-bit Windows 10 operating system. PSCAD 4.2.2 is used for the simulation program. The solution step of the simulation is 2-micro second for all of the case studies except case study-1. For all of the case studies, the fundamental frequency (f_f) is 50-Hz, the carrier frequency (f_c) is 150-Hz and the m-value is one. For the designed MMC, four case studies are simulated. The performance with the PD-PWM is almost same at that with POD-PWM and APOD-PWM. For this reason, the POD-PWM and APOD-PWM results are not given in this study. All of the voltage/current values are given in RMS. The THD is evaluated by considering the first thirty-one harmonic orders in the case studies. All of the case studies are operated for a 100-SM based MMC.

Case Study-1: The optimal solution step size in the simulation for the PS-PWM and PD-PWM is selected by considering the duration of the simulation and the accuracies of the output voltage and THD. The duration of the simulation with respect to the solution step is plotted in Fig. 3. All of the results are given in Table II and Table III. For the PS-PWM, the generated voltage in RMS is almost unaffected. However,

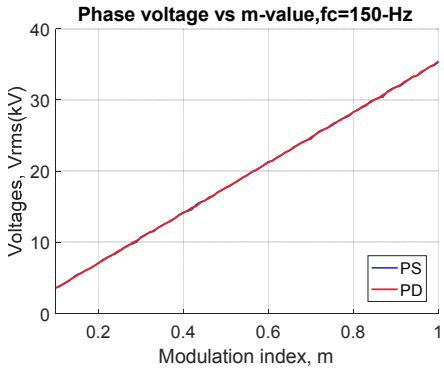


Fig. 4. Generated output phase voltage with respect to the PS-PWM and PD-PWM by varying the m-value.

the result of the THD is affected a lot by altering the solution step. The duration of the simulation is very long when the solution step is 1-micro-second for the PS-PWM. On the other hand, the output generated voltage is increase 0.4% by decreasing solution step from 20-us to 1-us for the PD-PWM. There is no remarkable effect on the THD of the phase voltage when changing solution step except 20-us for the PD-PWM. The changing of the duration is not proportional to the solution step in the PD-PWM. Due to the above reasons, the optimal solution step of the simulation is found to be 2-us.

Case Study-2: The DC voltage utilization factor by varying the m-value for the PS-PWM is classed with the PD-PWM at phase out. The m-value is increased by a 1% step from 0.1 to 1, and the phase voltage of the MMC is observed with a 150-Hz carrier frequency via applying both modulation methods in Fig. 4.

For both of the modulation techniques, the voltages are increased linearly by increasing the m-value. There is no remarkable difference between the two modulation methods in terms of the DC voltage utilization factor. This property may be advantageous for the closed loop controlling of both modulation techniques. The lowest value of the carrier frequency fc=150-Hz even for three-phase systems gives good results in terms of the DC voltage utilization. A low carrier frequency means lower switching losses. Therefore, it would be wise to choose a lower carrier frequency value in terms of a high inverter efficiency. The phase voltage of the MMC for the PS-PWM is given in Fig. 5 and that of the PD-PWM is plotted in Fig. 6. Due to the high number of SMs, the output looks like sinusoidal for both techniques.

Case Study-3: The harmonic content of the phase voltage by applying the PS-PWM and PD-PWM are investigated. Measured THD from the converter phase voltage was obtained by changing the m-value from 0.1 to 1 increased by a 1% step as shown in Fig. 7(a). In the PS-PWM, the THD-m-value curve is lower than the PD-PWM in the obtained interval of the m-value. Additionally, the THD is very low when the m-value is greater than 0.3. The THD of the PS-PWM is nearly 10 times better than the PD-PWM by considering all

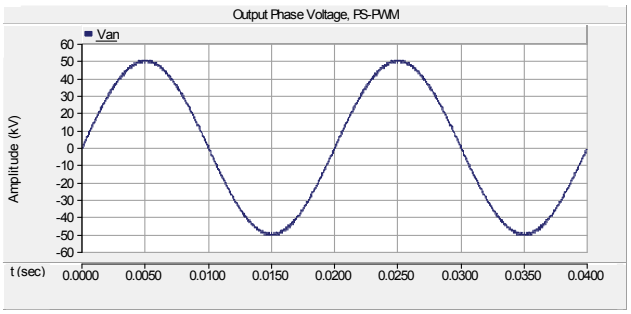


Fig. 5. Generated phase output voltage for the PS-PWM.

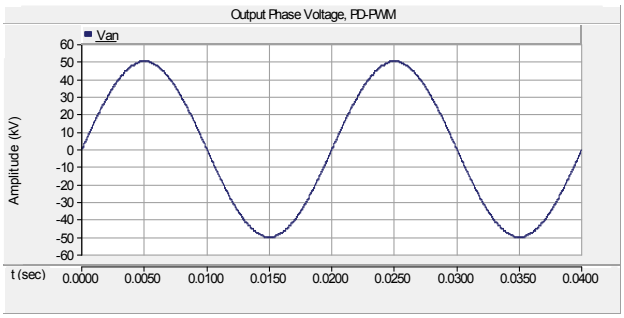
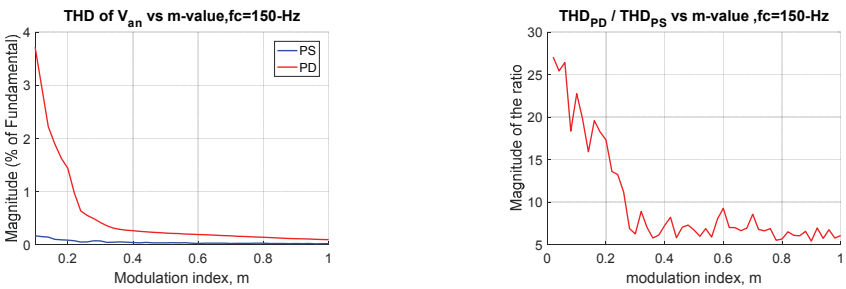
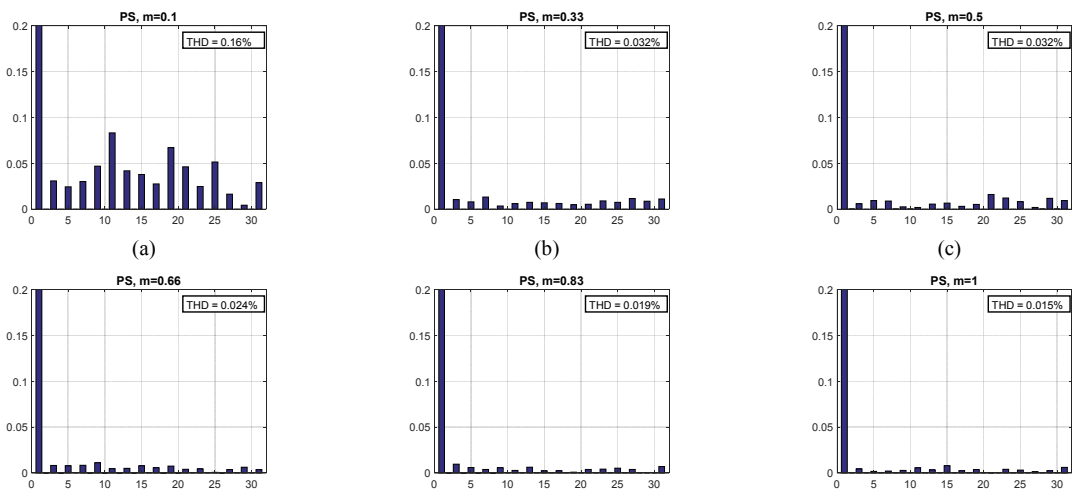


Fig. 6. Generated phase output voltage for the PD-PWM.



(a) (b)

Fig. 7. THD graphs by changing the m-values. (a) THD of the output phase voltage with respect to the PS-PWM and PD-PWM. (b) Ratio of the THD values of the PD-PWM and PS-PWM.



(a) (b) (c)

(d) (e) (f)

Fig. 8. THD and harmonic order of the output phase voltage for the PS-PWM with respect to different m-values. (a) m=0,1. (b) m=0,33. (c) m=0,5. (d) m=0,66. (e) m=0,83. (f) m=1.

of the m-values as shown in Fig. 7(b). The minimum ratio of the THD of the PD-PWM and PS-PWM is found to be 5.399. The mean value of the ratio for an m-value greater than 0.3 is 6.56. The first 31-harmonics orders and the numerical values of the THD are examined for six m-values by considering the modulation methods. The PS-PWM results are shown in Fig. 8 and those for the PD-PWM are shown in Fig. 9. There is no dominant harmonic order for both types of modulation techniques. For a low value of the m-value, the harmonics order and THD are higher for both of the modulation techniques. However, they are still less than the 3% individual and 5% THD limits stated in IEEE standard 519-2014 for the phase to neutral voltage that is between 1-kV and 69-kV [40]. The PS-PWM is better than PD-PWM in terms of operation by considering the power quality and grid efficiency. Due to their low harmonic contents, a passive filter is not needed for both modulation methods in the power circuit of the MMC. Therefore, the high passive filter cost is saved when it is utilized in medium and high voltage applications.

Case Study 4: The power performance of the MMC by varying the load current under a resistive load is considered for the PS-PWM and PD-PWM. The MMC with 100-SM

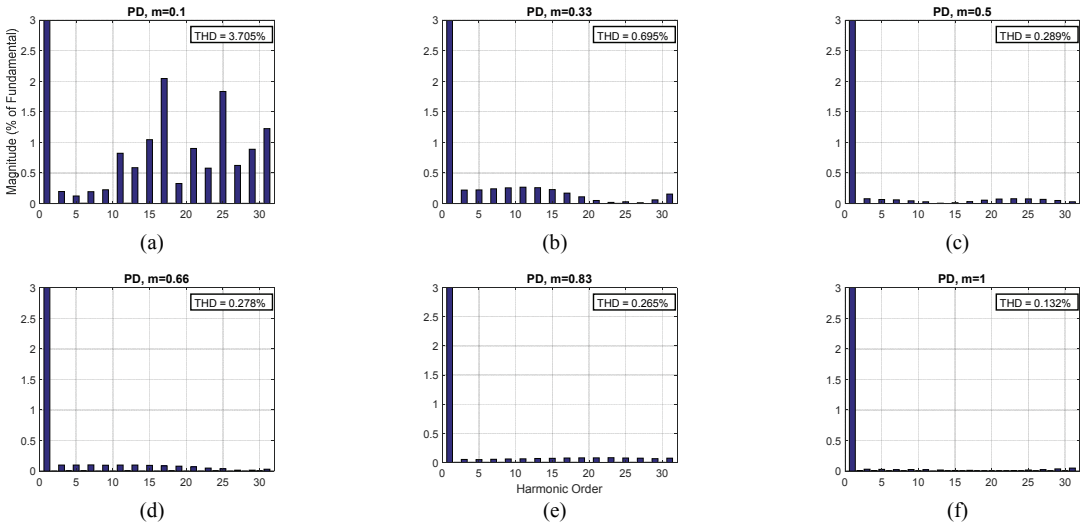


Fig. 9. THD and harmonic order of the output phase voltage for the PD-PWM with respect to different m-values. (a) m=0,1. (b) m=0,33. (c) m=0,5. (d) m=0,66. (e) m=0,83. (f) m=1.

TABLE IV
NUMERICAL RESULTS FOR THE PS-PWM BY VARYING THE LOAD CURRENT FOR AN MMC WITH A 100-SM BASED ARM

Irms (A)	Vrms (kV)	S_L (kW)	C_L (kW)	Pout (MW)	η (pu)	THD (%)
119.4	35.235	7.34	27.55	10.881	0.9968	0.0157
298.5	35.179	13.03	76.60	27.193	0.9967	0.0229
476.9	35.140	18.51	134.84	43.438	0.9964	0.0212
654.7	35.092	23.72	202.39	59.624	0.9962	0.0205

TABLE V
NUMERICAL RESULTS FOR THE PD-PWM BY VARYING THE LOAD CURRENT FOR AN MMC WITH A 100-SM BASED ARM

Irms (A)	Vrms (kV)	S_L (kW)	C_L (kW)	Pout (MW)	η (pu)	THD (%)
119.5	35.262	2.245	29.14	10.904	0.9971	0.1682
298.4	35.211	3.805	78.32	27.213	0.9969	0.1654
476.7	35.162	5.302	137.09	43.470	0.9967	0.1634
654.6	35.111	6.747	205.04	59.668	0.9964	0.1592

based arm is operated under 4-different load conditions with the optimized AI due to high simulation durations. The results are given in Table IV for the PS-PWM and in Table V for the PD-PWM.

When the sinusoidal waveform has 100-kV (maximum +50, minimum -50) amplitude, the rms value of the sine is 35.353-kV. For an inverter, if the m-value is 1, the rms value of the maximum output voltage can be 35.353-kV. For the PS-PWM, the DC voltage utilization factor of the MMC is 35.092-kV/35.353-kV=99.26% at full-load. In addition, the DC voltage utilization factor for the PD-PWM is 35.111-kV/35.353-kV=99.88%. The DC voltage utilization factor of the PD-PWM is better than that of the PS-PWM under full-load for the MMC. The switching loss of the PS-PWM is higher than that of the PD-PWM. However, the conduction loss of the PS-PWM is better than that of the PD-PWM under all conditions. The efficiencies of the MMC are at same level for both modulation techniques. In addition, the minimum efficiencies of the inverter are 99.62% and 99.64% for the PS-PWM and PD-PWM with the optimal AI. In all of the case studies, a purely resistive load is considered. Thus, the THD of the current and voltage are same. The THD of the voltage and current waveforms are 0.16% for the PD-PWM and 0.02% for the PS-PWM. These THD values are lower than the IEEE standard and the MMC does not need passive filters.

VI. EXPERIMENTAL RESULTS

A single phase MMC with a 6-SM based arm is constructed in a simulation environment and an experimental setup is designed, constructed and operated to validate the proposed method for the optimal selection of AI. As shown in Fig. 10, the experimental setup is composed of an input DC source, power supply units for the boards, a microcontroller, a FPGA control board, isolated voltage measurement boards, isolation - MOSFET driver - half bridge constructed SM switches boards, a SM capacitor, AIs, a variable resistive load and measurement devices.

A list of the numbered devices in Fig. 10 is given below.

1: Tektronix TPS 2024
2: +5 V power supply
3: Ardunio Mega
4: Xilinx Nexys 3
5: HCPL7800
6: 6N137 - IR2101 - IRFZ44N
7: 4700uF, 100V capacitor
8: Various valued AIs
9: Current probe of the TPS 2024 oscilloscope
10: Crompton analog wattmeter - Lutron DW-6163 wattmeter
11: Siemens rheostat as a load, 25Ω is used

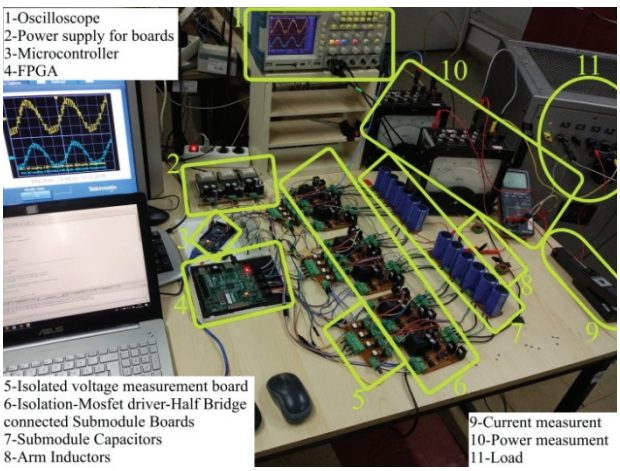


Fig. 10. MMC experimental setup with a 6-SM based arm.

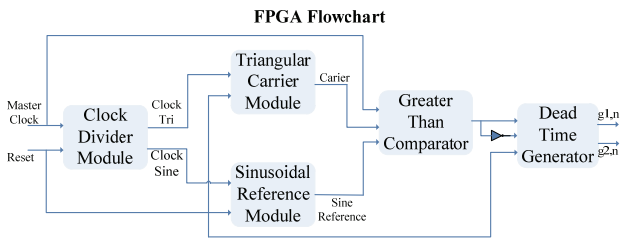


Fig. 11. FPGA flowchart for each SM of the MMC.

An external 0-400V DC power supply is used as an input DC source for the MMC. The FPGA is programmed for a half-bridge constructed 6-SM based arm. A flowchart of the FPGA is given in Fig. 11 for each of the SMs.

The operation of the FPGA flowchart for a CHB-MLI is explained in detail in [41]. The program is adjusted for a 6-SM based MMC. The clock divider module can adjust the frequency of the output clock using a dividing operation. The master clock is 100-MHz, the clock tri is nearly 150-Hz and the clock sine is 50-Hz. The dead time is 200ns for both modulation techniques. In the PD-PWM, the carrier signals are swapped with a frequency of 25-Hz in the FPGA to accomplish self-balancing of the capacitor voltages, which is given in [39]. The swapping operation is programmed in the Triangular Carrier Module of the FPGA flowchart.

The method for obtaining the measured values of the experimental studies are explained here. The coil inductance and resistance values are metered by using an LCR meter before connecting to an MMC system. The RMS values of the voltages/currents at the input/output sides are taken by utilizing a digital multimeter. The input/output active powers are measured by using analog and digital wattmeters to verify their results. Output voltage/current waveforms are captured using a digital oscilloscope and stored to a computer via the computer program of the oscilloscope. The THD of voltage/ current waveforms are computed by considering the first 31-harmonic orders.

10-different AIs are designed for the experimental setup.

TABLE VI
DESIGNED AIS FOR THE EXPERIMENT

Case No	Larm (H)	Rarm (Ω)	Quality factor	Core Type
1	0.011	0.089	0.038	Ferrite1
2	0.099	0.068	0.457	Ferrite2
3	0.115	0.174	0.207	Ferrite3
4	0.434	0.08	1.703	Ferrite2
5	1.065	0.092	3.634	Ferrite2
6	2.604	0.129	6.338	Ferrite2
7	4.889	4.47	0.343	Air
8	5.213	0.253	6.469	Ferrite2
9	10.042	0.353	8.932	Ferrite2
10	20.043	7.97	0.789	Air

TABLE VII
EXPERIMENTAL RESULTS FOR A 6-SM BASED MMC, PS-PWM

Case No	Pin (W)	Vout (V)	Pout (W)	η (pu)	THD Vout (%)	THD Iout (%)
1	87.0	38.4	57.6	0.662	16.52	16.30
2	86.1	38.2	56.9	0.661	17.12	16.60
3	74.8	38.3	57.0	0.762	16.72	15.77
4	85.2	38.4	57.6	0.676	16.59	16.00
5	83.4	38.3	57.0	0.684	16.96	16.39
6	82.1	38.4	57.6	0.701	16.42	15.98
7	55.4	34.2	45.4	**0.821**	15.05	14.73
8	71.9	38.9	58.7	0.816	16.53	15.96
9	78.8	38.3	57.0	0.724	16.26	15.56
10	50.2	30.8	37.2	0.742	**10.59**	**10.27**

They vary from 0,01mH to 20mH by using three different ferrite core types and air core types to analyze the effects of the core type and changing the values of the AIs. The measured values, quality factor and core types of the inductors are given in Table VI.

Various case studies are performed on the designed experimental setup to confirm the simulation studies and their results. Two case studies are performed on the experimental setup and in the simulation program to compare the PS-PWM and PD-PWM. In each case study, there are ten cases by changing the AI. This is done to understand the effects of the value and type of AI on the performance parameters of the MMC. For both case studies, there are two series connected 60-V DC sources at the input of the MMC and series connected 25-Ω resistive loads via a 0.5-mH inductor load at output sides of the designed MMC. First, all of the capacitors are charged and their voltages are balanced. Then the data are captured by using measurement devices. In the case studies, comparable simulation results with the same initial conditions are given for the 6-SM based MMC.

Case Study 1: The experimental setup is operated ten times with the PS-PWM technique for various AI values. The effects of the type and changing value of the AI are analyzed by measuring input power, output voltage, output power, efficiency and THD of the voltage/current of the 6-SM based MMC. The results are given in Table VII.

TABLE VIII
SIMULATION RESULTS FOR A 6-SM BASED MMC, PS-PWM

Case No	Pin (W)	Vout (V)	Pout (W)	η (pu)	THD Vout (%)	THD Iout (%)
1	90.7	40.43	58.26	0.642	16.01	15.93
2	91.8	40.43	58.22	0.634	16.02	15.94
3	90.4	40.29	57.85	0.640	16.03	15.94
4	89.3	40.32	58.04	0.650	16.00	15.92
5	86.9	39.79	56.66	0.652	15.99	15.90
6	85.5	41.18	61.11	0.715	14.98	14.91
7	57.5	35.96	46.82	**0.814**	14.07	14.00
8	75.0	39.75	56.87	0.758	15.55	15.49
9	82.9	39.17	55.96	0.675	14.75	14.71
10	52.4	32.62	39.10	0.746	**8.34**	**8.31**

TABLE IX
EXPERIMENTAL RESULTS FOR A 6-SM BASED MMC, PD-PWM

Case No	Pin (W)	Vout (V)	Pout (W)	η (pu)	THD Vout (%)	THD Iout (%)
1	107.3	38.7	58.82	0.548	9.36	10.38
2	108.2	38.8	58.98	0.545	8.72	8.63
3	94.5	38.9	59.13	0.625	9.85	9.84
4	103.8	38.9	59.13	0.569	8.31	8.49
5	102.3	38.8	58.98	0.576	9.45	9.45
6	100.5	38.7	58.82	0.585	9.13	8.99
7	59.1	34.9	47.46	**0.803**	8.30	8.39
8	96.9	39.0	59.67	0.615	9.89	9.44
9	95.2	38.9	59.52	0.625	8.50	8.45
10	52.5	30.9	38.01	0.723	**5.95**	**6.14**

A simulation is run and the variables are obtained for the PS-PWM for the same conditions as the experimental system. The results are given in Table VIII.

The simulation setup and its results are verified by experimental results. For the PS-PWM, the maximum efficiency occurs for the air cored AI in the 7th case for both the experimental and simulation studies. The THD of the 6-SM based MMC is about 15% at a 150-Hz carrier frequency. The minimum THD is calculated to be about 8% for both studies in the 10th case. However, the DC voltage utilization is low for this case. The ferrite cored AI, 5.2-mH is better in terms of efficiency in the 8th case. The THD and DC voltage utilization factor are acceptable when compared to others for the PS-PWM with a 5.2-mH AI.

Case Study 2: Experimental results with the PD-PWM by changing the AI to detect the performance parameters of the MMC are given in Table IX. For this test, carrier swapping is applied to the algorithm to achieve equal time usage of the gate signal of the SM. The SM carrier signals are shifted sequentially one SM gate to another with a 25-Hz swapping.

For the PD-PWM experimental results, the air cored AI shows good performance in terms of efficiency and THD. However, the output generated voltages are low when compared to ferrite ones. For the ferrite cored AI, the input powers increase a lot while supplying the same output powers.

TABLE X
SIMULATION RESULTS FOR A 6-SM BASED MMC, PD-PWM

Case No	Pin (W)	Vout (V)	Pout (W)	η (pu)	THD Vout (%)	THD Iout (%)
1	112.3	39.72	59.87	0.533	11.51	11.16
2	110.9	39.97	60.49	0.545	12.08	11.76
3	96.9	39.64	59.65	0.615	11.26	10.93
4	107.2	40.10	61.12	0.570	10.70	10.44
5	106.8	40.03	60.94	0.570	10.68	10.48
6	103.6	40.26	58.78	0.567	10.36	10.23
7	60.4	34.86	46.35	**0.767**	8.76	8.72
8	96.5	39.05	58.25	0.603	8.31	8.24
9	96.9	39.92	61.05	0.630	6.28	6.25
10	54.3	32.73	41.12	0.757	**4.70**	**4.68**

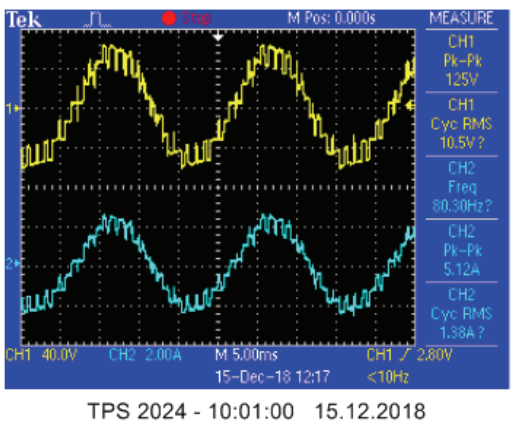


Fig. 12. Output phase voltage/current for the PS-PWM.

The simulation and experimental results obtained for the PD-PWM meet each other when considering the dc voltage utilization, efficiency and THD values.

The MMC is operated with a 5.2-mH ferrite cored AI which is the 8th case in Table VII. The magnitude of the input DC voltage is 120-V. For the PS-PWM technique, output voltage and current waveforms are given in Fig. 12. The output voltage waveform (yellow) is captured by using a voltage probe at the first channel of the oscilloscope, and the output current waveform (blue) is captured by a current probe at the second channel of the oscilloscope, which is the 9th case in Fig. 10. The screen and waveform data of the Tektronix TPS2024 oscilloscope is transferred to the computer by the Open Choice Desktop software program. Measured and calculated results are given for the 8th case in Table VII.

The MMC is operated for the PD-PWM technique via the same 5.2-mH ferrite cored AI. The performance of the experimental results are given for the 8th case in Table IX. The captured output voltage (yellow) and current (blue) waveforms are given in Fig. 13.

As can be seen in Fig. 12 and Fig. 13, 7-level output phase voltages are obtained as expected for both modulation techniques. For the PS-PWM, the number of switchings is

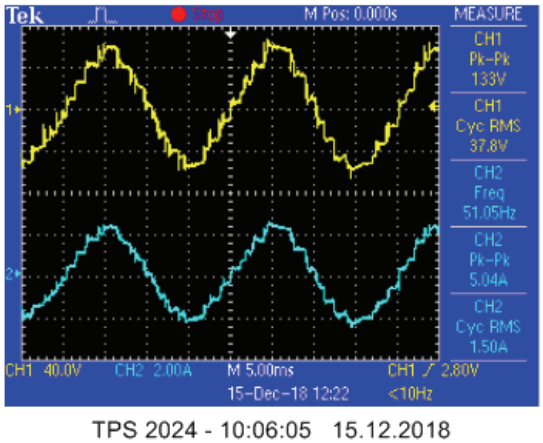


Fig. 13. Output phase voltage/current for the PD-PWM.

greater than the PD-PWM. As can be inferred from the THD columns of Table VII and Table IX, a more sinusoidal waveform is obtained when the PD-PWM is used rather than the PS-PWM.

For both modulation techniques, the obtained experimental and simulation results demonstrate that changes in the AI affect the DC voltage utilization, efficiency and THD of the output voltage/current. Air cored AIs have a high resistance and they filter output voltage. Therefore, their efficiency and THD performances are higher than those of the ferrite cored for this voltage level. However, for middle/high voltage levels, an increase in the air-cored inductor losses and a decrease in the efficiency are expected due to the high internal resistance of the AI.

The carrier frequency must be selected to be higher than 150-Hz to satisfy IEEE THD standards for a MMC with a 6-SM based arm at this voltage level. The efficiency of the inverter is also low at this operation voltage which is a 120-V DC voltage.

VII. Conclusions

AI selection has vital importance for designing MMCs. If it is selected only to limit fault current or to minimize circulation current as in previous studies, desired efficiency and THD performances for the MMC cannot be achieved. After the inverter power and SM capacitor are decided, the AI should be optimized in an acceptable interval by considering the low switching and conduction losses of the semiconductor, the high inverter output power, the high efficiency of the inverter and the low THD of the output voltage. The PS-PWM and PD-PWM are compared by considering the DC voltage utilization factor, the harmonic content and the efficiency with the optimal value of the AI. The DC voltage utilization factor increases linearly when the m-value increases for a 100-SM based MMC for both techniques. This feature is superior for both methods in closed loop control operation. The THD is very low when the m-value is equal to a value such as 0.02% for the PS-PWM and 0.16% for the PD-PWM for the full load condition. The PS-PWM is better than the PD-PWM in terms of THD and harmonic order and the results of both modulation methods satisfy the harmonic limits defined in IEEE standard 519- 2014. Additionally, the PS-PWM is less than 10 times the PD-PWM when considered all of the regions of the m-value. In addition, there is no dominant harmonic order for both of the methods. Under the worst case, the efficiencies of a 100-SM based MMC are 99.62% and 99.64% for the PS- PWM and PD-PWM, respectively. Increasing the number of SMs proportionally affects THD. However, it does not influence the efficiency performance very much. The obtained simulation results are validated with an experimental prototype of a 6-SM based MMC.

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Ali Osman Arslan received his B.S. and M.S. degrees from the Department of Electrical and Electronics Engineering of Gaziantep University, Gaziantep, Turkey, in 2009 and 2012, respectively. From September 2010 to May 2011, he was a Research Assistant at Kilis 7 Aralık University, Kilis, Turkey. Since May 2011, he has been working as a Research Assistant in the Department of Electrical and Electronics Engineering, Gaziantep University. His current research interests include power electronics, multilevel converters, modular multilevel converters and the control of electrical railway systems.

Mehmet Kurtoğlu received his B.S. degree from the Department of Electrical and Electronics Engineering, Çukurova University, Adana, Turkey, in 2014; and his M.S. degree from the Department of Electrical and Electronics Engineering, Gaziantep University, Gaziantep, Turkey, in 2017, where he is presently working towards Ph.D. degree in Department of Electrical and Electronics Engineering and working as a Research Assistant. His current research interests include multilevel converters and their modulation techniques, and the energy conversion systems and applications of power electronics to power systems.

Fatih Eroğlu was born in Kütahya, Turkey. He received his B.S. degree from the Department of Electrical and Electronics Engineering, Ihsan Dogramaci - Bilkent University, Ankara, Turkey, in 2015; and his M.S. degree from the Department of Electrical and Electronics Engineering, Gaziantep University, Gaziantep, Turkey, in 2018, where he is presently working as a Research Assistant. His current research interests include power electronic systems, and the modulation and control of power converters for renewable energy systems.

Ahmet Mete Vural received his Ph.D. degree in Electrical and Electronics Engineering from Çukurova University, Adana, Turkey, in 2012. He was a Visitor Scholar at Strathclyde University, Glasgow, SCT, UK, in 20s00. He worked as Research Assistant at Gaziantep University, Gaziantep, Turkey, from 1999 to 2004; and at the University of Wuppertal, Wuppertal, Germany, from 2004 to 2007. He is presently working as a full-time Associate Professor in the Department of Electrical and Electronics Engineering, Gaziantep University. His current research interests include utility applications of power electronics, multilevel converters, power quality, micro/smart grids, renewable energy, energy storage, and flexible AC transmission systems (FACTS).