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ZVT Series Capacitor Interleaved Buck Converter with High Step-Down Conversion Ratio

Zhangyong Chen†, Yong Chen*, Wei Jiang*, and Tiesheng Yan**

†,*School of Automation Engineering, Institute for Electric Vehicle Driving System and Safety Technology, University of Electronic Science and Technology of China, Chengdu, China
**School of Electrical Engineering and Electronic Information, Xihua University, Chengdu, China

Abstract

Voltage step-down converters are very popular in distributed power systems, voltage regular modules, electric vehicles, etc. However, a high step-down voltage ratio is required in many applications to prevent the traditional buck converter from operating at extreme duty cycles. In this paper, a series capacitor interleaved buck converter with a soft switching technique is proposed. The DC voltage ratio of the proposed converter is half that of the traditional buck converter and the voltage stress across the one main switch and the diodes is reduced. Moreover, by paralleling the series connected auxiliary switch and the auxiliary inductor with the main inductor, zero voltage transition (ZVT) of the main switches can be obtained without increasing the voltage or current stress of the main power switches. In addition, zero current turned-on and zero current switching (ZCS) of the auxiliary switches can be achieved. Furthermore, owing to the presence of the auxiliary inductor, the turned-off rate of the output diodes can be limited and the reverse-recovery switching losses of the diodes can be reduced. Thus, the efficiency of the proposed converter can be improved. The DC voltage gain ratio, soft switching conditions and a design guideline for the critical parameters are given in this paper. A loss analysis of the proposed converter is shown to demonstrate its advantages over traditional converter topologies. Finally, experimental results obtained from a 100V/10V prototype are presented to verify the analysis of the proposed converter.

Key words: Loss analysis, Series capacitor buck converter, Zero current switching, Zero voltage transition

I. INTRODUCTION

The step-down power-conversion technique is widely used in the power sources for microprocessors, automotive applications, LED drivers, solar-power regulators and so on. In the field of power conversion, high efficiency and high power density of power converters are the ultimate goal of researchers and engineers. However, owing to the high voltage stress and current stress of the components in power conversion systems, there are large conduction losses of the components, switching losses of the power switches, reverse-recovery switching losses of the power diodes and so on. These losses limit the efficiency improvements of power converters. In order to improve the power conversion efficiency of DC-DC step-down converters, passive snubbers were presented in [1], [2] to achieve zero-current turn-on and zero-voltage turn-off of switches. As a result, the switching losses of the power switches can be reduced. In addition, the coupled-inductor technique is introduced to the output-side of a step-down converter to relieve the reverse-recovery problems of output diodes in [3]-[5]. However, such a technique is achieved at the expense of increased voltage or current stress on the main switches. Thus, the improved performance of this converter is limited. In [6], a twin-buck converter with zero voltage transition was proposed. However, the soft switching ranges of this converter are narrowed which is determined by the restored inductor energy. By introducing a coupled-inductor and auxiliary switch, efficient ZVS operation with load variations of the converter was obtained in [7]. However, the circuit complexity of the proposed converter is increased. When operating in the critical conduction mode, soft switching

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†Corresponding Author: zhang_yong_ch@126.com
Tel: +86-028-66360662, Univ. Electronic Sci. & Tech. China (UESTC)
*Sch. Autom. Eng., Inst. Electr. Vehicle Driving Syst. Safety Technol., Univ. Electron. Sci. Technol. China, China
**Sch. Electr. Eng. Electron. Inform., Xihua Univ., China

for the main switches and diode in the buck converter is achieved. In addition, Gallium nitride (GaN) power switching devices [8] can be used to further improve the efficiency of the buck converter. Unfortunately, a large current ripple increases the conduction losses of the power switches and diode [9]. Thus, it is only available for low power applications. In [10], [11], the switch voltage stress of a converter was reduced by utilizing the switch-capacitor technique. Thus, a low switching loss and improved step-down conversion ratio are achieved to improve the character of this converter. A soft switching cell [12] and an active clamp circuit [13] can be used in the buck converters in PV panel and wind turbines applications. The zero voltage transition technique was first presented by Guichao Hua et al. [14] in order to achieve zero voltage switching of power switches without increasing the voltage stress and current stress in PWM converters. When this technique is applied in DC/DC buck converters and interleave buck converters [15]-[20], their efficiency can be increased.

In many applications, a high step-down conversion ratio is required to prevent the converter from operating at an extreme duty cycle. Many techniques have been presented to solve this problem. Four-phase interleaved buck converters [21], [22] and a two phase interleave buck converter [23] were proposed to achieve a high step-down conversion ratio and low switch voltage stress. In addition, automatic current sharing is also achieved without adding any active auxiliary components or using transformers. A series capacitor buck converter was proposed in [24] to reduce switching losses and inductor current ripple. Only one capacitor is added to the traditional interleave buck converter. Thus, the efficiency of interleave buck converters can be improved with a simple circuit topology. In order to further extended the duty cycle, the coupled-inductor technique was utilized in a converter in [25] by regulating the turns-ratio of the couple-inductor and the duty cycle of the main switches. In [26], two series capacitors have been introduced to an interleaved buck converter to achieve a very high step-down conversion ratio. By combining a quadratic buck converter and the soft switching technique, a high step-down ratio and zero voltage switching for the main switches can be achieved. As a result, this converter has been successfully applied to high step-down ratio applications [27], [28]. However, in terms of the cascade of the power conversion in quadratic buck converters, the efficiency is very low despite utilizing the soft switching technique. A three-level buck converter is presented to reduce the switch voltage stress of converters and a zero current transition technique is utilized to reduce switching losses. Thus, a high efficiency can be obtained. However, floating four switches are used in the converter proposed in [29]. However, the control of this converter is very complex. A zero voltage transition technique is utilized in the fourth-order buck converter [30], and high step-down and ZVS of the main switches can be achieved. However, this buck converter topology is also complex.

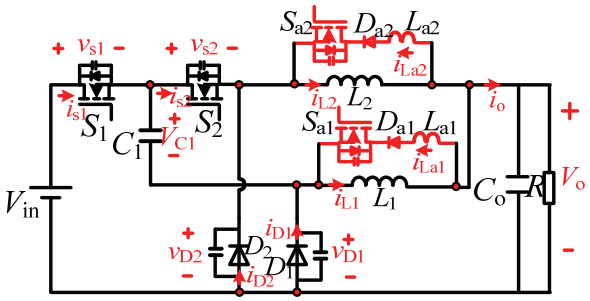


Fig. 1. Proposed zero voltage transition interleaved buck converter topology.

In order to achieve a high efficiency and a high step-down conversion ratio, a zero voltage transition technique is introduced to the series capacitor interleaved buck converter in this paper. The proposed converter, where the ZCS-ZVS PWM circuit cell [31], [32] is composed of a series connection of auxiliary switches and an inductor, is utilized. Zero voltage transition of the main power switches can be achieved and zero current switching of the auxiliary switches can be obtained in a wide operating range. Due to the small operating time of the auxiliary circuit, the additional conduction losses caused by the auxiliary circuit are very small. The proposed technique does not increase the voltage stress and current stress of the main switches and diodes. It behaves as a PWM-type character.

The circuit configuration and operation principle of the proposed converter are presented in Section II. Relevant analysis results, including the voltage transfer gain, soft switching condition, selection of the auxiliary circuit parameters and implementation of the driver circuit, are given in Section III. A loss analysis of the proposed converter is shown in Section IV, and the performance of the proposed converter is confirmed by the experimental results obtained with a 100V/10V prototype in Section V. Topology variations of the proposed converter are illustrated in Section VI, and some conclusions are given in Section VII.

II. Proposed ZVT Series Capacitor Interleaved Buck Converter

A. Circuit Configuration

The proposed zero voltage transition (ZVT) series capacitor based interleaved buck converter topology is shown in Fig. 1. The series capacitor based interleaved buck converter is composed of the switches S_1 and S_2, the diodes D_1 and D_2, the output inductors L_1 and L_2, and the series capacitor C_1, which was proposed and analyzed by Il-Oun Lee, et al. [24]. The analyzed results show that series capacitor interleaved buck converters have the merits of extended duty cycle, reduced switching losses, decreased inductor current ripples, and automatic current balancing, when compared with the

interleaved buck converter. Therefore, the series capacitor interleaved buck converter has been as potential candidate in applications where non-isolation, a high step-down conversion ratio and a high output current with low ripple are required. However, the switching losses and the capacitive discharging losses of the power switches in series capacitor buck converters are the dominant losses as derived from a loss analysis of this converter. These problems become worse with an increase in the switching frequency. Thus, in order to further improve the efficiency of this converter, the switching losses and capacitive discharging losses should be reduced or eliminated. The soft switching technique provides a solution for these problems.

In this paper, a zero voltage transition technique is proposed for use in a series capacitor buck converter without increasing the component voltage or current stress on the main power switches or diodes. In addition, zero voltage switching (ZVS) of the power switches can be achieved in the whole operating range, and the reverse recovery losses of the output diodes can be reduced due to the limited rate of the turned-off di/dt slew rate. Moreover, the zero current switching (ZCS) and zero current turn-on for the auxiliary switch can be achieved to reduce the switching losses of the auxiliary switch. In Fig. 1, the auxiliary circuit is composed of a series connection of the switch S_{a1}, the diode D_{a1} and the inductor L_{a1}, and a series connection of the switch S_{a2}, the diode D_{a2} and inductor L_{a2}, which are also paralleled with the output inductors L_1 and L_2, respectively. The auxiliary switches S_{a1} and S_{a2} are turned-on before the arrival of the gate pulse of the main switches S_1 and S_2 and they provide negative current through the switches S_1 and S_2. Zero voltage switching for the switches S_1 and S_2 can be achieved.

B. Operation Principle

In order to simplify the analysis of the proposed converter, the following assumptions are made. 1) All of the semiconductor devices in the proposed converter, which include the power switch S_1 and S_2, and the auxiliary switches S_{a1} and S_{a2}, are ideal except for the anti-parallel diodes and output capacitors. The output diodes D_1 and D_2, and the auxiliary diodes D_{a1} and D_{a2} are ideal except for the stray capacitors. 2) The output capacitor C_o and the series capacitor C_1 are very large so that the voltages V_o and V_{C1} can be considered as constants in a switching cycle. 3) The auxiliary switches S_{a1} and S_{a2} are turned-on before the main power switches S_1 and S_2, respectively. 4) The converter is operated in the steady state.

Fig. 2 shows key waveforms of the proposed converter, where v_{gs} is the gate pulse of the power switches S_1,S_2,S_{a1},S_{a2}, and the gate pulse of the switches S_2 and S_{a2} have a 180^0 shift delay to the switches S_1 and S_{a1}, respectively. In addition, the auxiliary switches S_{a1} and S_{a2} are turned-on before the main power switches S_1 and S_2. i_{La1} and i_{La2} are the currents through the auxiliary inductors L_{a1} and L_{a2}; i_{s1} and i_{s2} are the currents through the switches S_1 and S_2; and i_{D1} and i_{D2} are the currents through the output diodes D_1 and D_2. In the proposed converter, there exist ten operation modes in a switching cycle, and the equivalent circuits of proposed converter for each operation mode are shown in Fig. 3.

Mode 1 **[$t_0 \sim t_1$]**: At t=t_0, the gate pulse for the power switch S_{a1} is turned to on, the auxiliary switch S_{a1} is turned-on, and the switches S_1, S_2 and S_{a2} are turned-off. The output inductor current is freewheeling through the output diodes D_1 and D_2. Because of the turned-on auxiliary switch S_{a1}, the voltage across the auxiliary inductor is equal to the output voltage. In addition, the current i_{La1} is linearly increased and current i_{D1} is linearly decreased. When the current i_{D1} is decayed to zero, the diode D_1 is turned-off and this mode is ended. In this interval, the current i_{La1} can be expressed as:

$$i_{La1}(t) = \frac{V_o}{L_{a1}}(t - t_0) \tag{1}$$

At the end of this interval, the current i_{La1} is equal to $I_o/2 - \Delta i_{L1}/2$, since the diode D_1 is decayed to zero, where I_o is output current, V_o is the output voltage, and Δi_{L1} is the peak-peak current ripple of the inductor L_1. Thus, the interval time can be obtained as:

$$\Delta T_{10} = \frac{I_o / 2 - \Delta i_{L1} / 2}{V_o / L_{a1}} \tag{2}$$

Mode 2 **[$t_1 \sim t_2$]**: At t=t_1, the current i_{D1} is decayed to zero and the diode D_1 is turned-off. In this mode, due to the continued turn-on of the switch S_{a1}, the stray capacitor of the switch S_1 and the diode D_1 are resonant with the auxiliary inductor L_{a1}. In addition, the equivalent resonant capacitor is equal to the parallel stray capacitor of the switches S_1 and S_2 and the diode D_1. After half of a resonant period, the current i_{La1} is returned to $I_o/2 - \Delta i_{L1}/2$, and equal to the current i_{L1}. At the end this interval, the voltage across the diode D_1 rises up to the difference of the input voltage and the capacitor voltage V_{C1}. In addition, the voltage across the switch S_1 is decayed to zero. Then the gate pulse of the switch S_1 is arrives. In addition, the zero voltage switching of the power switch S_1 can be achieved and the switching losses can be eliminated. Based on the analysis, the circuit equation can be obtained as:

$$\begin{cases} -C_{eq}\dfrac{dv_{S1}(t)}{dt} = i_{La1}(t) - (I_o / 2 - \Delta i_{L1} / 2) \\ L_{a1}\dfrac{di_{La1}(t)}{dt} = V_o - V_{in} + V_{C1} + v_{s1}(t) \end{cases} \tag{3}$$

i_{La1} and v_{S1} can be solved according to equation (3) with the initial condition $i_{La1}(t_0) = I_o/2 - \Delta i_{L1}/2$, $v_{S1}(t_0) = V_{in} - V_{C1}$. Therefore, the auxiliary inductor current and drain-source across the switch S_1 can be expressed as:

$$\begin{cases} i_{La1}(t) = (I_o / 2 - \Delta i_{L1} / 2) + (V_o / Z_{r1}) \cdot \sin(\omega_{r1} t) \\ v_{s1}(t) = V_{in} - V_{C1} + (\cos(\omega_{r1} t) - 1) \cdot V_o \end{cases} \tag{4}$$

Where the character impedance $Z_{r1}=\sqrt{L_{a1}/C_{eq}}$ and the resonant angular frequency $\omega_{r1}=1/\sqrt{L_{a1}C_{eq}}$. In addition, $C_{eq1}=C_{S1}+C_{S2}+C_{d1}$ and C_{s1}, C_{S2},C_{d1} are the stray capacitors of the power switches S_1 and S_2 and the diode D_1.

The time of this interval is:

$$\Delta T_{21}=\pi\sqrt{L_{a1}C_{eq1}} \tag{5}$$

Mode 3 **[$t_2 \sim t_3$]**: At $t=t_2$, the gate pulse of the switch S_1 is achieved since the voltage across the switch S_1 was decayed to zero and anti-parallel diode of the switch S_1 was conducted in the previous mode. The auxiliary switch S_{a1} continues conducting and voltage across the inductor L_{a1} is equal to the difference of the input voltage V_{C1} and the output voltage V_o. Thus, the current i_{La1} is linearly decreased. In addition, the inductor current i_{L1} is increased at the rate of $(V_{in} - V_{C1} - V_o)/L_1$, and the current i_{L2} is freewheeling with the diode D_2. In this interval, the following equations can be obtained as:

$$i_{La1}(t)=(I_o/2-\Delta i_{L1}/2)-\frac{V_{in}-V_{C1}-V_o}{L_{a1}}(t-t_2) \tag{6}$$

$$i_{L1}(t)=i_{L1}(t_2)+\frac{V_{in}-V_{C1}-V_o}{L_1}(t-t_2) \tag{7}$$

When the current i_{La1} is decreased to zero, the current through the switch S_1 is equal to the inductor current i_{L1}, and this mode ends. Thus, the time interval is:

$$\Delta T_{32}=\frac{I_o/2-\Delta i_{L1}/2}{(V_{in}-V_{C1}-V_o)/L_{a1}} \tag{8}$$

Mode 4 **[$t_3 \sim t_4$]**: At $t=t_3$, the current through the switch S_{a1} is decayed to zero, and zero current turn-off for the auxiliary switch S_{a1} can be achieved. The current i_{S1} is equal to the current i_{L1} through inductor L_1, and the current i_{L1} is still linearly increased with the rate of $(V_{in} - V_{C1} - V_o)/L_1$. The diode D_2 is provided as the following path for the inductor current i_{L2}.

Mode 5 **[$t_4 \sim t_5$]**: At $t=t_4$, the gate pulse of the switch S_1 disappears and the switch S_1 is turned-off. Then, the currents i_{L1} and i_{L2} freewheel through the diodes D_1 and D_2, and the currents i_{L1} and i_{L2} are decreased with the rates of V_o/L_1 and V_o/L_2.

Mode 6 **[$t_5 \sim t_6$]**: After half of a switching period, the gate pulse of the auxiliary switch S_{a2} is arrived at and the auxiliary switch S_{a2} is turned-on. The auxiliary current i_{La2} is increased linearly with the rate of V_o/L_{a2}. The currents i_{L1} and i_{L2} are freewheeling through the diodes D_1 and D_2. In this interval, the current i_{La2} can be expressed as:

$$i_{La2}(t)=\frac{V_o}{L_{a2}}(t-t_5) \tag{9}$$

When the current i_{La2} is increased and becomes equal to the current i_{L2}, zero current turn-off for the diode D_2 is realized. At the end of this mode, the current i_{La2} is equal to $I_o/2 - \Delta i_{L2}/2$, where Δi_{L2} is the current ripple of the inductor L_2. Thus, the interval time can be obtained as:

$$\Delta T_{65}=\frac{I_o/2-\Delta i_{L2}/2}{V_o/L_{a2}} \tag{10}$$

Mode 7 **[$t_6 \sim t_7$]**: At t_6, the diode D_1 is turned-off at zero current. The auxiliary switch S_{a2} is continuously turned-on, the stray capacitor of the switch S_2 and the diode D_2 is resonant with the auxiliary inductor L_{a2}, and the equivalent resonant capacitor is equal to the parallel of C_{s2} and C_{d2}. After half of a resonant period, the current i_{La2} returns to $I_o/2 - \Delta i_{L1}/2$, and is equal to the current i_{L2}. At this end of this interval, the voltage across the diode D_2 is equal to V_{C1}, and the drain-source voltage across the switch S_2 is equal to zero. Thus, the condition for the zero voltage switching of the switch S_2 is guaranteed. Based on the analysis, the circuit equation can be obtained as:

$$\begin{cases} -C_{eq}\dfrac{dv_{S2}(t)}{dt}=i_{La2}(t)-(I_o/2-\Delta i_{L2}/2) \\ L_{a2}\dfrac{di_{La2}(t)}{dt}=V_o-V_{C1}+v_{s2}(t) \end{cases} \tag{11}$$

i_{La1} and v_{S1} can be solved according to equation (11) with the initial conditions $i_{La2}(t_0)= I_o/2 - \Delta i_{L1}/2$ and $v_{S2}(t_0)= V_{C1}$. Therefore, the auxiliary inductor current and drain-source across the switch S_1 can be expressed as:

$$\begin{cases} i_{La2}(t)=(I_o/2-\Delta i_{L2}/2)+(V_o/Z_{r2})\cdot\sin(\omega_{r2}t) \\ v_{s2}(t)=V_{C1}+(\cos(\omega_{r2}t)-1)\cdot V_o \end{cases} \tag{12}$$

Where the character impedance $Z_{r2}=\sqrt{L_{a2}/C_{eq2}}$, the resonant angular frequency $\omega_{r2}=1/\sqrt{L_{a2}C_{eq2}}$ and $C_{eq2}= C_{S2}+C_{d2}$. In addition, C_{S2} and C_{d2} are the stray capacitors of the power switch S_2 and the diode D_2, respectively.

The time of this interval is:

$$\Delta T_{76}=\pi\sqrt{L_{a2}C_{eq2}} \tag{13}$$

Mode 8 **[$t_7 \sim t_8$]**: At $t=t_7$, the gate pulse of the switch S_2 is achieved. The difference of the currents i_{La2} and i_{L2} is following through the switch S_2, and the anti-parallel diode for the switch S_2 is conducted. Thus, the zero voltage switching of the switch S_2 is guaranteed. The current through the auxiliary inductor and the auxiliary switch S_{a2} is decreased at the rate of $(V_o - V_{C1})/L_{a2}$, and the current i_{S2} is increased. When the current i_{La2} is decayed to zero, the current i_{S2} is equal to the current i_{L2}, the zero current switching for the auxiliary switch is achieved and this mode ends. Moreover, the diode D_1 provides the following path for

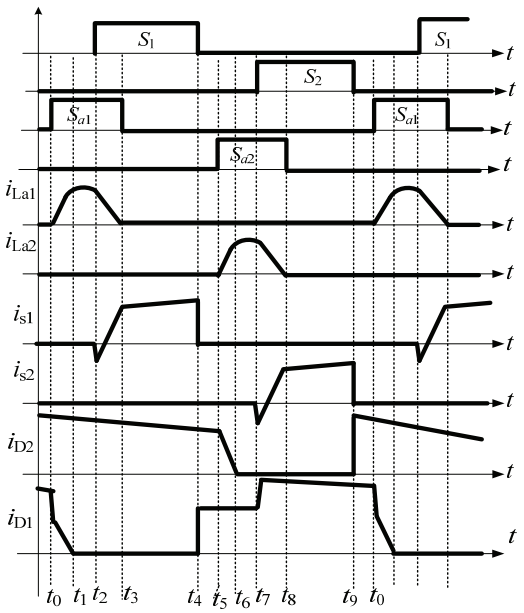


Fig. 2. Key waveforms of the proposed converter.

the output inductor L_1. In this interval, the following equations can be obtained as:

$$i_{La2}(t) = (I_o / 2 - \Delta i_{L2} / 2) - \frac{V_{C1} - V_o}{L_{a2}}(t - t_7) \quad (14)$$

$$i_{L2}(t) = i_{L2}(t_7) + \frac{V_{C1} - V_o}{L_2}(t - t_7) \quad (15)$$

When the current i_{La2} is decreased to zero, this mode ends. Thus, the time interval is:

$$\Delta T_{87} = \frac{I_o / 2 - \Delta i_{L2} / 2}{(V_{C1} - V_o) / L_{a2}} \quad (16)$$

Mode 9 **[$t_8 \sim t_9$]**: At t=t_8, the current i_{La2} is decreased to zero, and the auxiliary switch S_{a2} is turned-off at zero current. The capacitor C_1 provides the energy transfer to the load-side, and the diode D_1 provides the following path for the inductors L_1 and L_2. The current i_{L1} is decreased with the rate of V_o/L_1, and the current i_{L2} is increased with the rate of (V_{C1} - V_o)/L_2. Thus, the interleaved current is flowing through the diode D_1, and the current ripple of i_{D1} can be reduced. The following equation can be obtained as:

$$i_{L1}(t) = i_{L1}(t_8) - \frac{V_o}{L_1}(t - t_8) \quad (17)$$

$$i_{L2}(t) = i_{L2}(t_8) + \frac{V_{C1} - V_o}{L_2}(t - t_8) \quad (18)$$

$$i_{D1}(t) = i_{L1}(t) + i_{L2}(t) \quad (19)$$

Mode 10 **[$t_9 \sim t_{10}$]**: At t=t_9, the gate pulse for the power switch S_2 disappears and the switch S_2 is turned-off. The diodes D_1 and D_2 provide the following path for the inductors L_1 and L_2, respectively. The currents i_{L1} and i_{L2} are decreased linearly with the rates of V_o/L_1 and V_o/L_2. When the gate pulse for the auxiliary switch S_{a1} is achieved, the next switching begins again.

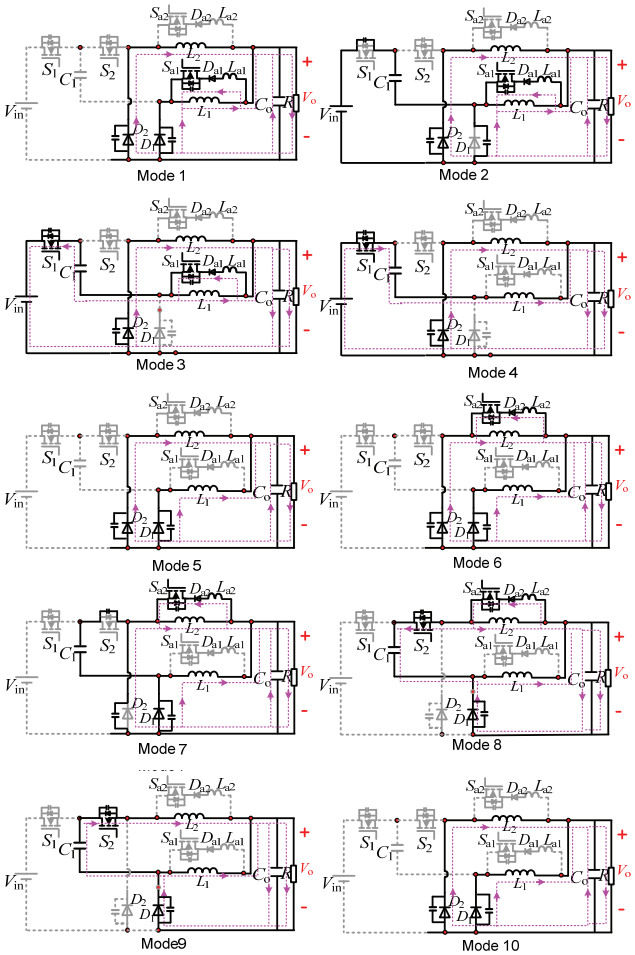


Fig. 3. Operational modes of the proposed converter.

III. Performance Analysis of the Proposed Converter

A. Voltage Transfer Gain

Based on the above analysis, in the case of D<0.5, the principle of the voltage-second balance is applied to the output inductors L_1 and L_2, and the following equations can be obtained as:

$$(V_{in} - V_{C1} - V_o)DT_s = V_o(1 - D)T_s \quad (20)$$

$$(V_{C1} - V_o)DT_s = V_o(1 - D)T_s \quad (21)$$

The voltage across the series capacitor and the DC voltage ratio can be expressed as:

$$V_{C1} = \frac{1}{2}V_{in} \qquad M = \frac{V_{in}}{V_o} = \frac{1}{2}D \quad (22)$$

It can be seen from equation (22) that the additional auxiliary zero voltage transition circuit has no effect on the voltage transfer gain. Moreover, the DC voltage ratio of the proposed converter is half that of the traditional interleaved buck converter. Thus, a higher step down ratio can be achieved when compared with the traditional buck converter.

B. Soft Switching Condition

1) Condition of Zero Voltage Switching for the Power Switches S_1 and S_2: Based on the analysis in section II, in order to achieve zero voltage switching of the power switches S_1 and S_2, there needs to be sufficient time to build the auxiliary inductor current and to decrease the voltage across the switch to zero. Therefore, the currents i_{La1} and i_{La2} should be made greater than the minimum of the currents i_{L1} and i_{L2}. In addition, they should complete the energy commutation of component in the converter. Thus, the requirement of the time interval of the auxiliary circuit for the switches S_1 and S_2 can be obtained as:

$$D_a T_s > \Delta T_{10} + \Delta T_{21} = \frac{I_o/2 - \Delta i_{L1}/2}{V_o / L_{a1}} + \pi\sqrt{L_{a1} C_{eq1}} \quad (23)$$

$$D_a T_s > \Delta T_{65} + \Delta T_{76} = \frac{I_o/2 - \Delta i_{L2}/2}{V_o / L_{a2}} + \pi\sqrt{L_{a2} C_{eq2}} \quad (24)$$

Where D_a is the duty cycle of the auxiliary switches S_{a1} and S_{a2}. T_s is the switching period. The current ripple of the output inductor currents i_{L1} and i_{L2} can be expressed as:

$$\Delta i_{L1} = \frac{V_o}{L_1}(1-D)T_s, \quad \Delta i_{L2} = \frac{V_o}{L_2}(1-D)T_s \quad (25)$$

2) Condition of Zero Current Switching for the Power Switches S_{a1} and S_{a2}: In order to achieve zero current switching for the auxiliary switches S_{a1} and S_{a2}, the current through the switches S_{a1} and S_{a2} should be reduced to zero. Thus, after the main switches S_1 and S_2 are turned-on, it needs external time to decay the currents i_{La1} and i_{La2} to zero. The condition of the ZCS switching for the auxiliary switches S_{a1} and S_{a2} can be obtained as:

For switch S_{a1}:

$$\begin{aligned} &D_a T_s > \Delta T_{10} + \Delta T_{21} + \Delta T_{32} \\ &= \frac{I_o/2 - \Delta i_{L1}/2}{V_o / L_{a1}} + \pi\sqrt{L_{a1} C_{eq1}} + \frac{I_o/2 - \Delta i_{L1}/2}{(V_{in} - V_{C1} - V_o)/L_{a1}} \end{aligned} \quad (26)$$

For switch S_{a2}:

$$\begin{aligned} &D_a T_s > \Delta T_{65} + \Delta T_{76} + \Delta T_{87} \\ &= \frac{I_o/2 - \Delta i_{L2}/2}{V_o / L_{a2}} + \pi\sqrt{L_{a2} C_{eq2}} + \frac{I_o/2 - \Delta i_{L2}/2}{(V_{C1} - V_o)/L_{a2}} \end{aligned} \quad (27)$$

Therefore, only the minimum times of the auxiliary switches S_{a1} and S_{a2} are greater than equations (26) and (27), and the ZCS switching can be achieved.

3) Zero Current Turn-off for the Output Diodes D_1 and D_2: Due to the existence of ZVT of the auxiliary circuit in mode 1, the turn-off slew rate of the current through the diodes D_1 and D_2 is limited by the auxiliary inductors L_{a1} and L_{a2}. Thus, soft turn-off for the output diodes D_1 and D_2 can be achieved and the reverse recovery losses of the fast-recovery diodes D_1 and D_2 are reduced.

C. Selection of the Resonant Inductors L_{a1} and L_{a2}

The resonant inductors L_{a1} and L_{a2} control the turn-off di/dt slew rate of the output diodes D_1 and D_2, and the reverse-recovery-related switching losses for the diodes can be reduced by slowing the turn-off di/dt slew rate. Thus, the resonant inductor is larger, and the reverse-recovery-related switching losses are lower. However, with a larger value of the inductors L_{a1} and L_{a2}, the resetting time of the resonant inductor becomes longer, and the conduction losses for the auxiliary switches are increased. Therefore, there exists a trade-off between the reverse-recovery-related switching losses for the diodes and the conduction losses for the auxiliary switches. Generally, the turn-off slew rate for the output diodes is keeping below 100A/μs to nearly eliminate the reverse-recovery-related switching losses of the fast recovery diodes, and the resetting time of the auxiliary inductor is within four times the diode's specified reverse recovery time t_{rr}. Thus, the selection condition of the resonant inductors L_{a1} and L_{a2} can be obtained as:

$$\begin{cases} V_o / L_{a1} \le 100A/\mu s \\ \dfrac{I_o/2 - \Delta i_{L1}/2}{(V_{in} - V_{C1} - V_o)/L_{a1}} < 4t_{rr} \end{cases} \quad (28)$$

$$\begin{cases} V_o / L_{a2} \le 100A/\mu s \\ \dfrac{I_o/2 - \Delta i_{L2}/2}{(V_{C1} - V_o)/L_{a2}} < 4t_{rr} \end{cases} \quad (29)$$

D. Stress Analysis and Selection of the Switches S_1, S_2 and S_{a1}, S_{a2}

1) The Main Power Switches S_1 and S_2, and the Diodes D_1 and D_2: Based on the above analysis, the voltage stress of the switch S_1 is equal to half of the input voltage, and the voltage stress of the switch S_2 is equal to the input voltage. The voltage stress of the output diodes D_1 and D_2 are clamped to half of the input voltage. Thus, the voltage stress can be expressed as:

$$V_{S1,stress} = 0.5V_{in}, V_{S2,stress} = V_{in}; \quad V_{D1,stress} = V_{D2,stress} = 0.5V_{in} \quad (30)$$

2) The Auxiliary Switches S_{a1} and S_{a2}: It can be seen from mode 4 and mode 9 that when the auxiliary switches S_{a1} and S_{a2} are turned-off, and the voltage across the auxiliary switch S_{a1} series diode D_{a1} or the auxiliary switch S_{a2} series diode D_{a2} is equal to the difference of half of the input voltage and the output voltage. Moreover, the zero current turn-on and zero current switching for the auxiliary switches S_{a1} and S_{a2} can be achieved. Thus, the switching turn-on losses and turn-off losses are very small and can be neglected. In the proposed converter, the conduction losses of the auxiliary switches should be carefully considered. In order to simplify the analysis, the quasi stepped square wave is assumed, as shown in fig. 4, for the auxiliary current. Thus, the average current stress and RMS current stress of the auxiliary circuit branch can be expressed as:

$$I_{ave} = \frac{1}{T_s}\left((\Delta T_1 + \Delta T_3) \cdot \frac{1}{2}\left(\frac{I_o}{2} - \frac{\Delta i_{L1,2}}{2}\right) + \left[\left(\frac{I_o}{2} - \frac{\Delta i_{L1,2}}{2}\right) + \frac{2V_o}{\pi Z_r}\right] \cdot \Delta T_2 \right) \quad (31)$$

TABLE I
LOSSES EQUATIONS OF THE PROPOSED CONVERTER OPERATED AT THE STEADY STATE

	I. The proposed converter	II. Series Capacitor Buck converter	III. InterleaveD Buck converter
RMS current stress of the switches S_1 and S_2	$\frac{I_o}{2}\sqrt{D}$	$\frac{I_o}{2}\sqrt{D}$	$\frac{I_o}{2}\sqrt{\frac{D}{2}}$
Conduction losses of the switches S_1 and S_2	$\frac{I_o^2}{4}D\cdot(R_{ds,on(S_1)}+R_{ds,on(S_2)})$	$\frac{I_o^2}{4}D\cdot(R_{ds,on(S_1)}+R_{ds,on(S_2)})$	$\frac{I_o^2}{4}\frac{D}{2}\cdot(R_{ds,on(S_1)}+R_{ds,on(S_2)})$
Voltage stress of the switch S_1	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	V_{in}
Voltage stress of the switch S_2	V_{in}	V_{in}	V_{in}
Peak current stress of the switches S1 and S2	$\frac{I_o}{2}+\frac{1}{2}\frac{0.5V_{in}-V_o}{L}DT_s$	$\frac{I_o}{2}+\frac{1}{2}\frac{0.5V_{in}-V_o}{L}DT_s$	$\frac{I_o}{2}+\frac{1}{4}\frac{V_{in}-V_o}{L}DT_s$
Switching losses of the switches S_1 and S_2	$\frac{1}{2}V_{(S_1)}I_{(S_1)}t_{off}f_s+\frac{1}{2}V_{(S_2)}I_{(S_2)}t_{off}f_s$	$\frac{1}{2}V_{(S_1)}I_{(S_1)}(t_{on}+t_{off})f_s$ $+\frac{1}{2}V_{(S_2)}I_{(S_2)}(t_{on}+t_{off})f_s$ $+\sum_i\frac{1}{2}C_{s(S_i)}V_{(S_i)}^2f_s$	$\frac{1}{2}V_{(S_1)}I_{(S_1)}(t_{on}+t_{off})f_s$ $+\frac{1}{2}V_{(S_2)}I_{(S_2)}(t_{on}+t_{off})f_s$ $+\sum_i\frac{1}{2}C_{s(S_i)}V_{(S_i)}^2f_s$
Average current stress of the output diode D_1	$\frac{I_o}{2}$	$\frac{I_o}{2}$	$\frac{I_o}{2}(1-\frac{D}{2})$
Average current stress of the output diode D_2	$\frac{I_o}{2}(1-D)$	$\frac{I_o}{2}(1-D)$	$\frac{I_o}{2}(1-\frac{D}{2})$
Reverse-recovery switching losses for the diodes D1 and D2	$\sum_i V_F I_{ave(Di)}$	$\sum_i V_F I_{ave(Di)}+\sum_i\frac{1}{2}V_{(D_i)}I_{(D_i)}t_{rr}f_s$	$\sum_i V_F I_{ave(Di)}+\sum_i\frac{1}{2}V_{(D_i)}I_{(D_i)}t_{rr}f_s$
Conduction losses of the auxiliary switches and diodes	$\sum_i V_F I_{ave(Dai)}+\sum_i R_{ds,on(S_{ai})}i_{rms(S_{ai})}^2$	--------	--------

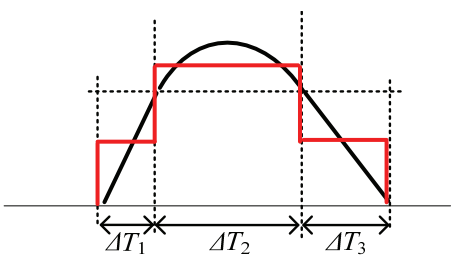


Fig. 4. Equivalent waveform of the auxiliary inductor current i_{La1} or i_{La2}.

$$I_{rms}=\sqrt{\frac{1}{T_s}\int i_{La}^2 dt}$$
$$=\sqrt{\frac{1}{T_s}\left((\Delta T_1+\Delta T_3)\cdot\frac{1}{4}(\frac{I_o}{2}-\frac{\Delta i_{L1,2}}{2})^2+[(\frac{I_o}{2}-\frac{\Delta i_{L1,2}}{2})+\frac{2V_o}{\pi Z_r}]^2\cdot\Delta T_2\right)} \quad (32)$$

Where the time intervals ΔT_1, ΔT_2 and ΔT_3 are the intervals of the auxiliary current charging time, resonant time and discharging time, respectively. $\Delta i_{L1,2}$ is the peak-peak ripple of the current i_{L1} or i_{L2}. I_o is the output load current.

IV. LOSS ANALYSIS

In order to evaluate the performance of the proposed converter, a loss breakdown of the ZVT series capacitor interleaved buck converter should be given. Based on the above analysis, through appropriate selection of the parameters of the proposed converter, the zero voltage switching of the main switches and the zero current switching of the auxiliary switches, the reverse-recovery switching losses of the main diodes can be eliminated over wide load and input voltage ranges. Therefore, when compared with the traditional series capacitor buck converter, the efficiency of the proposed converter has an advantage since the additional conduction losses caused by the auxiliary circuit are less than the reduced switching losses. Thus, the loss factors of the proposed converter considered in the analysis are as follows. 1) The conduction losses and turn-off loss of the main switches S1 and S2. 2) The conduction losses of the main diodes D1 and D2. 3) The conduction losses of the auxiliary switches and diodes.Firstly, the turn-on switching losses and capacitive discharging losses of the power switches are eliminated. Thus, only the conduction losses and turn-off losses of the main switches are considered in the loss analysis. For the switches S_1 and S_2, the related losses can be expressed as:

$$\begin{aligned}P_{sw(S_1)}&=\sum_i R_{ds,on(S_i)}i_{rms(S_i)}^2+\sum_i\frac{1}{2}V_{(S_i)}I_{(S_i)}t_{off}f_s\\&=R_{ds,on(S_1)}i_{rms(S_1)}^2+R_{ds,on(S_2)}i_{rms(S_2)}^2\\&\quad+\frac{1}{2}V_{(S_1)}I_{(S_1)}t_{off}f_s+\frac{1}{2}V_{(S_2)}I_{(S_2)}t_{off}f_s\end{aligned} \quad (33)$$

Next, due to the limited turned-off rate of the output diodes, the reverse-recovery switching losses are neglected in the

proposed converter. Thus, only the conduction losses are considered. For the output diodes D_1 and D_2, the related losses can be obtained as:

$$P_{sw(S_i)} = \sum_i V_F I_{(D_i)} = V_F I_{(D1)} + V_F I_{(D2)} \quad (34)$$

Finally, considering the losses caused by the auxiliary circuit, and due to the zero current turn-on and zero current switching turn-off for the auxiliary switches S_{a1} and S_{a2}, the switching related losses can be neglected. Therefore, for the auxiliary circuit, the conduction losses can be expressed as:

$$\begin{aligned} P_{sw(S_{ai},D_{ai})} &= \sum_i R_{ds,on(S_{ai})} i^2_{rms(S_{ai})} + \sum_i V_F I_{(D_{ai})} \\ &= R_{ds,on(S_{a1})} i^2_{rms(S_{a1})} + R_{ds,on(S_{a2})} i^2_{rms(S_{a2})} + V_F I_{(Da1)} + V_F I_{(Da2)} \end{aligned} \quad (35)$$

A comparison losses analysis of the proposed converter, the traditional series capacitor buck converter and the traditional interleaved buck converter are shown in Table I. It can be seen from this table that the conduction losses of the switches S_1 and S_2 are the same for the three converters due to half of duty cycles with the same output voltage. Moreover, the switching losses of the main switch and capacitive losses are eliminated in the proposed converter when compare with the series capacitor converter and the interleave buck converter. The reverse recovery switching losses for the output diodes can be eliminated in the proposed converter. However, the conduction losses of the auxiliary circuit are added and zero current switching for auxiliary switch is achieved. Thus, the condition where the additional conduction losses are smaller than the reduced switching losses of the main switch and the reverse recovery switching losses for the output diodes is guaranteed, and the efficiency of the proposed converter can be improved.

V. Experimental Results

A. Design Example

In order to verify theoretical analysis of the proposed converter, an experimental prototype of the ZVT series capacitor buck converter was established in the laboratory. The specifications of the converter are given as follows: 1) input voltage V_{in}=100V; 2) output voltage V_o=10V; 3) switching frequency f_s=100kHz. Thus, the duty cycle of the main switches S_1 and S_2 can be calculated as D=0.24. According to the stress analysis in the above section, the *IPB020N10N5* is selected for the main power switch S_1, and the switches S_{a1} and S_{a2}. The *IPB110N20N3* is selected as the main power switch S_1, and the output diodes D_1, D_2, D_{a1} and D_{a2} are MBR40250T (V_F=0.86V,T_{rr}=35ns,C_T=500pF). Based on the previous analysis, the auxiliary inductor should have a trade-off between additional conduction losses and duty cycle laminations of the auxiliary switch. Therefore, auxiliary inductors L_{a1}=L_{a2}=2.2μH are selected in this paper. In order to achieve zero voltage turned-on for the main switches S_1 and S_2, the duty cycle of the auxiliary switch can satisfy equations (24) and (25). Thus, the turn-on time for the auxiliary switch should be larger than 0.4μs. Furthermore, in order to achieve zero current turn-off for the auxiliary switches S_{a1} and S_{a2}, based on the equations (27) and (28), the duty cycle D_a should be larger than 0.48. The selected parameter of the passive components and semiconductors are shown in Table II.

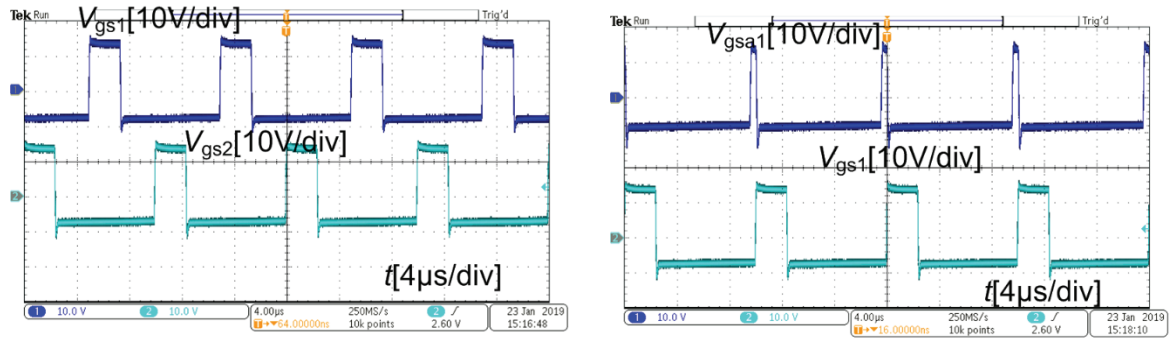
TABLE II
Parameters of the Proposed Converter

Specifications	Main parameters
The Switch (S_1,$S_{a1/2}$)	IPB020N10N5 (100V)
The Switch S_2	IPB110N20N3 (200V)
Diodes (D_1,D_2,D_{a1},D_{a2})	MBR40250T
Main inductor L_1,L_2	100μH
Auxiliary inductor L_{a1},L_{a2}	2.2μH
Capacitor C_1	2.2μF
Output Capacitor C_o	330μF

B. Waveforms

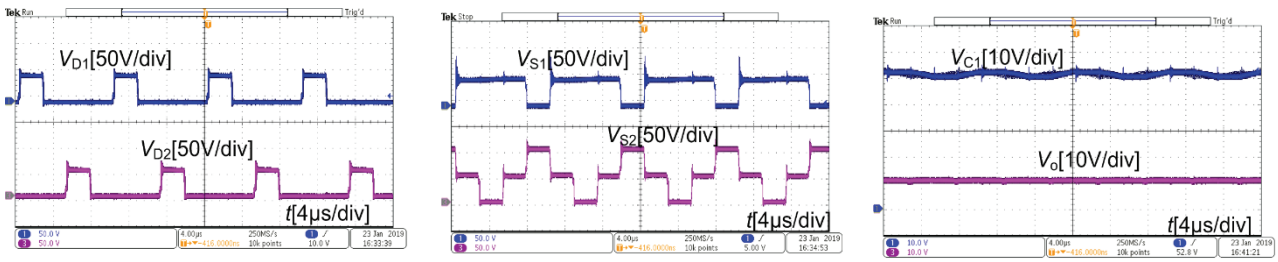
Fig. 5 shows gate pulse waveforms for the main switch and auxiliary switch. Key waveforms of the proposed converter are given in Fig. 6. It can be seen from Fig. 6 that the voltage stresses of the switch S_1 and the diodes D_1 and D_2 are equal to half of the input voltage V_{in}. It can also be seen that the voltage of the switch S_2 is a trapezoidal-type waveform. Thus, it corresponds to the theoretical analysis. In addition, the turned-off loss can be reduced, and the switching losses are reduced. Moreover, the voltage across the intermediate capacitor is equal to half of the input voltage. Thus, auto current sharing can be guaranteed. The operating time of the auxiliary circuit is very low and the current through the auxiliary circuit has no effect on the main power switches. Voltage and current waveforms of the main switch in the proposed converter are shown in Fig. 7. It can be seen from the full load and half load waveforms in Fig. 7(a) and (b) and (c) and (d), that the ZVS for the switches S_1 and S_2 is achieved and switching losses are reduced due to the low turn-off di/dt.

Fig. 8 shows voltage waveforms of the auxiliary switches S_{a1}/S_{a2} and current waveforms of the auxiliary inductor L_{a1}/L_{a2}. It can be seen from Fig. 8 that the zero current and zero voltage of S_{a1}/S_{a2} can be achieved at full load and 50% load. In the experiment results, the auxiliary switch S_{a1}/S_{a2} and diode D_{a1}/D_{a2} share the voltage stress of V_{in}/2. Thus, the voltage stress across the switches S_{a1}/S_{a2} is about V_{in}/4. The zero current turn-on and zero voltage turn-on of the switches S_{a1}/S_{a2} is obtained since the current through the auxiliary inductor commutes with the output diode. In addition, when the current through the diode is decreased to zero, the current i_{La1}/i_{La2} increased. Therefore, the added switching losses on



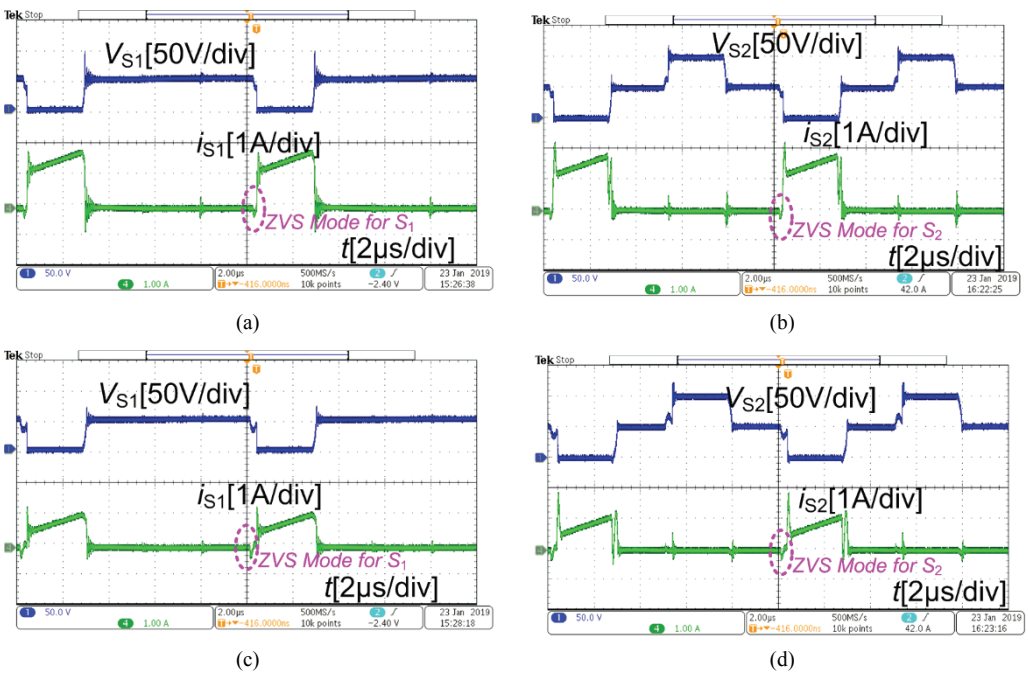
(a) (b)

Fig. 5. Gate pulse waveforms for the main switch and auxiliary switch. (a) Gate pulse of the switches S_1 and S_2. (b) Gate pulse of the switches S_{a1} and S_1.



(a) (b) (c)

Fig. 6. Key waveforms of the proposed converter. (a) Voltage across the main switches S_1 & S_2 and the diodes D_1 & D_2. (b) Voltage V_{C1} of the intermediate energy storage capacitance and output voltage V_o. (c) Current through the auxiliary inductor L_{a1}.



(a) (b) (c) (d)

Fig. 7. ZVS waveforms of the main switch S_1 and the switch S_2. (a) At full load. (b) At full load. (c) At 50% load. (d) At 50% load.

the auxiliary switches are very low and can be ignored. Moreover, the additional conduction losses caused by the auxiliary circuit are less than the reduced switching losses due to the low RMS of the auxiliary current. Thus, the performance of the proposed converter can be improved.

C. Efficiency

Fig. 9 shows the efficiency measured under different load conditions when the input voltage is 100 V. As can be seen in this figure, the proposed converter has improved efficiency

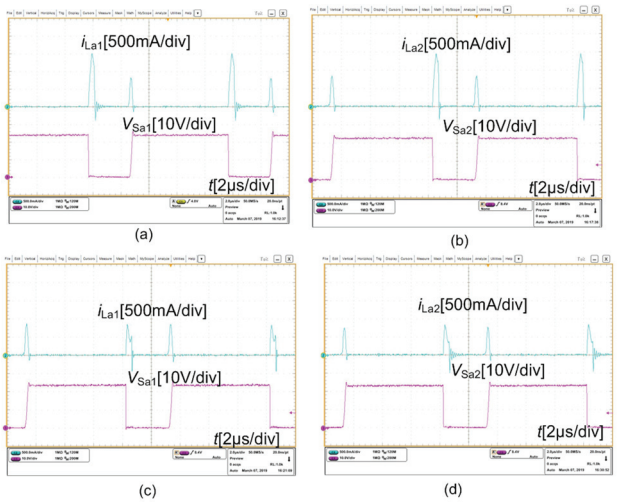


Fig. 8. Voltage waveforms of the switch S_{a1}/S_{a2}. (a) At full load. (b) At full load. (c) At 50% load. (d) At 50% load.

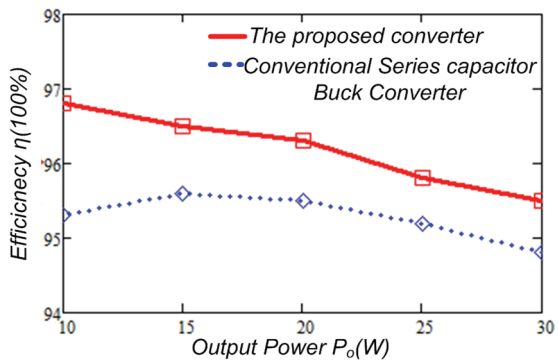


Fig. 9. Efficiency comparison of the proposed converter.

when compared with the traditional series buck converter. It is also indicated that the additional conduction losses of the proposed converter are less than the reduced switching loess of the main switches and reverse recovery loss of the diodes. This occurs in the proposed converter because the ZCS-ZVS PWM circuit cell is utilized, zero voltage transition of the main power switches are achieved and zero current switching of the auxiliary switches are obtained in a wide operating range. Moreover, the additional conduction losses caused by the auxiliary circuit are very small due to the small operating time of the auxiliary circuit. Furthermore, the proposed technique does not increase the voltage stress or current stress of the main switches and diodes, as can be seen in the experimental waveforms. Thus, the proposed converter has better performance when compared with the traditional series capacitor buck converter.

VI. Topology Variations of the Proposed Converter

In the above analysis, the zero voltage transition series capacitor interleaved buck converter prevails over the traditional series buck converter and the interleaved buck converter.

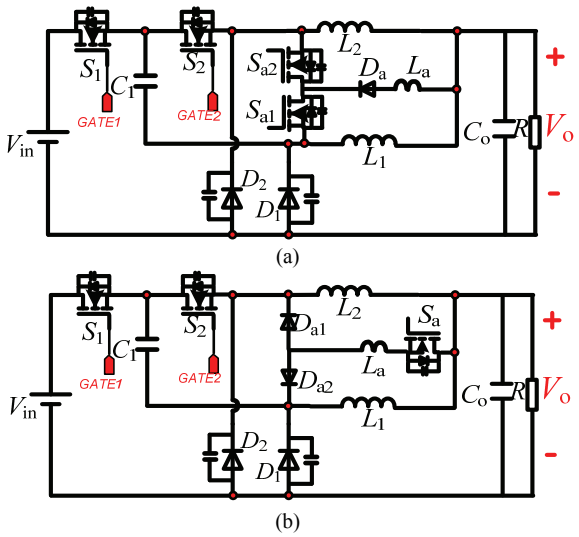


Fig. 10. Topology variations of the proposed converter.

However, two additional auxiliary switches, two diodes, and auxiliary inductors are used to obtain this character. As a result, the cost and complexity of the proposed converter are increased. In order to simplify the proposed converter topology, two topology variations of the proposed converter are shown in Fig. 10. In the ZVT auxiliary circuit for the proposed converter, the branch of the auxiliary series diode and inductor is commonly used, and the derived topology is shown in Fig. 10(a). In this figure, the gate pulse waveforms of the main switch and the auxiliary switch are the same as the previously analyzed converter in this paper. Thus, one auxiliary inductor and diode are eliminated.

In Fig. 10(b), only one auxiliary switch is utilized. Thus, the gate pulse waveform for the switch S_a should be conducted twice in one switching period.

VII. Conclusion

This paper presented a zero voltage transition (ZVT) series capacitor interleaved buck converter. The operational principle and a relevant analysis of the proposed converter are developed. In addition, the DC voltage gain ratio, the soft switching condition and a design guideline of the critical parameters are given in this paper. Furthermore, a loss analysis of the proposed converter is described. Experimental results show that zero voltage transition of the main power switches are achieved and that the reverse recovery losses of the output diodes are reduced without increasing the voltage stress or current stress of the main switches and diodes. The additional conduction losses caused by the auxiliary circuit are very small due to the small operating time of the auxiliary circuit. Based on these merits, the proposed zero voltage transition (ZVT) series capacitor interleaved buck converter with high step-down power-conversion can be used in the power sources for microprocessors, automotive applications, LED drivers, solar-power regulators and so on.

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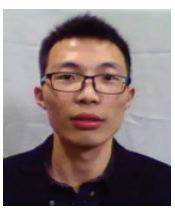
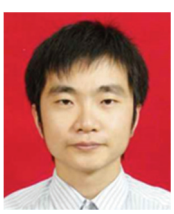
Zhangyong Chen was born in Sichuan Provence, China, in 1988. He received his B.S. degree in Electrical Engineering and its Automation, and his Ph.D. degree in Electrical Engineering from Southwest Jiaotong University (SWJTU), Chengdu, China, in 2010 and 2015, respectively. From September 2014 to September 2015, he was a Visiting Student in the Future Energy Electronics Center (FEEC), Virginia Tech, Blacksburg, VA, USA. In January 2016, began working as a Lecturer in the School of Energy Science and Engineering, and since August 2018, he has been an Associate Professor in the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China. His current research interests include switching-mode power supplies, soft switching techniques, power factor correction converters and renewable energy sources.

Yong Chen (SM'16, M'08) was born in Sichuan Province, China, in 1977. Since 2015, he has been a Professor and a Ph.D. Supervisor in the School of Energy Science and Engineering, and a Professor in the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China. He also served as the Director of the Institute for Electric Vehicle Driving System and Safety Technology, UESTC. He was a Visiting Scholar in the School of Mechanical Engineering, University of Adelaide, Adelaide, SA, Australia. Since January 2018, he has been presiding over a National Natural Science Foundation of China project and over Scientific and Technical Supporting Programs in Sichuan Province. He has published over 50 technical papers in journals and conference proceedings. In addition, he has 15 Chinese patents. His current research interests include power electronics, motor control, energy control and network control. He is a Senior Member of the IEEE, and a Member of the Chinese Society for Electrical Engineering (CSEE).



Wei Jiang was born in Sichuan Province, China, in 1993. He received his B.S. degree in Electrical Engineering from the School of Electrical Engineering and Electronic Information, Xihua University, Chengdu, China, in 2017. He is presently working towards his M.S. degree in Control Engineering in the School of Automation Engineering, University of Electronic Science and Technology of China (UESTC), Chengdu, China. His current research interests include switching-mode power supplies and soft switching techniques.



Tiesheng Yan was born in Shanxi, China, in 1981. He received his B.S. degree in Mechatronic Engineering from Lanzhou Railway University, Lanzhou, China, in 2002; and his M.S. and Ph.D. degrees in Power Electronics and Electrical Transmission from Southwest Jiaotong University, Chengdu, China, in 2005 and 2015, respectively. He was an Analog Application Manager at O2Micro China from May 2005 to May 2015. Since July 2015, he has been working as an Associate Professor at Xihua University, Chengdu, China. His current research interests including switching-mode power supplies, power factor correction converters and renewable energy sources.