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게이트 드라이버가 집적된 GaN 모듈을 이용한 48V-12V 컨버터의 설계 및 효율 분석

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Design and Efficiency Analysis 48V-12V Converter using Gate Driver Integrated GaN Module

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Abstract

This study presents the design and experimental result of a GaN-based DC - DC converter with an integrated gate driver. The GaN device is attractive to power electronic applications due to its superior device performance. However, the switching loss of a GaN-based power converter is susceptible to the common source inductance, and converter efficiency is severely degraded with a large loop inductance. The objective of this study is to achieve high-efficiency power conversion and the highest power density using a multiphase integrated half-bridge GaN solution with minimized loop inductance. Before designing the converter, several GaN and Si devices were compared and loss analysis was conducted. Moreover, the impact of common source inductance from layout parasitic inductance was carefully investigated. Experimental test was conducted in buck mode operation at 48 - 12 V, and results showed a peak efficiency of 97.8%.

Key words: GaN device, Common source inductance, Synchronous buck converter, Power loss calculation

1. Introduction

Synchronous buck converters have become a promising solution for many power conversion applications due to its high efficiency with bidirectional power flow capability. The power density of synchronous buck has been significantly improved with the recent advances in GaN technology and makes it more attractive to automotive industry. To fully utilize the performance of GaN devices, PCB layout and gate driver circuit have to be carefully designed to supress the voltage ringing and coupling noise[1]. This paper presents the benefit of using an integrated GaN solution for a synchronous buck converter, which provides the high efficiency power conversion with minimized common source inductance. In the following section, the total power loss of similarly rated devices are calculated and the merit of the integrated solution is investigated. Finally, the prototype hardware test results are provided.

2. Device Characteristic Comparison

Table 1 shows the device parameters of the similarly rated devices[2]-[5]. The rated drain to source voltage V_{DS} for GaN System device(GS6100SP) is rated for 100 V, and the rest of devices are rated for 80 V. Si device from Infineon(IPB017N08N5) has the lowest drain to source resistance R_{DS} and the integrate GaN solution from Texas Instruments (LMG5200) has the highest R_{DS} and obviously, it has the highest conduction loss. The overall device losses are not only determined by R_{DS} but also affected by the switching loss, which is directly related to the switching gate charge Q_{SW} which is defined as

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TABLE I
GAN AND SI DEVICE CHARACTERISTICS

		Vds [V]	Rds [$m\Omega$]	Qg [nC]	Qgs [nC]	Qsw [nC]	Qoss [nC]	Figure of Merit
GaN	EPC2021	80	2.5	15	3.8	4	56	10
	GS6100SP	100	7.4	16	3.0	8.5	30	63
	LMG5200	80	18	3.8	(0.9)	(0.95)	20	N/A
Silicon	IPB017N08N5	80	1.7	17	57	59	207	100.3

$Q_{GS}/2+Q_{GD}$. The figure of merit(FOM), which is the multiplication of R_{DS} and Q_{SW} is the most important criteria for selecting the appropriate device. Smaller FOM is preferred for high efficiency design. Q_{SW} of LMG5200 is not specified but it is assumed that Q_{SW} of LMG5200 is smilar to EPC2105. In Table 1, Q_{GS} of GaN devices are lowered by one order of magnitude over Si device and eventually makes FOM relatively low.

3. Power Loss Calculation

The power loss of each device was calculated based on equations provided in [6].

3.1 Conduction Loss

The conduction loss of the high side and low side switching devices is

$$P_{cond(HS)} = R_{DS(HS)} \times I^2_{DS,RMS(HS)} \quad (1)$$

$$P_{cond(LS)} = R_{DS(LS)} \times I^2_{DS,RMS(LS)} \quad . \quad (2)$$

The RMS value of Drain to Source current $I_{DS,RMS}$ can be found from the duty cycle D, output current I_O and current ripple I_{ripple}

$$I_{RMS(HS)} = \sqrt{\frac{D}{3}(I_{O,Max}{}^2 + I_{O,Max}I_{O,Min} + I_{O,Min}{}^2} \quad (3)$$

$$I_{RMS(LS)} = \sqrt{\frac{D'}{3}(I_{O,Max}{}^2 + I_{O,Max}I_{O,Min} + I_{O,Min}{}^2)} \quad (4)$$

$$I_{O,Max} = I_O + \frac{I_{ripple}}{2} \quad (5)$$

$$I_{O,Min} = I_O - \frac{I_{ripple}}{2} \quad . \quad (6)$$

3.2 Switching Loss

The switching loss from high side FET is calculated as

$$P_{SW} = V_{IN} \times I_O \times f_{SW} \times \frac{Q_{SW}}{I_G} \quad (7)$$

TABLE II
THE CALCULATED COMMON SOURCE INDUCTANCE

Device	EPC2021	GS6100SP	LMG5200	IPB017N8N5
L_{CSI} [nH]	1.12	0.6	0.1	1.49

where V_{IN}, f_{SW} and I_G are input voltage, switching frequency, and gate driving current respectively. The gate driving current can be found from gate driving voltage V_{drive}, gate driver inner resistance R_{driver}, external gate resistance R_G, and plateau voltage V_{PL}

$$I_G = \frac{V_{driver} - V_{PL}}{R_G + R_{driver}} . \quad (8)$$

The switching loss for the low side FET is ignored because it turns on and off during the freewheeling period and achieves zero voltage switching(ZVS).

The common source inductance(CSI) is the inductance seen from the main current path and it carries the drain source current I_{DS} and the gate charging current I_G. Mainly it is originated from device package parasitics L_{Pack} and circuit layout parasitics L_{PCB}. The parasitic inductance from circuit layout inductance can be calculated as

$$L = \mu_0 \frac{h}{w} l \quad (9)$$

where w and l are width and length of the trace, and h is dielectric thickness[7]. Fig. 1 shows the synchronous buck converter circuit diagram with common source inductance between high side FET and low side FET.

When the high side FET is turned on, L_{CSI} induces a negative voltage across gate to source capacitance C_{GS} and it slows down the gate turn on process. The effective V_{GS_Eff} is presented as

$$V_{GS\_Eff} = V_G - V_{SW} - L_{CSI} \frac{di_{DS}}{dt} \quad (10)$$

where V_G. V_{SW} are gate voltage and switching node voltage with respect to the ground. Also, the LCR resonant tank existing in gate driver loop causes

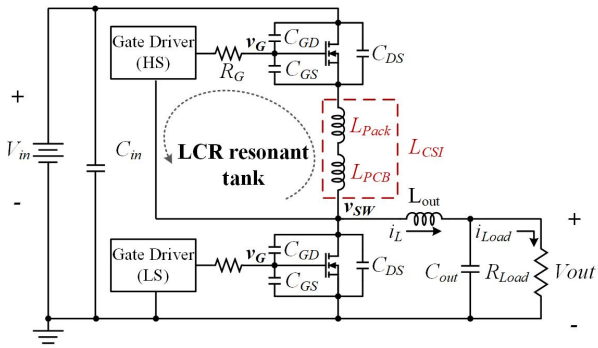


Fig. 1. The circuit diagram of a synchronous buck converter with the common source inductance.

TABLE Ⅲ
THE POWER LOSS CALCULATION AT 500 W

	IPB017 N8N5	EPC 2021	GS6100SP	LMG 5200
P_{cond} (W)	5.90	3.42	12.00	30.74
P_{SW} (W)	25.10	9.48	4.08	3.65
P_{gate} (W)	0.45	0.03	0.04	0.04
P_{dead} (W)	0.92	1.08	1.99	1.50
P_{RR} (W)	1.85	0.00	0.17	0.00
P_{COSS}	1.24	0.26	0.31	0.33
P_{Total} (W)	35.45	14.28	18.58	36.25

voltage ringing during this period[8]. Therefore, the gate driver circuit and PCB layout has to be carefully designed. L_{CSI} from parasitic inductances are calculated from the manufacturer's layout examples and device package infomration. All GaN devices are lead-free and accordingly the parasitic inductance induced by device package is small compare to the Si device with lead terminal.

3.3 Gate Driver Loss

The gate driver power loss are found from gate charge Q_G, V_{driver}, and f_{SW}

$$P_{gate} = P_{gate(HS)} + P_{gate(LS)} = (Q_{g(HS)} + Q_{g(LS)}) \times V_{driver} \times f_{SW} \quad (11)$$

3.4 3rd Quadrant Conduction Loss

During the deadtime, the inductor current flow from drain to source of the low side enhancement mode GaN[9]. For Si device, the body diode or anti parallel diode provide the conduction path.

$$P_{dead} = V_{SD} \times [I_{O,Min} \times t_{dead,r} + I_{O,Max} \times t_{dead,f}] \times f_{sw} \quad (12)$$

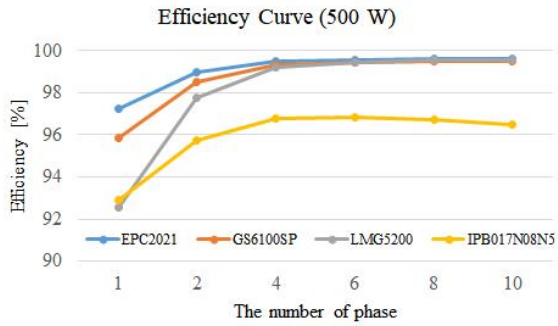


Fig. 2. Efficiency curve of with respect to the number of phases.

3.5 Reverse Recovery Loss

The reverse recovery loss comes from low side FET is

$$P_{RR} = Q_{RR(LS)} \times V_{IN} \times f_{SW} \quad (13)$$

where Q_{RR} is the reverse recovery charge of the switching device.

3.6 Output Capacitance Loss

$$P_{C\_OSS} = 0.5(Q_{OSS(HS)} + Q_{OSS(LS)}) \times V_{IN} \times f_{sw} \quad (14)$$

where Q_{OSS} is the output charge of the switching device.

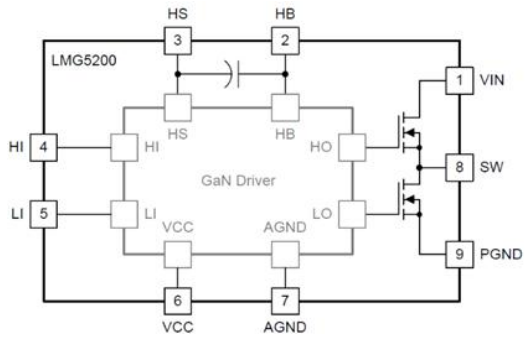
3.7 Total Loss Comparison

Table Ⅲ shows the total calculated power loss which includes switching loss, conduction loss, gate driver loss, dead time loss, reverse recovery loss and output capacitance loss. The output power is 500 W and the switching frequency is 250 kHz. The calculation of switching loss includes the impact of L_{CSI}[6]. Fig. 2 presents the efficiency of the converter with respect to the number of phases. The calculation results shows that the efficiency of LMG 5200 is not attractive. However, as shonw in Fig. 2, the performance of LMG5200 approaches to discrete devices in multi phase configuration.

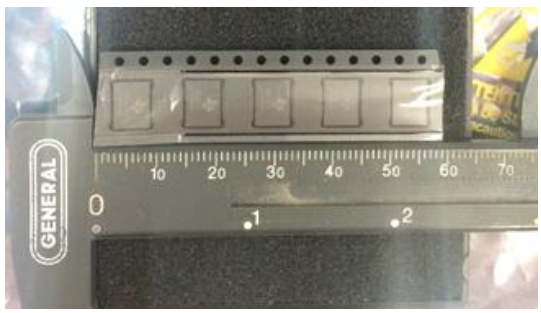
The interleaving effectively reduce P_{total} by reducing P_{cond}. For example, P_{cond} of 6 phase interleaving converter is only $(1/6)^2$ of that of single phase converter. Accordingly, LMG5200, which has the largest R_{DS} takes a huge advantage of interleaving.

4. Experimental Result

Experimental test was conducted to verify the performance of an integrated half-bridge GaN solution.



(a) Diagram of LMG5200[5]



(b) Picture of LMG5200

Fig. 3. Information of LMG5200.

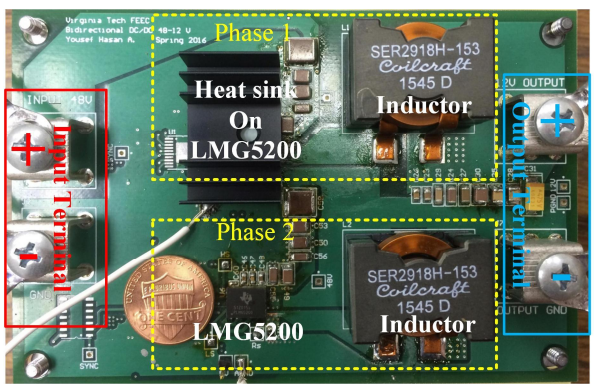


Fig. 4. The PCB board design of prototype synchronous buck converter using LMG 5200.

Fig. 3 shows the diagram and picture of LMG5200. Fig. 4 shows the prototype converter circuit. The size of PCB board is 12 cm x 8 cm x 1.5 cm and LMG5200, is used for each phase, which has gate drivers, boot strap circuit and 2 GaN FETs. The selected inductor is SER2918H-153(L = 15 uH) from Coilcraft.. The input voltage is 48 V and output voltage is 12 V and the switching frequency is 250 kHz. The board has two phase dc-dc converter. In phase 1, a heat sink is attached to LMG5200 for thermal management. In phase 2, LMG5200 without a heat sink is mounted and a penny is placed to show the size of the integrated GaN solution.

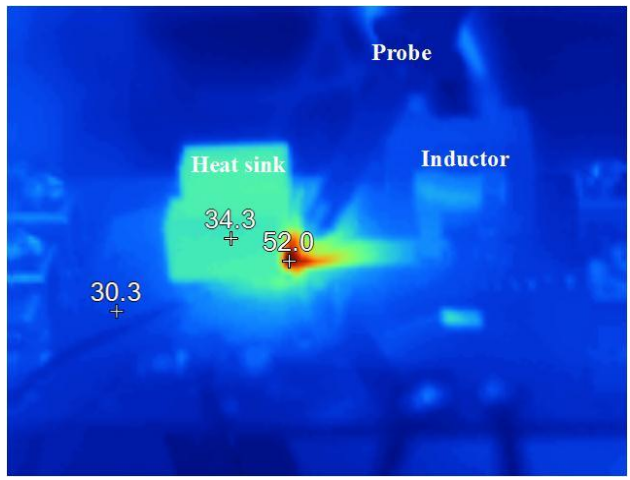


Fig. 5. Thermal image of synchronous buck converter under 100% load after 30min operation.

The converter was originally designed for 6 phase interleaving operation. However, only one phase converter is verified in this simulation to see the efficiency and switching characteristics. Thermal image under 100% load is provided in Fig. 5. The probe is placed as close as possible to the switching node of LMG5200 to see the switching wave form of low side GaN FET. A spring ground is used to minimize the loop inductance. The room temperature was 28 ℃. In Fig. 5, the heat sink temperature is 34.3 ℃ and the board stayed below 30.5 ℃ under the full load condition with out a cooling fan. The maximum temperature was 52 ℃ in right side of heat sink. This is due to the PCB design that has a small diameter via which does not provide an enough current path. The issue can be solved with the revised PCB design. Turn on and turn off transient waveform is provided in Fig. 6 and Fig. 7. The dead time t_{dead} was set to 13.3 ns for both turn on and turn off period. The propagation delay t_{propa} was 29.5 ns. The gate to source voltage V_{GS} for both high side and low side are provided and the low side drain to source voltage $V_{DS(LS)}$ is presented. In Fig. 6, the turn off transient does not have severe ringing in $V_{DS(LS)}$. However, In Fig. 7, a huge voltage ringing from LCR tank is shown. Also, a negative voltage drop V_{SD} during the 3rd quadrant conduction mode is shown. If t_{dead} is not optimized, the conduction loss from V_{SD} can significantly lower the overall efficiency. Fig. 7. shows the efficiency curve of the converter. The efficiency was measured from 2 A(25% of load) to 8 A(100% of load). The maximum efficiency was 97.8 %.

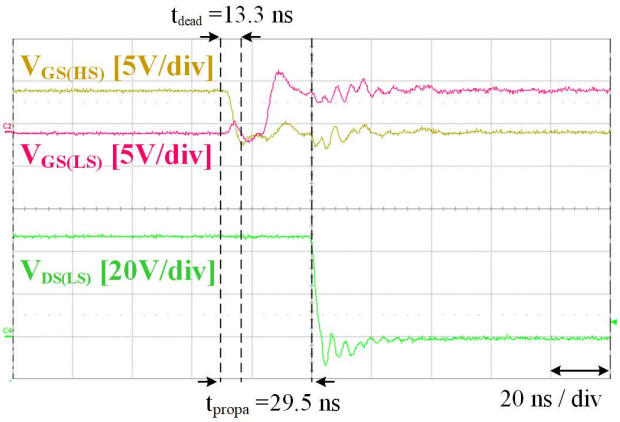


Fig. 6. Turn on waveform of low side GaN FET.

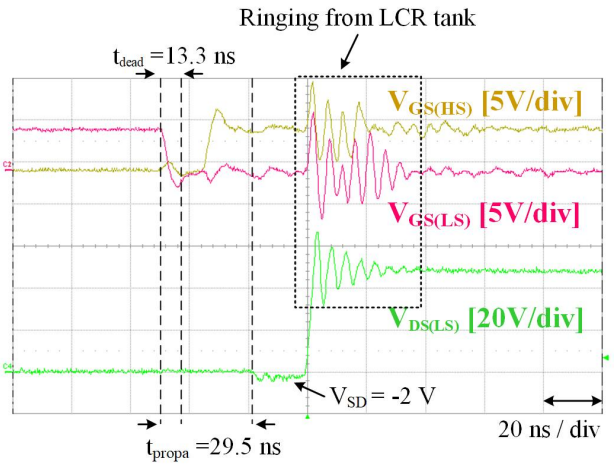


Fig. 7. Turn off waveform of low side GaN FET.

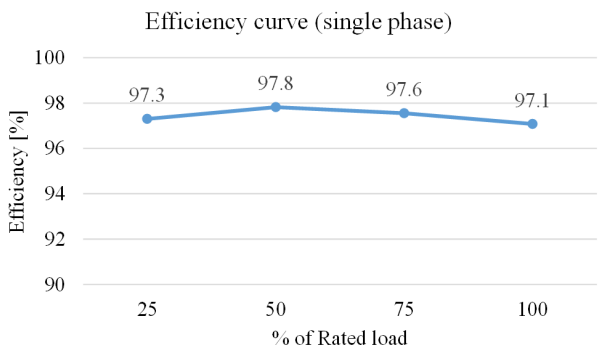


Fig. 8. The efficiency curve of prototype hardware.

5. Conclusion

48V-12V DC-DC converter using integrated GaN power stage was designed and tested with prototype hardware. This gate driver integrated half bridge module can save a lot of effort of designing stable gate driver circuit. By reducing a complicated gate drive circuit, manufacturing failure and cost will be way more reduced compare with discrete device. Also, the minimized layout parasitic inductance and integrated gate drive circuit in the GaN power module minimized the effect of common source inductance and simplified the PCB layout. The test results showed that the designed converter achieved 97.8 % peak efficiency. For the future work, the operation of multi phase interleaving will be verified.

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