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Analysis and Implementation of High Step-Up DC/DC Convertor with Modified Super-Lift Technique

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Abstract

In this paper, a new high step up DC/DC converter with a modified super-lift technique is presented. The coupled inductor technique is combined with the super-lift technique to provide a tenfold or more voltage gain with a proper duty cycle and a low turn ratio. Due to a high conversion ratio, the voltage stress on the semiconductor devices is reduced. As a result, low voltage ultra-fast recovery diodes and low on resistance MOSFET can be used, which improves the reverse recovery problems and conduction losses. This converter employs a passive clamp circuit to recycle the energy stored in the leakage inductance. The proposed convertor features a high conversion ratio with a low turn ratio, low voltage stress, low reverse recovery losses, omission of the inrush currents of the switch capacitor loops, high efficiency, small volume and reduced cost. This converter is suitable for renewable energy applications. The operational principle and a steady-state analysis of the proposed converter are presented in details. A 200W, 30V input, 380V output laboratory prototype circuit is implemented to confirm the theoretical analysis.

Key words: Coupled inductor, DC-DC convertors, High step up converter, Non-isolated technique, Super-lift technique

I. INTRODUCTION

Nowadays, the utilization of renewable energy sources is expanded more and more due to their clean and cost-effective features [1], [2]. However, renewable energy sources such as photovoltaic panels, fuel cell, etc. provide a low DC voltage (typically lower than 50 V). In order to connect these sources to an AC load or network, the output voltage should be increased to a higher voltage level (typically 300V-400V). The conventional boost converter cannot provide such a high conversion ratio due to the high voltage stress on the switch and extreme operating duty cycle problems [3], [4]. Thus, DC/DC high step up converters are required. These converters are applied in other applications such as high-intensity discharge lamps (HID) for automobile headlamps, battery backup systems for uninterrupted power supplies (UPS) and power supplies in the telecommunication industry [3], [5].

Several techniques having been presented in the literature to provide a high voltage gain such as the voltage-lift or/and voltage-multiplier technique, cascading techniques, employing transformers and coupled inductors, etc. [6], [7]. The voltage-lift or/and voltage-multiplier technique uses a switch capacitor circuit. The parallel charging and series discharging of the capacitors can result in a high voltage gain that is dependent on the number of switches and capacitors [3], [8]. By cascading two step-up converters, a high voltage gain is achievable [9]. The main drawback of this technique is the high voltage and current stress on the switch. Although the voltage stress can be reduced by employing coupled inductors, the conduction losses still increase due to the high current stress of the switch [2]. The other technique employs transformers in the boost converter. Some topologies that utilizes this technique are presented in [10], [11]. In these topologies, the high voltage gain can be adjusted by two degrees of freedom,

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which are the duty cycle and the turn ratio. The main drawbacks of this technique are a high voltage spike on the switch and losses due to the leakage inductance. In order to solve the high voltage spike problem, employing a snubber circuit and a clamp circuit is unavoidable, which increases the system cost. However, this still leaves the problem of the leakage inductance losses [5]. When galvanic isolation is not required, the use of non-isolated coupled inductors is preferred due to their simpler winding structure, lower conduction losses, and continuous conduction current at the primary winding, which results in a smaller primary winding current ripple and lower input filtering capacitance [7]. This technique can also provide a high voltage gain with two degrees of freedom: the duty cycle and the turn ratio. However, it still suffers from the main drawbacks of transformer-based circuits. The first problem can be solved by employing an active/passive clamp circuit [7], [12], [13] and the leakage inductance losses problem can be alleviated by using a near unity turn ratio. Furthermore, a lower turn ratio results in a lower cost and a smaller core volume.

Recently, some topologies have been presented that combine the coupled inductor technique with other techniques such as cascading, voltage-lift or/and voltage-multiplier, z-source and multilevel techniques. These combinations result in achieving a high voltage gain with a lower turn ratio, which reduces the leakage inductance losses [14]-[17]. In [18]-[21], a synchronous boost converter, flyback converter and voltage multiplier were combined to provide a high step up non-isolated converter. In [22], the coupled inductor technique was combined with the z-source technique. Although a large conversion ratio was achieved, two large inductor cores were required for a 100W prototype circuit, which impress the efficiency in addition to increasing the circuit volume. The other drawbacks of this converter were the high voltage stress of the diodes and the floating output. This topology was improved in [23] by employing a single larger inductor core. Although, the efficiency is improved it is not acceptable, particularly for larger power applications. In [8], the super-lift (SL) technique was introduced. In this technique, a switch capacitor circuit was employed to increase the output voltage of a conventional boost converter stage by stage. The use of more diodes and capacitors resulted in a larger voltage gain. This technique is not appropriate for high step up applications due to the large number of components required to achieve a tenfold voltage gain. However, it can be a good approach in combination with other techniques. In [18], this technique was combined with the coupled inductor technique to achieve a high voltage gain with a proper number of components. The main drawback of the switch capacitor circuits, such as those used in the super-lift technique, is the inrush current event produced in the capacitor charging/discharging loops. The other disadvantage of this converter is the fact that it requires a relatively high turn ratio to achieve a tenfold voltage gain, which increases the core size and leakage inductance while decreasing the efficiency.

In order to solve inrush current problem of the switch capacitor loops and to achieve a tenfold or more voltage gain with a lower turn ratio, a new high step up converter employing coupled inductors and the super-lift technique is proposed.

The main contributions of this paper are as follows.

1) Achieving a high voltage gain with a low turn ratio and a proper duty cycle, which results in low switch voltage stress and better switch parameters.
2) Low voltage stress of the diodes resulting in diodes with low conduction losses and a much lower reverse recovery time.
3) Alleviation of the reverse recovery problem for all of the diodes.
4) A low inrush current through the switch at the turn on instant while charging voltage lifting capacitors.

This paper is organized as follows. In section II, the operating principle of the proposed convertor is expressed. Section III provides an analysis of the steady-state operation and design guidelines. In section IV, the performance of the proposed converter is compared with previous non-isolated converters. Experimental results obtained with a 200W, 30V input 380V output prototype circuit are discussed in section IV. Finally, some conclusions are presented in section V.

II. Operating Principle of the Proposed Convertor

A schematic of the proposed converter is shown in Fig. 1. This converter consists of one power switch, one coupled inductor, five capacitors and five diodes. The magnetizing inductance L_m, the leakage inductance L_k and an ideal transformer model the coupled inductor. In this converter, the second winding of the coupled inductor is placed in the capacitor charging/discharging loops of the super lift circuit. This modified super-lift module contains the second winding of the coupled inductor. Hence, it creates no inrush current and transfers a high voltage to the output with a proper number of components and a low turn ratio of the coupled inductor.

Since the second winding of the coupled inductor is connected to the drain of the switch, a clamp circuit is required to clamp the off-state voltage of the switch and to reduce the voltage stress of the switch. The clamp circuit is also effective in terms of the voltage gain improvement. A passive clamp circuit is used, which consists of one capacitor C_c and one diode D_c. In order to discharge the clamp capacitor, the charging of the capacitor C_1 in the super-lift stage is down via clamp capacitor discharging while the switch is on. When the switch is in the on-state, D_1 and D_3 are conducting and C_1 and C_3 are charged via C_c and C_2, respectively.

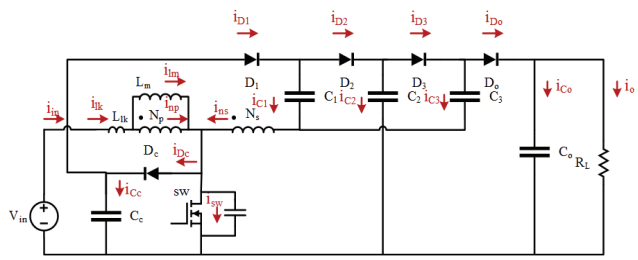


Fig. 1. Schematic of the proposed convertor.

The N_s leakage inductance make a resonance with the capacitors in the charging/discharging loops. Thus, no inrush current is created.

The magnetizing inductance of the coupled inductors is much larger than the leakage inductance. To simplify the analysis, the secondary side leakage inductance is transferred to the primary side and modeled with L_{lk}. When the switch is in the off-state D_2, D_o and D_c conduct. Therefore, the leakage energy and the energy stored in C_1 and C_3 are transferred to C_2 and C_o, respectively. In addition, the clamp capacitor is charged and clamps the stress voltage of the switch to a proper voltage.

To simplify the analysis, the following assumptions are made.

1) The switch is ideal but its parasitic capacitor is considered.
2) The ESR of the capacitors and inductors and the conduction voltage of the diodes and switch are neglected.
3) The magnetizing inductor L_m is large enough to have a constant current during a switching period.
4) The capacitors are large enough to have a constant voltage during a switching period.
5) K and n are the coupling coefficient of the coupled inductor and the turn ratio of the second winding to the primary winding, where: $K \approx L_m/(L_m+L_{lk})$ and $n=N_s/N_p$.

Based on these assumptions, the operation of the proposed convertor in one switching period is divided into five operating modes. These operating modes are determined from the key waveforms of the proposed converter shown in Fig. 2. The equivalent circuit of the proposed convertor in each operating mode is shown in Fig. 3, and the operation in each mode is described as follows.

1) Mode I [t_0, t_1]

During this mode, the switch is on. The diodes D_1 and D_3 are conducting and the other diodes are off. In this mode, the energy is stored in the magnetizing inductor L_m. Simultaneously, the leakage inductance of the second winding L_{lk2} resonates with the series capacitors C_1, C_c and C_3, C_2. Since the resonance frequency is adjusted to be less than the switching frequency, the charging/discharging currents of C_1/C_c and C_3/C_2 are considered to be linear. The voltage across C_1 and C_3 can be derived as:

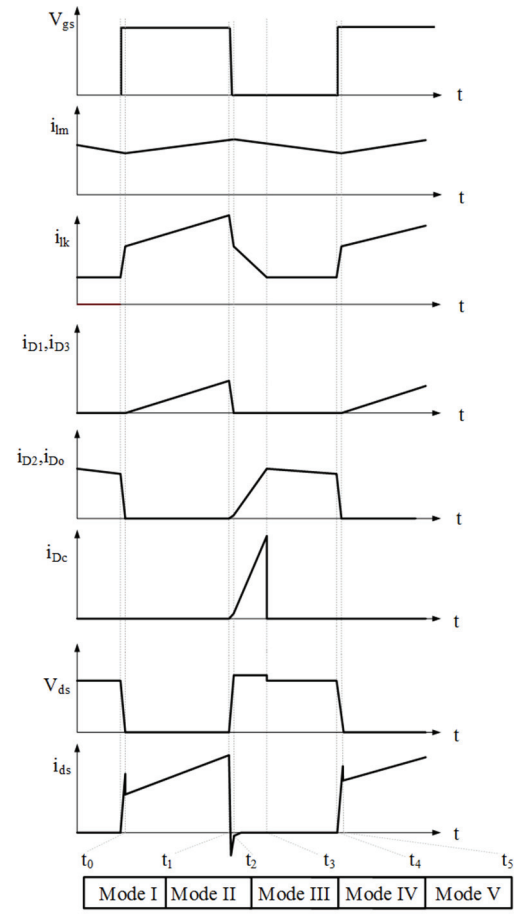


Fig. 2. Typical key waveforms of the proposed convertor.

$$V_{C1} = V_{C_c} + nV_{L_m}{}^{I} \tag{1}$$

$$V_{C3} = V_{C2} + nV_{L_m}{}^{I} \tag{2}$$

During this mode, the voltage across L_m is (V_{C1}-V_{Cc})/n. Therefore, the magnetizing and leakage inductance currents increase linearly as follows:

$$i_{lm}(t) = i_{lm}(t_0) + \frac{V_{C1} - V_{C_c}}{nL_m} \tag{3}$$

$$i_{lk}(t) = i_{lk}(t_0) + \frac{nV_{in} - V_{C1} + V_{C_c}}{nL_{lk}} \tag{4}$$

In this mode, the output capacitor C_o is discharged to the load R_L. At t_1, the switch is turned off and this mode ends.

2) Mode II [t_1, t_2]

In this mode, D_c is conducting and the leakage inductance current is reduced to the magnetizing inductance current. Since the reverse voltage across L_{lk} is very large, this mode duration is very short.

3) Mode III [t_2, t_3]

During this mode, the switch is off. The leakage inductance current becomes less than the magnetizing inductance current and the windings currents increase in the reverse direction.

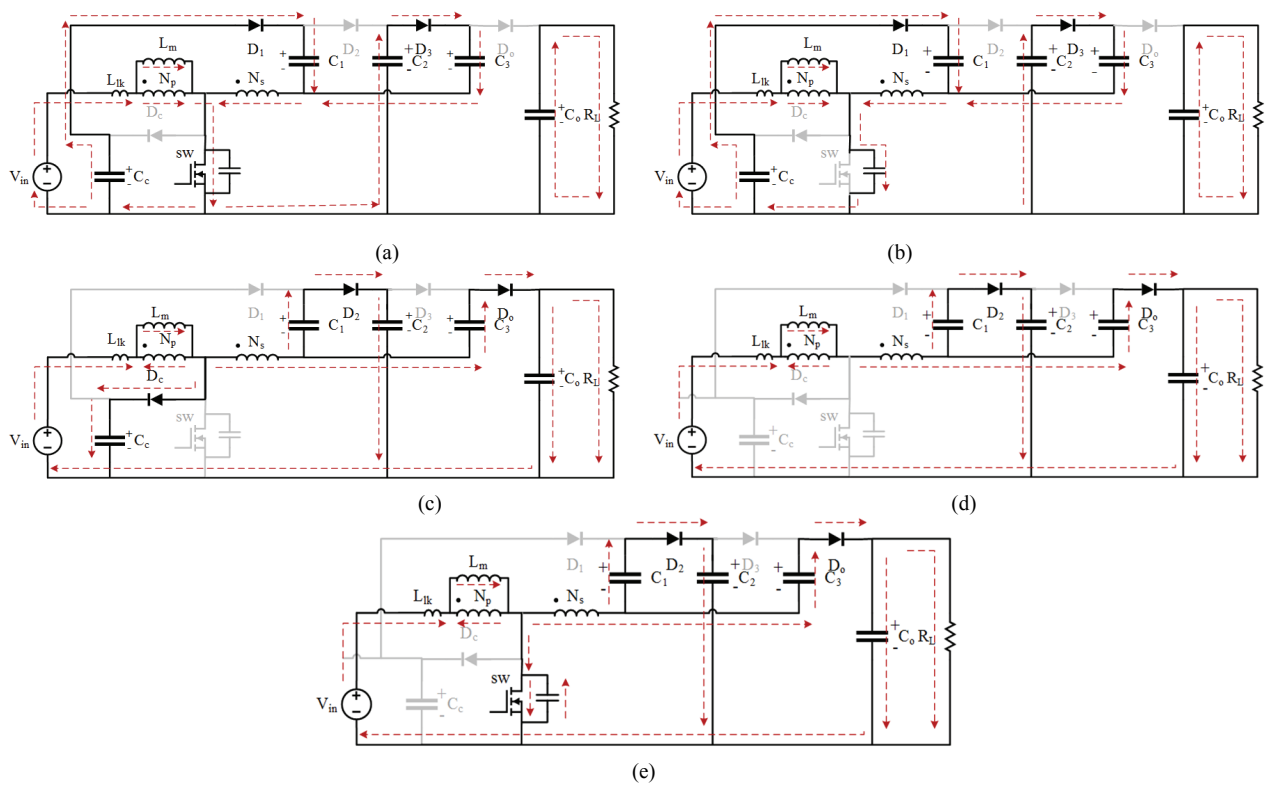


Fig. 3. Equivalent circuits for each of the operating modes. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

Thus, the leakage inductance current decreases. The diodes D_1 and D_3 turn off at zero current and the diodes D_2, D_o and D_c are turned on. In this mode, the clamp capacitor C_c is charged via the leakage inductor of the coupled inductor. Therefore, the current of the clamp diode decreases. In this mode, the currents of the diodes D_2 and D_o increase since these diodes are in series with the second winding of the coupled inductor. The capacitor C_2 is charged via the coupled inductor and C_1. In addition, the input energy is transferred to the output via the coupled inductor and C_3. At t_3, the current of the clamp diode reaches zero. Therefore, D_c is turned off at zero current and this mode ends.

4) Mode IV [t_3, t_4]

During this mode, the switch is off, diode D_c is turned off and the other diodes remain unchanged. In this mode, the leakage inductance current decreases and the currents of the diodes D_2 and D_o increase as before. The capacitor C_2 continues being charged via the coupled inductor and the capacitor C_1. In addition, the input energy continues transferring to the output via the coupled inductor and C_3. The voltage across C_2 and C_o can be derived as:

$$V_{C2} = V_{C_c} + nV_{L_m}{}^{IV} + V_{C1} \tag{5}$$

$$V_{C_o} = V_{C_c} + nV_{L_m}{}^{IV} + V_{C3} \tag{6}$$

During this mode, the voltage across L_m is (V_{C2}- V_{C1}-V_{Cc})/n. Therefore, the magnetizing and leakage inductance currents can be expressed by:

$$i_{lm}(t) = i_{lm}(t_0) + \frac{V_{C2} - V_{C1} - V_{C_c}}{nL_m} \tag{7}$$

$$i_{lk}(t) = i_{lk}(t_0) + \frac{nV_{in} + V_{C2} - V_{C1} - (n+1)V_{C_c}}{nL_{lk}} \tag{8}$$

At t_4, the switch is turned on and this mode ends.

5) Mode V [t_4, t_5]

During this mode, the switch is turned on and the diodes remain unchanged. The leakage inductance current increases and the currents of the diodes D_2 and D_o decrease. The capacitor C_2 continues being charged via the coupled inductor and C_1, and the input energy continues transferring to the output via the coupled inductor and C_3. At t_5, the currents of D_o and D_2 reach zero and this mode ends. Thus, at the end of this mode, the leakage inductance current is equal to the magnetizing inductance current.

III. Steady-State Analysis

A. Voltage Gain Analysis

The CCM operation of the proposed converter is studied here. Modes II, III and V are very short intervals in comparison with modes I and IV. Thus, to simplify the analysis only the two larger intervals, i.e. mode I and IV, are considered. In mode I, when the switch is conducting voltage across the

magnetizing and leakage inductors, they are written as:

$$V_{lm}^{I} = \frac{V_{c1} - V_{C_c}}{n} \tag{9}$$

$$V_{lk}^{I} = V_{in} - \frac{V_{c1} - V_{C_c}}{n} \tag{10}$$

During mode IV, when the switch is in the off-state, the voltage across the magnetizing and leakage inductors are defined by:

$$V_{lm}^{IV} = \frac{V_{c2} - V_{c1} - V_{C_c}}{n} \tag{11}$$

$$V_{lk}^{IV} = V_{C_c} - V_{in} - \frac{V_{c2} - V_{c1} - V_{C_c}}{n} \tag{12}$$

From equations (1)-(9) and (11), the output voltage is obtained as:

$$V_o = 2 \times V_{C_2} - V_{C_c} \tag{13}$$

From the volt-second balance principle for the magnetizing inductor L_m and the leakage inductor L_{lk}, the following equations can be derived as:

$$\int_0^{DT_s} V_{lm}^{I} + \int_{DT_s}^{T_s} V_{lm}^{IV} = 0 \tag{14}$$

$$\int_0^{DT_s} V_{lk}^{I} + \int_{DT_s}^{T_s} V_{lk}^{IV} = 0 \tag{15}$$

From equations (9)-(15) and some simplifications, the voltage across the clamp capacitor is obtained as:

$$V_{C_c} = \frac{V_{in}}{(1-D)} \tag{16}$$

On the other hand, from the ampere-second balance of the capacitors C_1 and C_3 in one switching period, the average current of D_1 and D_3 can be expressed by:

$$< i_{D1} >=< i_{D3} >= \frac{1}{2} < {i_{n2}}^{I} >= I_o \tag{17}$$

According to the key waveforms shown in Fig. 2 and equation (17), the output current I_o is obtained as:

$$I_o = \frac{1}{2} \times \frac{D \times {i_{n2(peak)}}^{I}}{2} \tag{18}$$

where the peak current of the second winding of the coupled inductor $I_{n2\,(peak)}$ can be written as:

$${i_{n2(peak)}}^{I} = \frac{{i_{lk}}^{I} - {i_{lm}}^{I}}{N} = \frac{DT}{n}\left[\frac{1}{l_k}\left(V_{in} - \frac{V_{c1} - V_{C_c}}{n}\right)\right] \tag{19}$$

From equations (16), (18) and (19), the voltage across the capacitor C_1 is achieved as:

$$V_{c1} = -\frac{4n^2 l_k f I_o}{D^2} + \left(n + \frac{1}{1-D}\right) V_{in} \tag{20}$$

From equations (14), (16) and (19), the voltage across the capacitor C_2 can be derived as:

$$V_{c2} = -\frac{4n^2 l_k f I_o}{D^2(1-D)} + \left(\frac{n+2}{1-D}\right) V_{in} \tag{21}$$

Thus, by substituting equation (21) into (13) the output voltage can be computed as:

$$V_o = -\frac{8n^2 l_k f I_o}{D^2(1-D)} + \left(\frac{2n+3}{1-D}\right) V_{in} \tag{22}$$

Thus, the voltage gain can be obtained as:

$$M = \frac{V_o}{V_{in}} = \frac{2n+3}{(1-D)(1+\alpha)} \tag{23}$$

where the coefficient α is related to the leakage inductance of the coupled inductor and is obtained from the following equation:

$$\alpha = \frac{8n^2 l_k f}{D^2(1-D)R_l} \tag{24}$$

By neglecting the leakage inductance, the ideal voltage gain is expressed by:

$$M = \frac{V_o}{V_{in}} = \frac{2n+3}{(1-D)} \tag{25}$$

B. Voltage and Current Stress Analysis

By ignoring the leakage inductance, the voltage stresses of the switch and diodes can be written as:

$$V_{sw} = V_{Dc} = \left(\frac{1}{1-D}\right) V_{in} = \frac{V_o}{2n+3} \tag{26}$$

$$V_{D1} = V_{D2} = V_{D3} = V_{Do} = \left(\frac{n+1}{1-D}\right) V_{in} = \frac{n+1}{2n+3} V_o \tag{27}$$

From the ampere-second balance of the capacitors C_1 and C_3 in one switching period, the average current of D_2 and D_o can be expressed by:

$$< i_{D2} >=< i_{Do} >= \frac{1}{2} < {i_{n2}}^{IV} >= I_o \tag{28}$$

According to the key waveforms of Fig. 2 and equation (28), the output current I_o is obtained as:

$$I_o = \frac{(1-D) \times {i_{n2(peak)}}^{IV}}{2} \tag{29}$$

According to (17), (18), (28) and (29), the peak currents of the power devices can be derived as:

$$i_{D1(peak)} = i_{D3(peak)} = \frac{2I_o}{D} \tag{30}$$

$$i_{D2(peak)} = i_{Do(peak)} = \frac{I_o}{(1-D)} \tag{31}$$

$$\begin{aligned} i_{sw(peak)} &= i_{lm} + {i_{n1(peak)}}^{I} + {i_{n2(peak)}}^{I} \\ &= i_{lm} + \frac{4(n+1)I_o}{D} \end{aligned} \tag{32}$$

By ignoring the ripple of i_{lm}, the average of the magnetizing inductor I_{lm} can be expressed by:

$$i_{lm} = I_{lm} = I_{in} = \frac{2(n+1)I_o}{(1-D)} = \frac{2(n+1)V_o}{(1-D)R_l} \quad (33)$$

By substituting (33) into (32) and some simplification, the peak current of the switch is obtained as:

$$i_{sw(peak)} = \frac{2(n+1)(2-D)I_o}{D(1-D)} \quad (34)$$

C. Design Procedure of the Converter Elements

To assure the CCM operation of the proposed converter, the average current of the magnetizing inductor should be more than half of its ripple. This means that:

$$I_{lm} = I_{in} > \frac{\Delta i_{lm}}{2} \quad (35)$$

The ripple of the magnetizing inductance current (Δi_{lm}) can be expressed as:

$$\Delta i_{lm} = \frac{DV_{in}}{l_m f} \quad (36)$$

Thus, the minimum value of the magnetizing inductor can be computed from equations (25), (33), (35) and (36) as follows:

$$l_m \geq \frac{D(1-D)^2 R_{l(BCM)}}{4(n+1)(2n+3)f} \quad (37)$$

where $R_{L\,(BCM)}$ is the load resistance in the boundary condition mode (BCM) operation.

Equation (38) expresses the voltage ripple equation of the capacitor, which is used to design the capacitor volume.

$$C.\Delta V_c \geq \Delta Q = I_c.\Delta t \quad (38)$$

From (38) the capacitors volumes are computed as:

$$C_o \geq \frac{DV_o}{R_l f \Delta V_o} \quad (39)$$

$$C_1 = C_2 = C_3 = C_c \geq \frac{V_o}{R_l f \Delta V_o} \quad (40)$$

In the proposed converter, each of the capacitors in series with another one resonates with the leakage inductance. In order to reduce the inrush current, this resonant period must be larger than the switching period as per the following equation:

$$2\pi\sqrt{\frac{C_i C_j}{C_i + C_j} l_k} > T \quad (41)$$

where $C_i=\{C_1, C_3\}$ and $C_j=\{C_c, C_2, C_o\}$.

Therefore, the proper value of the capacitors should provide the terms of equations (40) and (41)

A clamp capacitor is designed to limit the voltage spike of the switch. To achieve this, the resonant period between the clamp capacitor and the leakage inductance should be much greater than the minimum off-time of the switch as per the following equation:

$$0.5 \times 2\pi\sqrt{C_c l_k} \geq (1-D)T \quad (42)$$

Hence:

$$C_c \geq \frac{(1-D)^2}{\pi^2 f^2 l_k} \quad (43)$$

The clamp capacitor value should be designed according to both of the conditions assigned in equations (40) and (43).

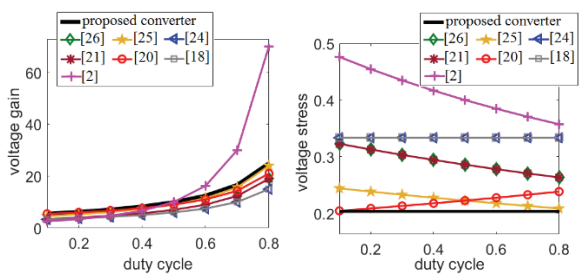
IV. Performance Comparison

The performance of the proposed converter is compared with that of other recent non-isolated single switch topologies [2], [18], [20], [21], [24]-[26] in terms of voltage gain, voltage stress on power devices, component count and efficiency. This comparison is summarized in Table I. The mentioned efficiency is obtained from PSpice simulation results at the same conversion ratio, the same output power and with the same components. The switch voltage stress for all of these converters are more than 100V. Thus, an IRFP250N is employed. However, since the voltage stress of the proposed converter is lower than 100V, an IRFP150N is used. For diodes with low voltage and current stresses, the BYV28-200 is employed; and for diodes with large current and voltage stresses MURXXX series diodes are used. These components are chosen according to PSpice library availability. The efficiency comparison indicates that the proposed converter has a better efficiency, which is due to the low voltage stress of the switches and diode.

In Fig. 4, the voltage gain and voltage stress variations of the proposed converter versus the duty cycle at a specified turn ratio ($n=1$) are compared with [2], [18], [20], [21], [24]-[26] under CCM operation. As can be observed, the proposed converter achieves lower voltage stress in comparison with these topologies. Although, for $D>0.5$, [2] has a larger voltage gain than the proposed converter, its switch voltage stress is higher according to Fig. 4 (b), which decreases its efficiency due to higher conduction losses of the high voltage switches. In addition, the voltage gain and voltage stress of the switch versus the turn ratio at a specified duty cycle ($D=0.6$) is compared with its counterparts [2], [18], [20], [21], [24]-[26] in Fig. 5. The proposed converter has better performance for $n<2.5$ in comparison with [20] and for n<1.67 in comparison with [25]. While for a larger turn ratio, the voltage gains of [20] and [25] are better than those of the proposed converter, a larger turn ratio results in more leakage inductance and parasitic resistance, which results in a lower efficiency. In addition, for all values of the turn ratio, the proposed converter has better performance than [18], [21], [24], and

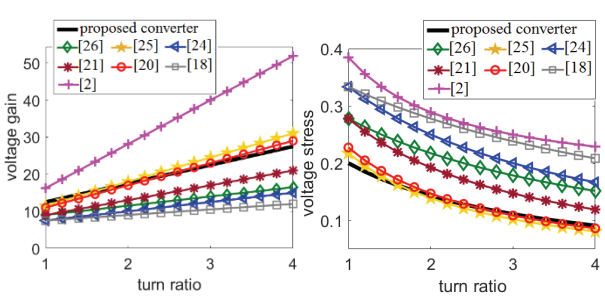
TABLE I
COMPARISON OF THE PROPOSED CONVERTER WITH PERVIOUS NON-ISOLATED CONVERTERS

Non-isolated topologies	[2]	[18]	[20]	[21]	[24]	[25]	[26]	Proposed convertor
Voltage gain	$\frac{n(3D+2)+(2-D)}{2(1-D)^2}$	$\frac{3+nD-D}{1-D}$	$\frac{2+3n-nD}{1-D}$	$\frac{2+n+nD}{1-D}$	$\frac{2+n}{1-D}$	$\frac{2+2n+nD}{1-D}$	$\frac{2+n+D}{1-D}$	$\frac{3+2n}{1-D}$
Voltage stress on switch	$\frac{[2+D(n-1)]V_o}{n(3D+2)+(2-D)}$	$\frac{V_o}{3+nD-D}$	$\frac{V_o}{2+3n-nD}$	$\frac{V_o}{2+n+nD}$	$\frac{V_o}{2+n}$	$\frac{V_o}{2+2n+2D}$	$\frac{V_o}{2+n+D}$	$\frac{V_o}{3+2n}$
Maximum Voltage stress on diodes	$\frac{(2n)V_o}{n(3D+2)+(2-D)}$	$\frac{(n+1)V_o}{3+nD-D}$	$\frac{(n+1)V_o}{2+3n-nD}$	$\frac{(n+1)V_o}{2+n+nD}$	$\frac{(n+1)V_o}{2+n}$	$\frac{(n+1)V_o}{2+2n+2D}$	$\frac{(n+1)V_o}{2+n+D}$	$\frac{(n+1)V_o}{3+2n}$
Switches	1	1	1	1	1	1	1	1
Diodes	6	4	5	4	3	6	4	5
Capacitors	5	4	5	4	4	6	5	5
Core	2	1	1	1	2	1	2	1
Efficiency (%) P_{OUT}=200W	90.67	93.6	91.84	92.23	94.7	91.98	94.66	95.2



(a) (b)

Fig. 4. Comparison of the voltage gain and voltage stress on a switch versus duty cycle variations for n=1. (a) Voltage gain. (b) Voltage stress of a switch normalized by the output voltage (V_s/V_o).



(a) (b)

Fig. 5. Comparison of the voltage gain and voltage stress on a switch versus turn ratio variations for D=0.6. (a) Voltage gain. (b) Voltage stress of a switch normalized by output voltage (V_s/V_o).

[26]. Although, for all turn ratios, [2] has a larger voltage gain than the proposed converter, its voltage stress is very high according to Fig. 5(b), which decrease its efficiency. However, the proposed converter can achieve a high voltage gain without a large duty cycle and a turn ratio that results in a reduction of the magnetic component size, current stress of the switch, input current ripple and conduction losses.

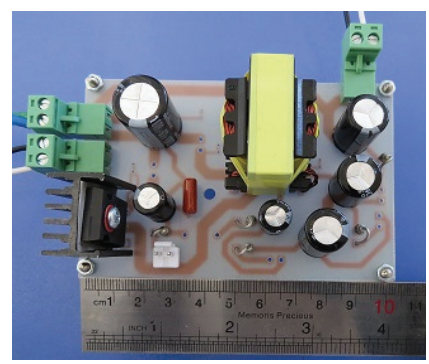


Fig. 6. Photograph of the laboratory prototype converter.

TABLE II
CHARACTERISTICS OF THE LABORATORY PROTOTYPE CIRCUIT

Symbol	Parameter	Value
V_{in}	Input DC voltage	30V
V_{out}	Output DC voltage	380V
P_o	Maximum output power	200W
f_{sw}	Switching frequency	100kHz
C_o	Output capacitor	22μF/450V
C_c,C_1	Clamp capacitor	22μF/160V
C_2-C_3	Capacitors	22μF/400V
D_C, D_1-D_3, D_o	Diodes	BYV28-200
SW	Power switch	IRFP150
---	Magnetizing core	EI33/29
N_s/N_p	Turn ratio	1
L_m	Magnetizing inductance	108μH
K	Coupling coefficient	0.97

V. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis of the proposed convertor, a 30V to 380V, 200 W laboratory prototype circuit has been implemented and tested. A photograph of the

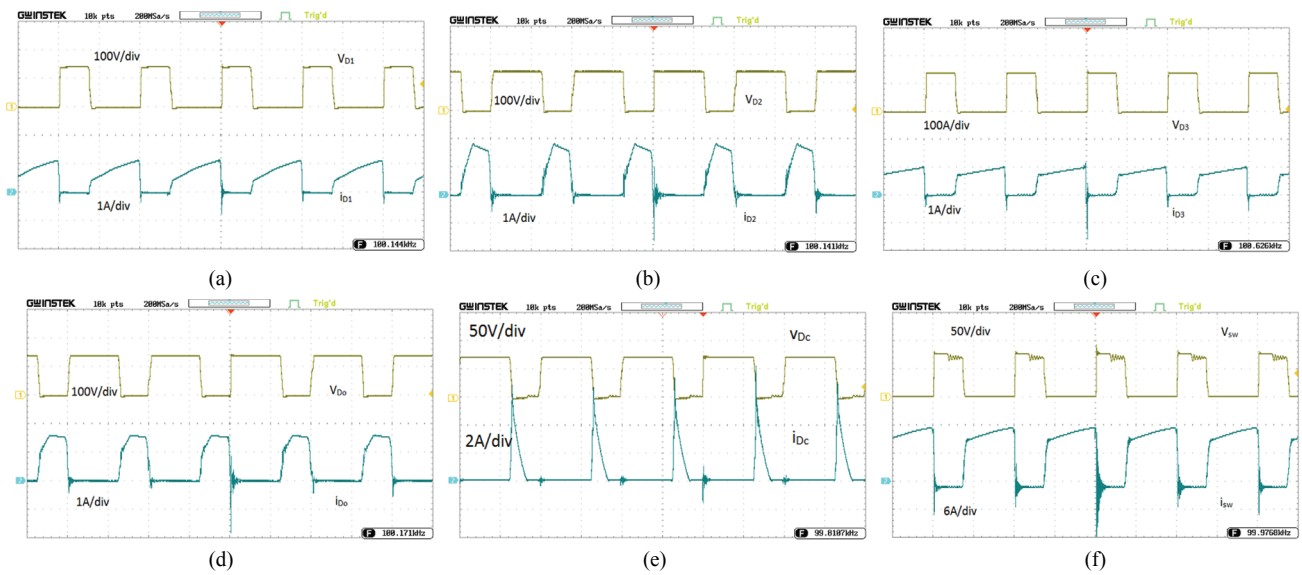


Fig. 7. Experimental voltage and current waveforms. (a) Diode D1. (b) Diode D2. (c) Diode D3. (d) Output diode D_O. (e) Clamp diode D_C. (f) Switch.

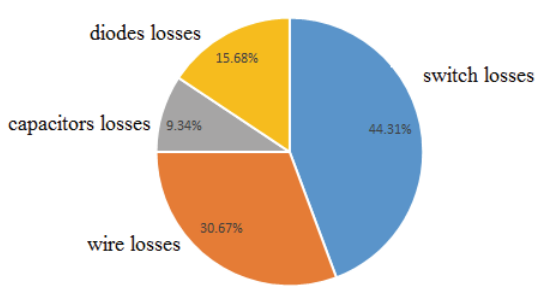


Fig. 8. Pie graph of a loss breakdown at the rated power.

experimental circuit is shown in Fig. 6. This circuit is designed for a proper value of the duty cycle and a low turn ratio. Thus, the duty cycle and turn ratio are adjusted to about $D=0.6$ and $n=1$, respectively. The minimum magnetizing inductor can be calculated from (37). According to this, the proper value of the magnetizing inductor is chosen to be $100\mu H$. In order to find proper values for the capacitors, the voltage ripple of the output capacitor and the others are considered to be *0.1%* and *1-2%* of their average voltages, respectively. According to (39) and (40), the minimum value of the output capacitor and the others are computed to be $8.5\mu F$ and $1.4\mu F$, respectively. In order to have a low ESR effect, equal diode current stresses and to satisfy equations (41)-(43) the values for all of the capacitors are chosen to be $22\mu F$. The characteristics of the laboratory prototype circuit are given in Table II. Experimental results of the implemented circuit under a full load, input voltage $V_{IN}=30V$, output power $P_O=200W$ and load resistance $R_L=720\Omega$, are shown in Fig. 7. The voltage and currents waveforms for all of the diodes and switches are illustrated in Fig. 7(a)-(f). As can be seen, the voltage stress of the diodes $D_{1\text{-}3}$ and D_o are equal and matched with equation (27). The leakage inductance of the coupled inductor alleviates the reverse recovery problem of the diodes. The clamp circuit limits the voltage stress of the power switch to about 80V, which is equal to the expected value from equation (26). Thus, a low on-resistance low voltage *MOSFET* is chosen.

TABLE IIII
ESTIMATED EFFICIENCY AND LOSS DISTRIBUTIONS

Type	$r_{parasitic}$ (mΩ)	$I_{rms}/I_{ave}/I_{max}$ * (A)	V_F/V_{max} + (V)	P_{Loss} (W)	P_{loss} ratio (%)
S (conduction loss)	30	8.35	-	2.1	14.31
S (switching loss)	-	11	80	4.4	30
Coupled inductor	80	7.5	-	4.5	30.67
$C_{1\text{-}3}$	200	1.12	-	3*0.25	5.11
C_c	200	0.72	-	0.1	0.68
C_o	200	1.62	-	0.52	3.55
D_c, $D_{1\text{-}3}$ and D_o	-	0.52	0.89	5*0.46	15.68
total	-	-	-	14.67	100

*I_{rms} for conduction losses, capacitors and coupled inductor losses, I_{ave} for diodes and I_{max} for switching losses
+V_F for diodes and V_{max} for switching losses

A power loss breakdown analysis at the rated current considering the nominal specifications and selected components is given in Table III and Fig. 8. In this estimation, both the conduction losses and switching losses are calculated for the active switch while only the conduction losses and copper losses were considered for the diodes and the coupled inductor respectively. According to the estimated values, the switch losses have the most significant impact on the converter efficiency. The measured converter efficiency at the rated power is about 92.77%, while its theoretical value from Table III is 93.16%.

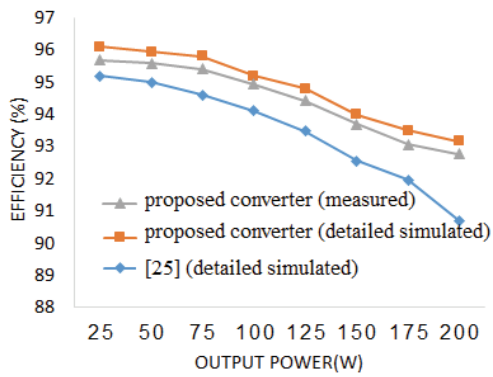


Fig. 9. Efficiency curve of the proposed converter under different loads.

Fig. 9 demonstrates the efficiency of the proposed convertor, which is calculated by measuring the input and output average powers at different loads. As can be observed, the maximum efficiency yields around 95.7% at P_o=25W. Further, under the full load condition i.e. P_o= *200W*, V_{IN}=*30V* and R_L=*720Ω*, the efficiency is about 92.77%. A detailed PSPICE simulation considering the parasitic resistances for all of the elements and ignoring the core loss and PCB track losses is used to compare the efficiency of the proposed converter with that of the converter proposed in [25]. The results of this comparison are shown in Fig. 9. As can be seen, the detailed simulated efficiency of the proposed converter under different loads is near to those achieved by measurements.

VI. Conclusion

In this paper, a new dc/dc high step up converter was introduced. A high voltage gain has been achieved by combining the coupled inductor technique with the super-lift technique. This converter employs a passive clamp circuit to recycle the energy stored in the leakage inductance. In this topology, a high voltage gain with a proper duty cycle and a low turn ratio is achievable. In addition, the voltage stress on the semiconductor devices has been reduced. A small volume, reduced reverse recovery and conduction losses, high efficiency and low cost are other advantages of the proposed convertor. A laboratory prototype circuit verified the theoretical analysis.

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