

High-Reliability Three-Phase Dual-Buck Grid-Connected Inverter without Shoot-Through Problem

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Abstract

When compared to traditional bridge-type inverters, the dual-buck inverter has a higher reliability due to the fact that its bridge legs do not have a shoot-through problem. In this paper, the working principle of the dual-buck inverter is analyzed. A comparison of the working modes under full-cycle and half-cycle control is discussed. With half-cycle control, the inverter can realize a higher efficiency. However, this results in current zero-crossing distortion. The corresponding control strategy of the dual-buck inverter is proposed in order to realize both high efficiency and low current harmonic distortion. In addition, the system stability is analyzed. Dead-time is unnecessary due to the advantages of the topology. Thus, the current harmonic distortion can be further reduced. An inverter with the proposed control strategy has the advantages of high reliability, high efficiency and low current harmonic distortion. Finally, simulation and experimental results are given to verify the theoretical analysis.

Key words: Dual-buck inverter, Dead-time, Half-cycle control, Shoot-through problem, System stability

I. INTRODUCTION

Three-phase grid-connected inverters are widely used in the fields of distributed generation, electric vehicles and so on [1]-[3]. The dual-buck topology can be applied in three-phase grid-connected inverters. When compared to the traditional bridge-type topology, the dual-buck topology has obvious advantages [4]-[6]. For example, the reverse recovery loss of the freewheeling diode is slight. As a result, the efficiency can be improved. There is no shoot-through problem of the bridge legs. Dead-time which can reduce the current Total Harmonic Distortion (THD) does not need to be added to the driving signals. Thus, the filter specifications, especially the LCL filter

specification, can be reduced [7], [8]. Dead-time results in mostly low frequency harmonics [9]. The inhibition effect of the LCL filter on low-frequency harmonics is only equivalent to the L filter [10]. Without dead-time, the LCL filter specification can be greatly reduced.

Due to the above advantages, research on the principle and control strategy of three-phase dual-buck inverters is of great significance. In [11], a three-phase dual-buck inverter controlled by SVPWM has been introduced. SVPWM control is equivalent to third-time harmonic injection SPWM control, which can realize high DC voltage utilization. In [12], a three-phase dual-buck inverter is regarded as three independent single-phase dual-buck inverters. The three single-phase inverters are separately controlled and do not interact with each other. However, the filters are difficult to design. In [13], a vector mode single-cycle control strategy of a dual-buck inverter is proposed. Like the SVPWM control, the three-phase AC voltages are divided into six sectors. However, single-cycle control models for each of the sectors should be established, which complicates the control strategy.

Manuscript received May 17, 2018; accepted Dec. 13, 2018
Recommended for publication by Associate Editor Hao Ma.

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Dual-buck inverters can work in models with and without bias current, which corresponds to full-cycle and half-cycle control respectively. In [14], two kinds of control methods are briefly introduced. The conclusions shows that half-cycle control can realize a higher efficiency than full-cycle control. Under full-cycle control, the two buck converters of each bridge leg work simultaneously. The inductor currents of each buck converter are always continuous. Thus, bias current occurs. Under half-cycle control, the two buck converters of each bridge leg work alternately. The inductor currents of each buck converter are only maintained for half cycle. There is no bias current. Therefore, a working model without bias current has lower switching and conduction losses than a working model with bias current [15], [16]. However, zero-crossing distortion cannot be avoided under half-cycle control.

In order to solve these problems, this paper studies the principle and control strategy of a three-phase dual-buck grid-connected inverter without dead-time. The working models under full-cycle and half-cycle control are analyzed in detail. A comparison of the working models shows that half-cycle control has obvious advantages. On this basis, a half-cycle control strategy of a dual-buck inverter is proposed. It can effectively inhibit zero-crossing distortion. The control strategy can realize a high-quality grid current and low switching loss. In addition, the stability of the inverter system with an LCL filter is not reduced. In addition, it can greatly reduce the filter specification and result in savings in terms of the size and cost of the system since the topology without a dead-zone can eliminate the low frequency harmonics introduced by dead-time.

The remainder of this paper is organized as follows. Section I introduces the dual-buck topology, and the relationship between the input and output is analyzed. Section II discusses the working principle of the inverter under full-cycle and half-cycle control, and the working modes comparison is analyzed in detail. Section III shows the control strategy, and the inhibition method of the zero-crossing distortion and the system stability are discussed. Finally, a simulation model and a principle prototype of an 18kW three-phase dual-buck grid-connected inverter are built to verify the theoretical analysis.

II. TOPOLOGY OF THE DUAL-BUCK INVERTER

Fig. 1 shows the topology of a dual-buck inverter. Taking phase a as an example, L_{a1} and L_{a2} are the converter-side inductances. Due to of L_{a1} and L_{a2} , the shoot-through problem can be avoided. L_{ag} is the grid-side inductance. L_{a1} , L_{a2} , L_{ag} and C_a form the LCL filter. i_{ar} and i_{ag} are the converter-side and grid-side inductor currents of the LCL filter. U_{DC} is the input voltage. e_a is the grid voltage.

Fig. 2 shows waveforms of u_{AN} , U_{DC} and i_{ag} . u_{AN} can be expressed as:

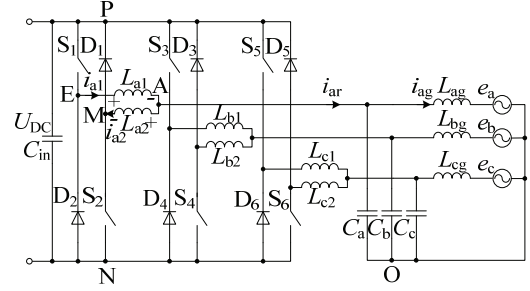


Fig. 1. Topology of a dual-buck inverter.

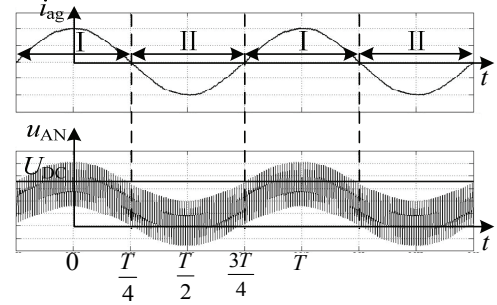


Fig. 2. Waveforms of u_{AN} , U_{DC} and i_{ag} .

TABLE I
RELATIONSHIP BETWEEN u_{AN} AND U_{DC}

switching vector	Mode I		Mode II	
000	$u_{AN} < U_{DC}$	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} < 0$
001	$u_{AN} < U_{DC}$	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} < 0$ ($e_a < U_{DC}/3$)
010	$u_{AN} < U_{DC}$	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} < 0$ ($e_a < U_{DC}/3$)
011	$u_{AN} < U_{DC}$ ($e_a < U_{DC}/3$)	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} > 0$
100	$u_{AN} < U_{DC}$	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} < 0$ ($e_a < U_{DC}/3$)
101	$u_{AN} < U_{DC}$ ($e_a < U_{DC}/3$)	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} > 0$
110	$u_{AN} < U_{DC}$ ($e_a < U_{DC}/3$)	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} > 0$
111	$u_{AN} > U_{DC}$	$u_{AN} > 0$	$u_{AN} < U_{DC}$	$u_{AN} > 0$

$$u_{AN} = u_{AO} + u_{ON} = e_a + L_{ag} \frac{di_{ag}}{dt} + u_{ON} \quad (1)$$

The voltage of L_{ag} is far lower than that of e_a and u_{ON} . Thus, u_{AN} can be approximately expressed as:

$$u_{AN} \approx e_a + u_{ON} \quad (2)$$

The instantaneous value of u_{ON} is related to the switching vectors of the SVPWM modulation. It changes depending on the voltages U_{DC} , $2U_{DC}/3$, $U_{DC}/3$ and 0. According to Fig. 2 and eq. (2), the relationship between u_{AN} and U_{DC} can be obtained, and is shown in Table I.

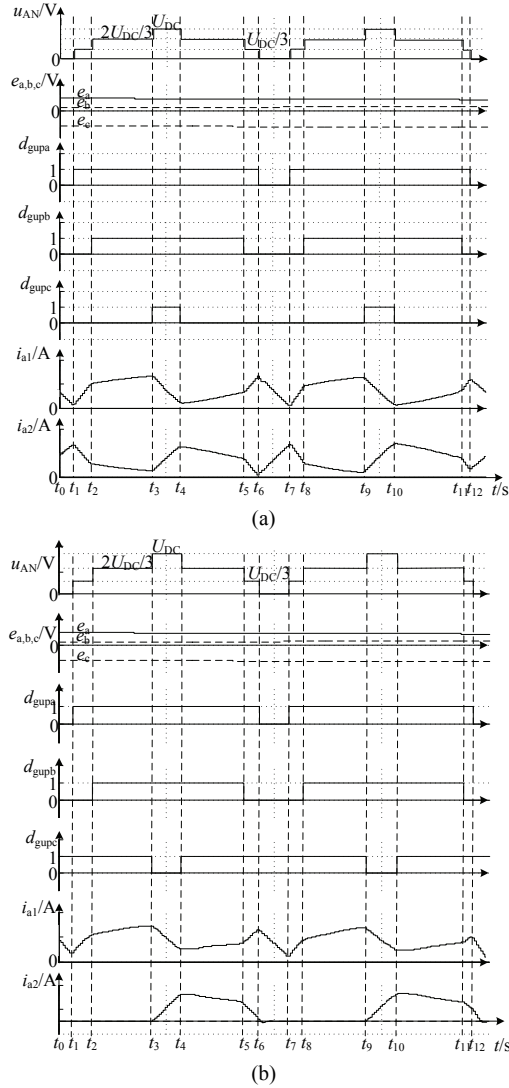


Fig. 3. Key waveforms of full-cycle and half-cycle control in mode I. (a) Full cycle control. (b) Half-cycle control.

In mode I, the polarity of e_a is positive. When the switching vector (111) works, the instantaneous value of u_{AN} is:

$$u_{AN(111)} = e_a + U_{DC} \quad (3)$$

It can be seen that $u_{AN(111)}$ is higher than U_{DC} . When the switching vectors (110), (101) and (011) work, the instantaneous value of u_{AN} is:

$$u_{AN(110)} = u_{AN(101)} = u_{AN(011)} = e_a + 2U_{DC}/3 \quad (4)$$

Under this condition, $u_{AN(110)}$, $u_{AN(101)}$ and $u_{AN(011)}$ are higher than U_{DC} when the instantaneous value of e_a is higher than $U_{DC}/3$. When the switching vectors (100), (010) and (001) work, the instantaneous value of u_{AN} is:

$$u_{AN(100)} = u_{AN(010)} = u_{AN(001)} = e_a + U_{DC}/3 \quad (5)$$

The input voltage is higher than $3e_a$. Thus, $u_{AN(100)}$, $u_{AN(010)}$ and $u_{AN(001)}$ are lower than U_{DC} . When the switching vector (000) works, $u_{AN(000)}$ is e_a , which is also lower than U_{DC} . In mode II, the relationship between u_{AN} and U_{DC} can be obtained

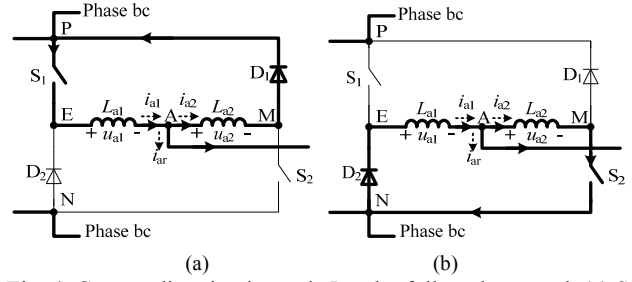


Fig. 4. Current direction in mode I under full-cycle control. (a) S_1 on, S_2 off. (b) S_1 off, S_2 on.

through the same analytical process.

Fig. 3 shows key waveforms of full-cycle and half-cycle control in mode I. The waveforms from top to bottom respectively are u_{AN} , the grid voltages, the three-phase driving signals and the inductance currents. Definitions of full-cycle and half-cycle control are given in [14]. The bridge leg output voltages of the two working models are the same. However, the inductance currents i_{a1} and i_{a2} are different. Therefore, the working modes of the two working models are different.

III. WORKING PRINCIPLE

A. Full-Cycle Working Model

Mode I: In Fig. 3, e_a can be regarded as a constant value in a switching cycle because the switching frequency is much higher than the grid frequency. Taking Sector I as an example, the active switching vectors are (000) (100) (110) and (111). Fig. 4 shows the current direction of phase a in mode I under full-cycle control. From t_1 to t_6 , given in Fig. 3(a), S_1 is on and S_2 is off. The current flows through S_1 , L_{a1} , L_{a2} and D_1 , as shown in Fig. 4(a). From t_6 to t_7 , the current flows through S_2 , L_{a1} , L_{a2} and D_2 , as shown in Fig. 4(b).

t_1 - t_2 : The active switching vector is (100). According to Table I, u_{AN} is lower than U_{DC} , and the potential of point A is lower than that of point P. i_{a1} increases and i_{a2} decreases.

t_2 - t_3 : The active switching vector is (110). In Sector I, e_a is lower than $U_{DC}/3$. According to Table I, u_{AN} is lower than U_{DC} , i_{a1} increases and i_{a2} decreases. When compared to the period from t_1 to t_2 , the potential difference of point A and point P during t_2 to t_3 is lower. Therefore, the slope of the current during t_2 to t_3 is lower than that during t_1 to t_2 .

t_3 - t_4 : The active switching vector is (111). u_{AN} is higher than U_{DC} . i_{a1} decreases and i_{a2} increases.

t_4 - t_5 : The working principle is similar to that of t_2 - t_3 .

t_5 - t_6 : The working principle is similar to that of t_1 - t_2 .

t_6 - t_7 : The active switching vector is (000). u_{AN} is higher than 0, and the potential of point A is higher than that of point N. i_{a1} decreases and i_{a2} increases.

Mode II: The analysis process is similar to that of Mode I. The difference is that the direction of i_{ar} is opposite.

It can be seen that the currents of L_{a1} and L_{a2} always exist under

full-cycle control. Under ideal conditions, the relationship between u_{a1} and u_{a2} is:

$$u_{a1} + u_{a2} = 0 \quad (6)$$

The relationship between i_{a1} and i_{a2} is:

$$i_{a1} - i_{a2} = i_{ar} \quad (7)$$

According to Fig. 2, u_{AN} is always higher than 0 in Mode I, which means that i_{a1} decreases and i_{a2} increases when S_2 turns on. According to (7), i_{ar} decreases. u_{AN} is always lower than U_{DC} in Mode II. i_{a1} increases and i_{a2} decreases when S_1 turns on. In addition, i_{ar} increases. It can be seen that under full-cycle control, L_{a1} and L_{a2} work in parallel. Assuming that $L_{a1}=L_{a2}=L_r$, the inverter-side equivalent inductor of the LCL filter L_{ar} can be expressed as:

$$L_{ar} = \frac{L_{a1}}{2} = \frac{L_{a2}}{2} = \frac{L_r}{2} \quad (8)$$

B. Half-Cycle Working Model

Mode I: As shown in Fig. 3(b), e_a and e_b are positive. The driving signals of the lower leg switches of the two phases are forced to be low. In addition, e_c is negative. The upper leg switch driving signal of phase c is forced to be low.

Fig. 5 shows the current direction of phase a in mode I under half-cycle control. The branch of S_2 does not conduct because its driving signal is forced to be low. L_{a2} and D_1 form a branch where the current path is unidirectional.

Fig. 5(a) corresponds to the switching states during t_1 to t_3 . L_{a1} works separately. The value of the inverter-side equivalent inductor of the LCL filter is L_r . Fig. 5(b) corresponds to the switching states during t_3 to t_6 . In addition, L_{a1} and L_{a2} work in parallel, and the inverter-side equivalent inductor L_{ar} is $L_r/2$. Fig. 5(c) corresponds to the switching states before i_{a2} decreases to 0 during t_6 to t_7 . In addition, L_{a1} and L_{a2} work in parallel. Fig. 5(d) corresponds to the switching states after i_{a2} decreases to 0 during t_6 to t_7 . Furthermore, L_{a1} works separately.

t_1 - t_2 : The active switching vector is (100). u_{AN} is lower than U_{DC} , and i_{a1} increases. Before t_1 , i_{a2} is 0. Therefore, D_1 does not freewheel during t_1 to t_2 . D_1 is kept off and i_{a2} is still 0.

t_2 - t_3 : The active switching vector is (110). i_{a1} increases and i_{a2} is still 0.

t_3 - t_4 : The active switching vector is (111). u_{AN} is higher than U_{DC} , and i_{a1} decreases. Since the potential of point A is higher than that of point P, D_1 turns on, and i_{a2} starts to rise from 0.

t_4 - t_5 : Unlike t_2 - t_3 , i_{a2} not 0 before t_4 . D_1 freewheels and i_{a2} decreases.

t_5 - t_6 : Unlike t_1 - t_2 , D_1 freewheels. i_{a1} increases and i_{a2} decreases.

t_6 - t_7 : The active switching vector is (000). u_{AN} is higher than 0, and i_{a1} decreases. Because S_2 is kept off, D_1 does not stop freewheeling until i_{a2} decreases to 0.

Mode II: The analysis process is similar to that of Mode I. When L_{a2} works separately, L_{ar} is L_r . When L_{a1} and L_{a2} work in parallel, L_{ar} is $L_r/2$.

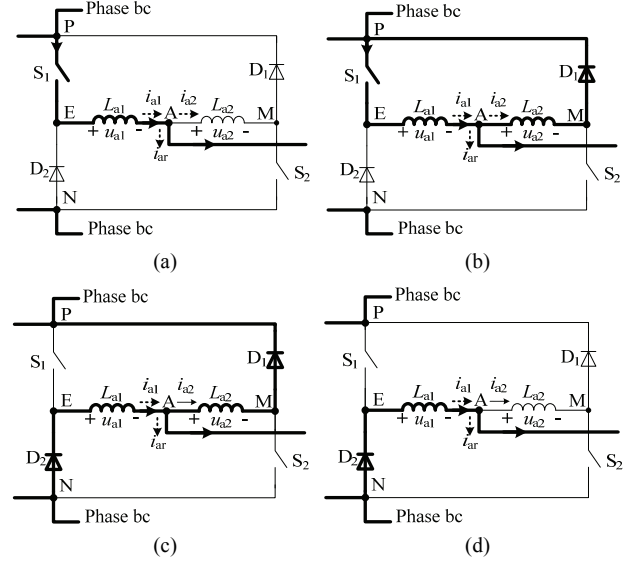


Fig. 5. Current direction in mode I under half-cycle control. (a) S_1 on, S_2 off, D_1 off. (b) S_1 on, S_2 off, D_1 on. (c) S_1 off, S_2 off, D_1 on. (d) S_1 off, S_2 off, D_1 off.

According to a comparison analysis, L_{ar} is always $L_r/2$ under full-cycle control. Under half-cycle control, L_{ar} is L_r , when L_{a1} or L_{a2} works separately. The grid current harmonic can be expressed as:

$$I_{gh} = \left| \frac{U_{oh} k_h^2}{2\omega_h [L_{ar}(k_h^2 - 1) + L_g(k_h^2 - 1)]} \right| \quad (9)$$

where U_{oh} is the output voltage harmonic of the bridge leg. In addition, k_h can be expressed as:

$$k_h = \frac{f_{res}}{h f_1} \quad (10)$$

where f_{res} is the resonant frequency of the LCL filter [17]. In addition, f_1 is the grid frequency. According to (9) and (10), the filtering effect under half-cycle control is better than that under full-cycle control.

In addition, the RMS current of the switches under half-cycle control is lower than that under full-cycle control. The authors of [14] give the conduction, switching and reverse recovery loss expressions of the power switches. It can be seen that the efficiency of half-cycle control is higher.

IV. CONTROL STRATEGY

According to [14], zero-crossing distortion is caused by sudden changes of the ripple current direction. Therefore, the current ripples of L_{a1} , L_{a2} , L_{b1} , L_{b2} , L_{c1} and L_{c2} should be inhibited as much as possible. Taking phase a as an example, when i_a is changed from positive to negative, before the zero-crossing point, the increment of i_{a1} should be reduced when S_1 is turned on, which means reducing u_{PA} . In addition, u_{PA} can be expressed as:

$$u_{PA} = u_{PN} - u_{AN} \approx U_{DC} - e_a - u_{ON} \quad (11)$$

After the zero-crossing point, the increment of i_{a2} should be reduced when S_2 is turned on, which means reducing u_{AN} . According to (2) and (11), u_{AN} and u_{PA} can be controlled by changing u_{ON} . In addition, u_{ON} can be expressed as:

$$u_{ON} = \frac{u_{AO} + u_{BO} + u_{CO}}{3} \quad (12)$$

where u_{AO} , u_{BO} and u_{CO} are the output voltages of the three-phase bridge legs. They can be controlled by changing the voltage vector references in the control loop.

The essence of zero-crossing inhibition is to increase u_{ON} before the zero-crossing point, and to decrease u_{ON} after the zero-crossing point. When i_a changes from negative to positive, the principle is similar. Therefore, negative feedback of the current ripple method can be introduced to inhibit zero-crossing distortion. Fig. 6 shows the proposed control strategy. A high-pass filter (HPF) is introduced to extract the current ripple [18], [19]. The SVPWM driving signals are forced to be low during the corresponding half cycle.

When i_a changes from positive to negative, the ripple of i_{a1} is positive before the zero-crossing point. After the negative feedbacks are added to u_α and u_β , the references that take part in the SVPWM decrease. That is to say, u_{AO} , u_{BO} and u_{CO} decrease. As a result, u_{ON} decreases, and according to equation (2), u_{AN} decreases. Thus, i_{a1} decreases. After the zero-crossing point, according to eq. (11), u_{PA} decreases. As a result, the current near the zero-crossing point is close to 0 and zero-crossing distortion can be inhibited.

The transfer function of the HPF can be expressed as:

$$G_{HPF}(s) = \frac{H_0 s^2}{s^2 + \alpha \omega_0 s + \omega_0^2} \quad (13)$$

where H_0 is the transmission gain. In addition, α is the damping coefficient, and ω_0 is the cut-off angular frequency. In order to detect the whole process of zero-crossing distortion, the cut-off frequency should be low. The grid frequency is 50Hz. Thus, the cut-off frequency is set as 150Hz. Because the proportional coefficient k_1 already exists, H_0 can be set as 1.

It can be seen that a HPF is added after current sampling. When compared to the traditional SVPWM strategy, the proposed strategy does not need additional sensors or sampling. The second-order HPF described in (13) has good performance and is easy to realize in digital control systems.

According to Fig. 6, a system block diagram can be obtained, as shown in Fig. 7. The closed-loop transfer function can be expressed as:

$$\frac{I_g(s)}{ERR(s)} = \frac{G_{PI}(s)G_{INV}(s)G_2(s)}{1+G_1(s)G_2(s)} \quad (14)$$

where $G_{INV}(s)$ is the transfer function of the inverter. It is a proportion-delay link [20]. $G_1(s)$ and $G_2(s)$ can be expressed as follows:

$$\begin{cases} G_1(s) = \frac{1+sCR}{(sL_r+R_r)(sL_g+R_g)sC} \\ G_2(s) = G_1(s) + k_1 G_{HPF}(s) G_{INV}(s) \end{cases} \quad (15)$$

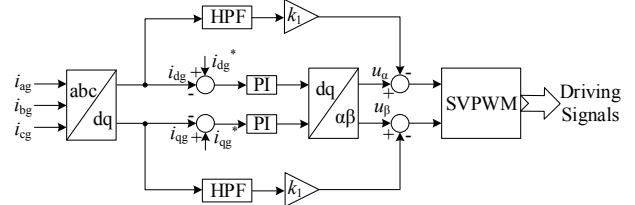


Fig. 6. Control strategy of a three-phase dual-buck inverter.

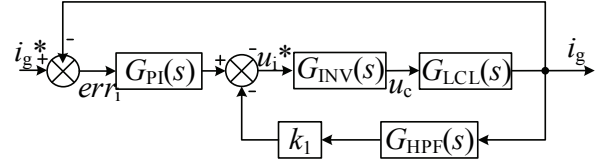


Fig. 7. System block diagram.

where C is the filtering capacitor, and R is the damping resistor. R_r and R_g are the parasitic resistors of L_r and L_g .

In this paper, LCL filter capacitor current negative feedback has been added [21]. The closed-loop transfer function can be expressed as:

$$\frac{I_g(s)}{ERR(s)} = \frac{G_{PI}(s)G_{INV}(s)G_3(s)}{1+G_1(s)G_3(s)} \quad (16)$$

where $G_3(s)$ can be expressed as:

$$G_3(s) = G_2(s) + \frac{sC(sL_g+R_g)k_2 G_{INV}(s)}{1+sCR} \quad (17)$$

where k_2 is the coefficient of the current sampling. According to the analysis of [21], the system can realize stability. As a result, the influence of the current ripple negative feedback on system stability can be inhibited.

V. EXPERIMENTAL RESULTS

Based on the above analysis, a simulation model of an 18kW three-phase dual-buck grid-connected inverter based on MATLAB/Simulink has been built. The input voltage is 700V DC. The output is connected to a 220V/380V/50Hz grid. The switching frequency is 5kHz. L_r is 1.6mH, C is 20μF, and L_g is 1.2mH.

Fig. 8 shows the inverter-side inductor currents during the zero-crossing period. The current is i_{a1} , i_{a2} and i_{ar} . In Fig. 8(a), the current ripple before and after the zero-crossing point are obvious. In Fig. 8(b), the proposed control strategy with zero-crossing distortion inhibition has been applied. The current ripple can be effectively inhibited.

Fig. 9 shows the inverter-side inductor currents during 1.5 times the grid cycle. The corresponding grid-side current THD is 10.2% and 3.1%. It can be seen that the control method proposed in this paper can inhibit zero-crossing distortion and obtain higher quality current waveforms.

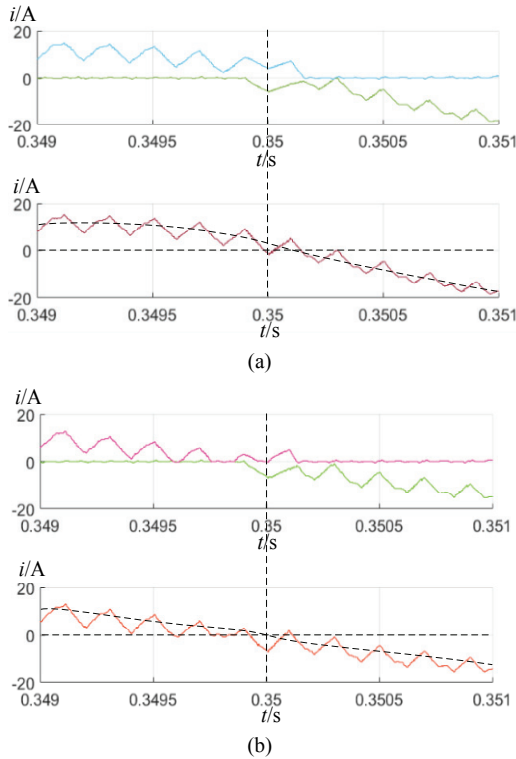


Fig. 8. Inverter-side inductor currents during the zero-crossing period. (a) Half-cycle control without zero-crossing distortion inhibition. (b) Half-cycle control with the proposed control strategy.

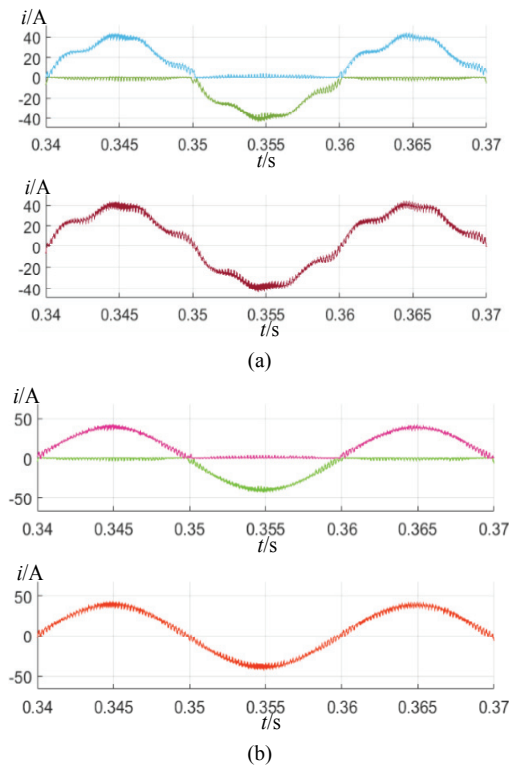


Fig. 9. Inverter-side inductor currents during 1.5 times the grid cycle. (a) Half-cycle control without zero-crossing distortion inhibition. (b) Half-cycle control with the proposed control strategy.

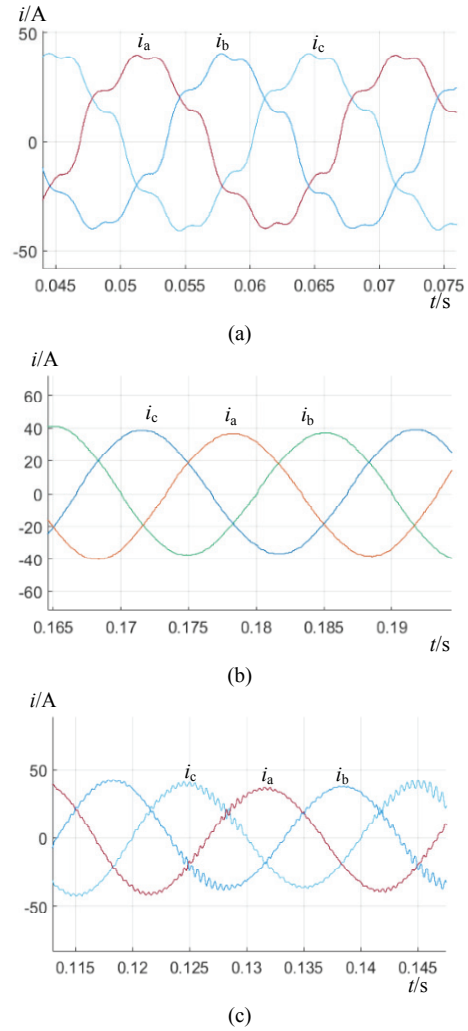


Fig. 10. Grid-side currents. (a) Half-cycle control without zero-crossing distortion inhibition. (b) Half-cycle control with the proposed control strategy. (c) Half-cycle control without active damping.

Fig. 10 shows grid-side inductor currents. Fig. 10(a) and Fig. 10(b) show the grid-side current of Fig. 9(a) and Fig. 9(b), respectively. In Fig. 10(a), half-cycle control leads to zero-crossing distortion. The three-phase currents interact with each other. In Fig. 10(b), zero-crossing distortion has been effectively inhibited. In Fig. 10(c), active damping is not added since it would cause current oscillations. The grid current THD is 5.3%.

A principle prototype has been built to verify the theoretical analysis. The parameters are the same as those of the simulation model.

Fig. 11 shows experimental results of half-cycle control without zero-crossing inhibition. The waveforms in Fig. 11(a) are the grid voltage e_a and the three-phase grid currents i_{ag} , i_{bg} and i_{cg} . The waveforms in Fig. 11(b) are the inverter-side inductor current i_{ar} and the driving signals of phase a. The driving signals are forced to be low during half of the grid cycle. The zero-crossing distortion occurs.

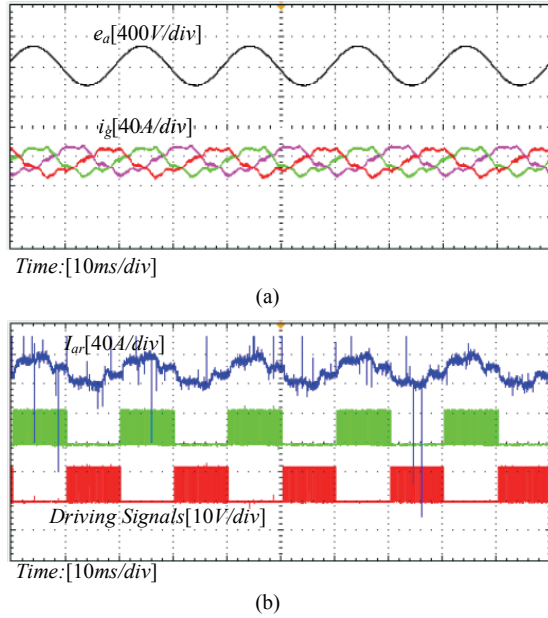


Fig. 11. Experimental results of half-cycle control without zero-crossing inhibition. (a) Grid-side inductor current. (b) Inverter-side inductor current.

TABLE II

THD OF GRID CURRENT WITH DIFFERENT VALUES OF k_1

k_1	0	10	50	100	150
THD	10.7%	9.3%	6.5%	3.2%	3.3%

Table II shows grid current THDs of the proposed control strategy with different values of k_1 . If k_1 is 0, there is no current ripple negative feedback, and zero-crossing distortion occurs, which corresponds to Fig. 11(a). With the increment of k_1 , the current distortion decreases. After k_1 reaches 100, zero-crossing distortion can be basically eliminated.

Fig. 12 shows experimental results with zero-crossing distortion inhibition. k_1 is 100. In Fig. 12(a), active damping is not added. Although zero-crossing distortion can be inhibited, the grid current oscillates at the resonant frequency of the LCL filter. In Fig. 12(b)-(d) and (e), active damping is added. Oscillation disappears and the system stability can be improved. Fig. 12(b) shows the inductor current i_{ar} , i_{a2} and the grid voltage e_a . Fig. 12(c) and 12(d) show the three-phase grid current under full load and half load. It can be seen that the proposed strategy is able to inhibit zero-crossing distortion under different loads. In the no-load condition shown in Fig. 12(e), the current is 0. When compared with Fig. 11, Fig. 12 can inhibit zero-crossing distortion.

Table III shows the grid current THDs of the proposed control strategy with different loads. k_1 is 100. The THD decreases with the increment of the load. According to Fig. 12(c)-(e), under low load conditions, the high THD is not caused by zero-crossing distortion. Because the parameters of the LCL filter are fixed, the filtering affect is weakened under low load conditions.

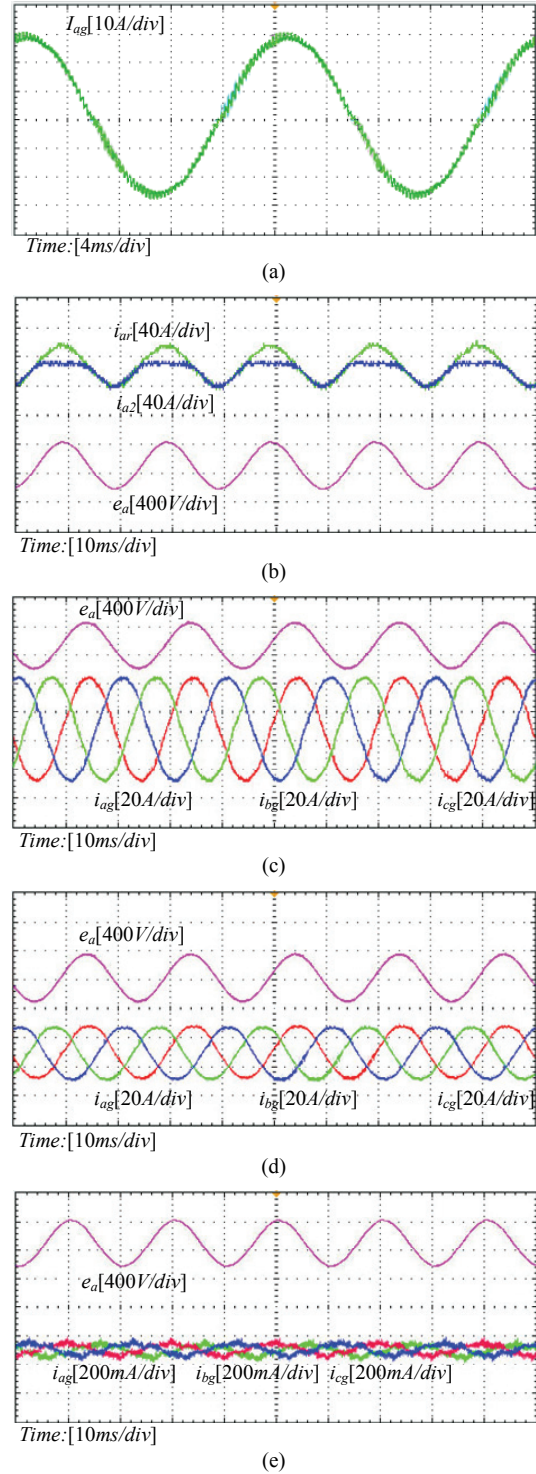


Fig. 12. Experimental results with zero-crossing distortion inhibition. (a) Current oscillation without active damping. (b) inductor current with active damping. (c) Three-phase current under a full load. (d) Three-phase current under a half load. (e) Three-phase current under no load.

TABLE III
THD OF GRID CURRENT WITH DIFFERENT LOADS

Output Power	18kW	9kW	3kW
THD	3.2%	4.8%	19.7%

VI. CONCLUSION

This paper analyzes the working principle of three-phase dual-buck grid-connected inverters. The cause of the zero-crossing distortion of grid current is discussed. The half-cycle SVPWM control strategy with negative current ripple feedback is proposed. Dual-buck inverters do not have a shoot-through problem and the harmonics caused by dead-time can be avoided. However, the current THD cannot be improved unless zero-crossing distortion is eliminated. Zero-crossing distortion inhibition is the premise of a low THD. With the proposed control strategy, the advantages of the dual-buck topology can be realized. The negative current ripple feedback control strategy can change the SVPWM vector reference during the zero-crossing time. Thus, the current ripple and the zero-crossing distortion can be effectively inhibited. As a result, half-cycle control can realize high efficiency and a low THD.

ACKNOWLEDGMENT

The authors would like to acknowledge the support provided by the National Natural Science Foundation (51607052).

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