JPE 19-2-3

https://doi.org/10.6113/JPE.2019.19.2.353
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Zero-Current-Switching in Full-Bridge DC-DC Converters Based on Activity Auxiliary Circuit

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Abstract

To address the problem of circulating current loss in the traditional zero-current switching (ZCS) full-bridge (FB) DC/DC converter, a ZCS FB DC/DC converter topology and modulation strategy is proposed in this paper. The strategy can achieve ZCS turn on and zero-voltage and zero-current switching (ZVZCS) turn off for the primary switches and realize ZVZCS turn on and zero-voltage switching (ZVS) turn off for the auxiliary switches. Moreover, its resonant circuit power is small. Compared with the traditional phase shift full-bridge converter, the new converter decreases circulating current loss and does not increase the current stress of the primary switches and the voltage stress of the rectifier diodes. The diodes turn off naturally when the current decreases to zero. Thus, neither reverse recovery current nor loss on diodes occurs. In this paper, we analyzed the operating principle, steady-state characteristics and soft-switching conditions and range of the converter in detail. A 740 V/1 kW, 100 kHz experimental prototype was established, verifying the effectiveness of the converter through experimental results.

Key words: Circulating current loss, Full-bridge converter, Rectifier diodes, Turn-off losses, Zero-current switching

I. INTRODUCTION

With the advantages of simple topology, easy control, and high efficiency, the full-bridge converter is widely used in high-power applications, such as power supply, renewable energy, and electric vehicle traction systems [1], [2]. Soft-switching technology has the following advantages: improving operating environment and reliability of power switches, reducing power losses and sizes of converters, enhancing efficiency, suppressing the exorbitant dv/dt and di/dt, and cutting down electromagnetic interference (EMI) and system noise effectively [3]-[5].

Traditional phase shift zero-voltage full-bridge DC–DC converters [6], [7] can solve the problem of hard-switching of the primary switch, but the lagging switches are suffering from realizing soft-switching difficultly under the light load condition, thereby limiting the load range of the converter. To solve this problem, various zero-voltage and zero-current switching (ZVZCS) full-bridge converters [8]-[11] based on auxiliary circles were proposed. The leading switch realizes ZVS and the lagging switch realizes ZCS. It widens the soft-switching range and reduces the switching loss of the lagging switch, but the leading switch does not realize the ZCS turn off. The great switching loss in the primary switch still exists.

In order to solve the problem of great switching loss in the primary switch, zero-current switching full-bridge converters have been proposed in [12]-[14]. To achieve ZCS turn off of the primary switch, the auxiliary switch and additional transformer is added to the primary switch in [12]. Unfortunately, the additional transformer increases the magnetic loss and the volume of the converter. In [13], two auxiliary switches are connected in parallel in the secondary to achieve ZCS turn off of the primary switch of the converter. However, ZCS turn off is only achieved under a discontinuous conduction mode, and the auxiliary switches are hard turn off, thereby increasing the total losses of converters. The reference [14] proposed to add an active auxiliary circle in the primary and a passive snubber circuit on the secondary side of the converter, respectively, to achieve the ZCS turn-off of the leading switch and the ZCS turn-off of the lagging switch. Unfortunately, these auxiliary circuits are complex and increase the current and voltage stress of the power switches; moreover, they result in additional circulating current loss.

To solve the aforementioned issues, a ZCS full-bridge DC/DC converter and modulation strategy is proposed in this

Manuscript received Sep. 7, 2018; accepted Dec. 6, 2018
Recommended for publication by Associate Editor Hongfei Wu.
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paper. The converter realizes ZCS turn-on and ZVZCS turn-off of primary switches and achieves ZVZCS turn-on and ZVS turn-off of auxiliary switches. The converter decreases circulating current loss and does not increase the current stress of the primary switches and the voltage stress of the rectifier diodes. The diodes turn off naturally when the current decreases to zero. Thus, no reverse recovery current and loss occurs on diodes. The converter improves the conversion efficiency of high-frequency high-power applications.

This paper analyzed the operating principle, steady-state characteristics, soft-switching conditions, and range, and conducts parameter design and loss analysis of the converter in detail. A 740 V/1 kW, 100 kHz experimental prototype was established, thereby verifying the effectiveness of the converter by experimental results.

II. Circuit Topology and Operation Principle

Fig. 1 shows the proposed ZCS full-bridge converter topology, where V_{in} is the input DC voltage source. Switches S_1–S_4, and antiparallel diodes D_1–D_4 consist of the full bridge inverter structure; L_r is the leakage inductance of T or the summation of the leakage inductance and an external inductance. The auxiliary switches S_5 and S_6 in parallel with the resonant capacitor C_r are connected in series with the secondary circuit. D_5 and D_6 are antiparallel diodes of the switches S_5 and S_6. The diodes D_{R1}–D_{R4} are the secondary output rectifier diodes. T is the high frequency transformer. L_o is the output filter inductance. C_o is the output filter capacitor, and R is the load. i_p is the primary current, i_s is the secondary current, and v_{Cr} is the auxiliary resonant capacitor voltage.

Fig. 2 and Fig. 3 respectively show the working waveforms and operation modes of the proposed converter. In Fig.2, v_{g1}/v_{g4} and v_{g2}/v_{g3} are the driving waveforms of S_1/S_4 and S_2/S_3, respectively. v_{g5} and v_{g6} are the driving waveforms of S_5 and S_6, respectively. S_1/S_2 and S_4/S_3 turn off after S_5/S_6 turn off with off delay time t_δ. t_d is the dead time between S_1 and S_2 as well as S_3 and S_4. T_s is a switching period. t_{on} is the conduction time of the primary switches. D_{in} is the converter input duty cycle expressed as D=t_{on}/T_h, D is the converter output duty cycle expressed as D=$(t_{on}$-$t_\delta)/T_h$, where $T_h = T_s/2$.

To facilitate the analysis, several assumptions are used as follows:

(1) All the switches, diodes, capacitors and inductors are ideal devices.

(2) N_1 and N_2 are the turns of the transformer's primary and secondary, respectively. The transformer turn ratio N_T is N_1/N_2. The roll line resistance of the transformer is neglected.

(3) The output inductance L_o is sufficiently large to keep the filter inductor current i_{Lo} at a constant value I_o during the switching period.

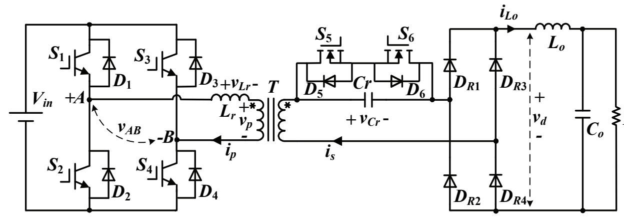


Fig. 1. The proposed ZCS full-bridge converter.

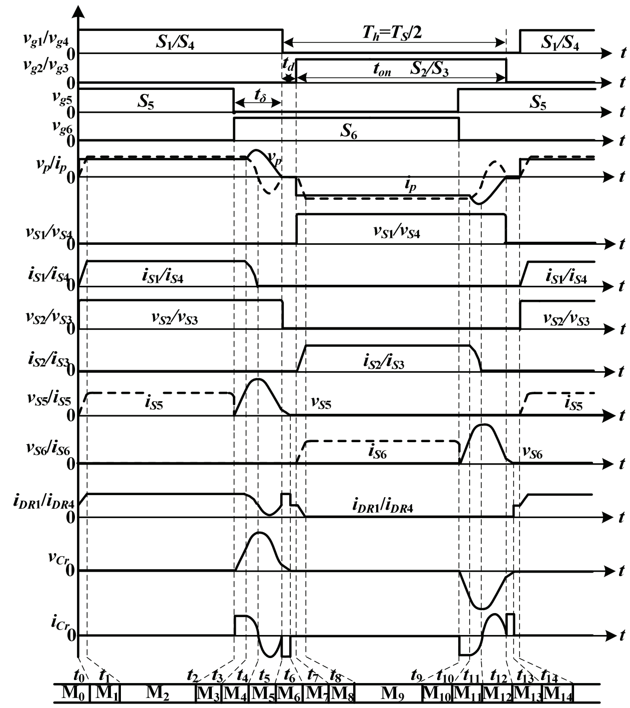


Fig. 2. Working waveforms of the proposed converter.

Mode 0 [$\sim t_0$] [*see Fig*. 3(*a*)]: Prior to t_0, the primary switches S_1–S_4 are off, the auxiliary switch S_6 is off and S_5 is on, the initial voltage of the auxiliary resonant capacitor C_r is v_{Cr}=0. The rectifier diodes D_{R1}–D_{R4} are on. The load current flows through rectifier diodes for freewheeling.

Mode 1 [t_0–t_1] [*see Fig*. 3(*b*)]: At t_0, S_1 and S_4 turn on. i_p and i_s increase linearly. L_r limits the increase rate of i_p; thus, S_1 and S_4 realize ZCS turn on. When i_s increases to I_o, D_{R2}, and D_{R3} turn off, and mode 1 ends.

i_p is described as

$$i_p = \frac{V_{in}}{L_r}\left(t - t_0\right) \tag{1}$$

The duration time of this mode is

$$t_{01} = \frac{I_o L_r}{N_T V_{in}} \tag{2}$$

Mode 2 [t_1–t_2] [*see Fig*. 3(c)]: At t_1, D_{R2} and D_{R3} are turned off. The power is delivered from the input DC voltage source to the load.

Mode 3 [t_2–t_3] [*see Fig*. 3(d)]: At t_2, S_6 turns on under ZVZCS, and S_5 as well as D_6 turn off simultaneously. C_r is

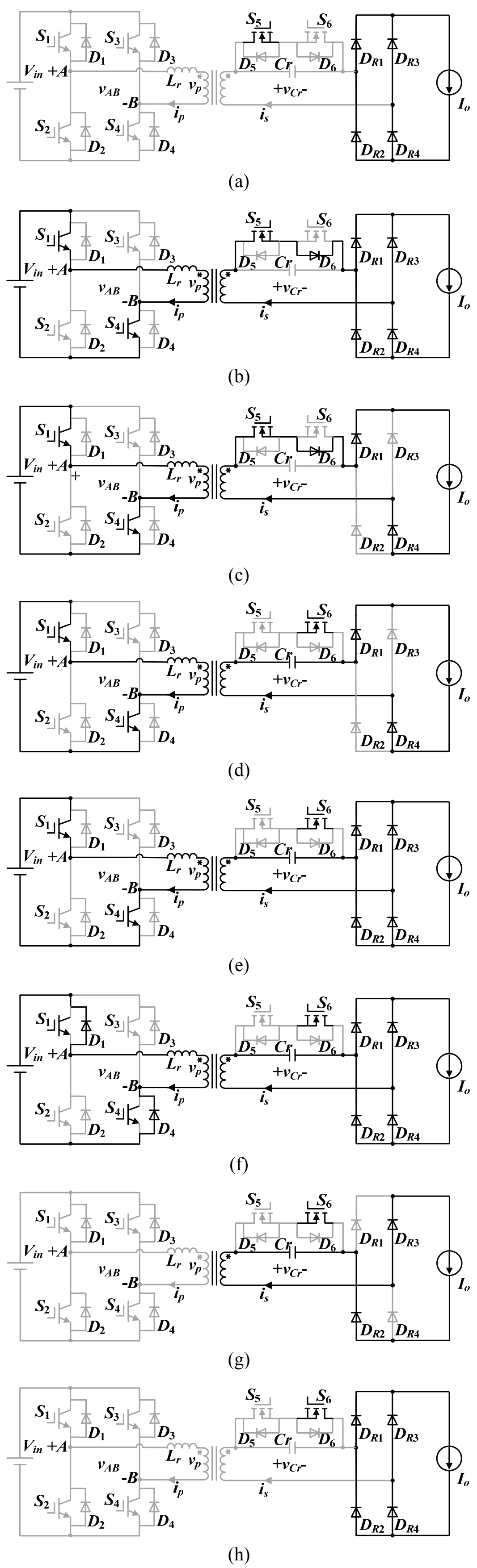


Fig. 3. Equivalent circuits of different operation modes.

charged by load current, v_{Cr} increases linearly from zero.

C_r paralleled with S_5 and D_6. Thus, S_5 and D_6 turn off under ZVS. When v_{Cr} increases to the secondary voltage, the mode 3 ends.

v_{Cr} is expressed as

$$v_{cr} = \frac{I_o}{C_r}(t - t_2) \tag{3}$$

The time duration of this mode is

$$t_{23} = \frac{V_{in} C_r}{I_o N_T} \tag{4}$$

Mode 4 [t_3–t_4] [*see Fig*. 3(e)]: At t_3, D_{R2} and D_{R3} turn on, v_d=0. The load current flows through the rectifier diodes for freewheeling. C_r resonates with L_r. Hence, i_p decreases, and v_{Cr} increases resonantly. When i_p decreases to zero, v_{Cr} increases to the maximum voltage V_{Crmax}, and Mode 4 ends.

The current through the rectifier diodes and i_{Cr} and v_{Cr} are expressed as

$$i_{DR1} = \frac{I_o}{2}\left[1 + \cos\frac{N_T}{\sqrt{L_r C_r}}(t - t_3)\right] \tag{5}$$

$$i_{DR2} = \frac{I_o}{2}\left[1\text{-}\cos\frac{N_T}{\sqrt{L_r C_r}}(t - t_3)\right] \tag{6}$$

$$i_{Cr}(t) = I_o \cos\frac{N_T}{\sqrt{L_r C_r}}(t - t_3) \tag{7}$$

$$v_{Cr} = \frac{V_{in}}{N_T} + \frac{I_o}{N_T}\sqrt{\frac{L_k}{C_r}}\sin\frac{N_T}{\sqrt{L_r C_r}}(t - t_3) \tag{8}$$

The maximum voltage V_{Crmax} is

$$V_{Cr\max} = \frac{V_{in}}{N_T} + \frac{I_o}{N_T}\sqrt{\frac{L_r}{C_r}} \tag{9}$$

The duration time of this mode is 1/4 resonant period, as follows:

$$t_{34} = \frac{\pi\sqrt{L_r C_r}}{2N_T} \tag{10}$$

Mode 5 [t_4–t_5] [*see Fig*. 3(f)]: At t_4, D_1 and D_4 turn on, C_r continues to resonate with L_r, the voltage across S_1 and S_4 is clamped at zero. Consequently, ZVZCS turn off can be achieved in S_1 and S_4. i_p rises from zero in reverse, and v_{cr} decreases from the maximum voltage. The load current flows through the rectifier diodes for freewheeling.

i_p and v_{Cr} are expressed as

$$i_p(t) = \frac{I_o}{N_T}\sin\frac{N_T}{\sqrt{L_r C_r}}(t - t_4) \tag{11}$$

$$v_{Cr}(t) = v_{Cr\max} + \frac{I_o}{N_T}\sqrt{\frac{L_r}{C_r}}\left[\cos\frac{N_T}{\sqrt{L_r C_r}}(t - t_4) - 1\right] \tag{12}$$

After 1/2 resonant period, i_p decreases to zero and v_{cr} decreases to V_{Crmin}, mode 5 ends.

The minimum voltage V_{Crmin} is

$$V_{Cr\min} = \frac{V_{in}}{N_T} - \frac{I_o}{N_T}\sqrt{\frac{L_r}{C_r}} \tag{13}$$

The duration time of this mode is 1/2 resonant period, namely,

$$t_{45} = \frac{\pi\sqrt{L_r C_r}}{N_T} \tag{14}$$

Mode 6 [t_5–t_6] [*see Fig*. 3(g)]: At t_5, i_p decreases to zero, D_{R1} and D_{R4} turn off. C_r is discharged by the output current. v_{Cr} decreases linearly. When v_{Cr} decreases to zero, mode 6 ends.

v_{Cr} is expressed as follows:

$$v_{Cr} = v_{Cr\min} - \frac{I_o}{C_r}(t - t_5) \tag{15}$$

The duration time of this mode is

$$t_{56} = \left(\frac{V_{in}}{I_o N_T} - \frac{1}{N_T}\sqrt{\frac{L_r}{C_r}}\right) C_r \tag{16}$$

Mode 7 [t_6–t_7] [*see Fig*. 3(h)]: At t_6, v_{Cr} decreases to zero, D_{R1} and D_{R4} turn on. The load current flows through rectifier diodes for freewheeling.

Mode 7 ends when S_2 and S_3 turn on, and the converter starts with the second half switching cycle. Owing to the symmetrical configuration of the proposed converter, the analysis of the second half switching cycle is omitted.

III. Steady State Characteristics

A. Output Voltage Characteristics

The waveforms of the rectifier voltage and the filter inductor current are shown in Fig. 4. The average value of the output voltage V_o approximately equal to that of the voltage v_d rectified by the transformer secondary rectifier diodes. Based on the waveform of v_d depicted in Fig. 4, V_o is given by the following:

$$V_o = \frac{1}{T_h}\int_0^{T_h} V_d(t)dt = \frac{V_{in}D}{N_T} + \frac{V_{in}^2 C_r}{2N_T^2 I_o T_h} \tag{17}$$

According to (17), when the value of the resonant capacitor is near zero, the output voltage characteristics of the converter are the same as those of the hard-switching full-bridge converter. Fig 5 shows the effects of the different auxiliary resonant capacitor C_r on the output voltage characteristics under an open-loop control scheme when the output load R=10Ω (Fig. 5(a) and Fig. 5(b) are , the 2D and 3D plots). Clearly, the output voltage increases with the increasing in the auxiliary resonant capacitor C_r, which is beneficial to improve the voltage gain.

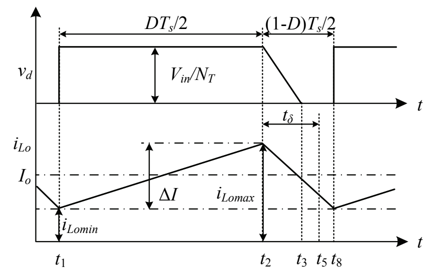
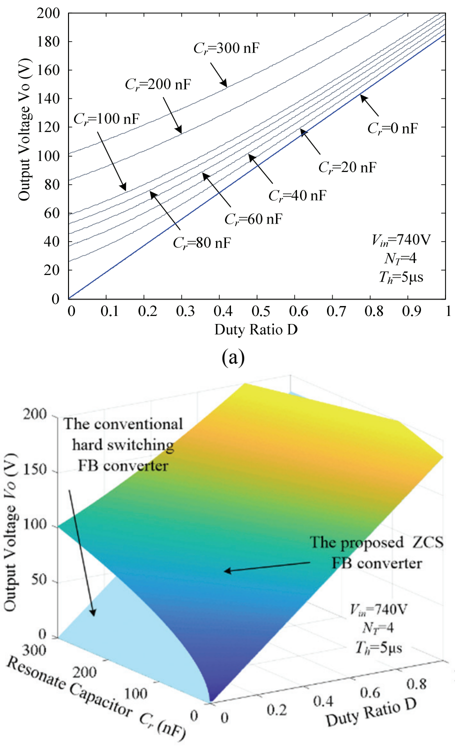


Fig. 4. Waveforms of rectified voltage and output filter current.



(a)

(b)

Fig. 5. Open loop output voltage (R_o=10Ω). (a) Two-dimensional plot. (b) Three-dimensional plot.

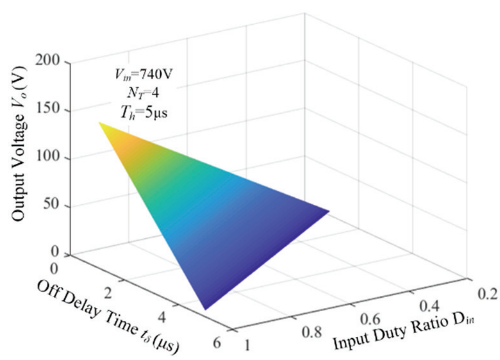


Fig. 6. Open loop output voltage with different t_δ (R_o=10Ω).

Fig. 6 shows the effect of different off delay time t_δ on the output voltage characteristics under an open-loop control scheme when the output load R=10Ω. Fig. 6 intuitively shows that the output voltage decreases as t_δ increases when the input duty ratio D_{in} is constant.

TABLE I
VOLTAGE AND CURRENT STRESS ON MAIN COMPONENTS OF THE REFERENCE CONVERTERS

Topology	Current stress	Voltage stress	
	Primary switches	Auxiliary switches	Rectifier diodes
Traditional phase shift full bridge converter	$\frac{I_o}{N_T}$	-	$\frac{V_{in}}{N_T}$
Proposed converter	$\frac{I_o}{N_T}$	$\frac{V_{in}}{N_T}+\frac{I_o}{N_T}\sqrt{\frac{L_r}{C_r}}$	$\frac{V_{in}}{N_T}$

B. Maximum Current and Voltage Stresses of Components

The voltage and current stress on the main components of the proposed converter and the traditional phase shift full-bridge converter are shown in Table I.

From Table I, it can be seen that the current stress on the primary switches and the voltage stress on the rectifier diodes of the proposed converter are the same as that of the traditional phase shift full-bridge converter. Decreasing L_r or increasing C_r is beneficial to the reduction of voltage stress on the auxiliary switches under the same input voltage V_{in}, load current I_o, and ratio of the transformer N_T.

C. dv/dt of Auxiliary Switches and di/dt of Rectifier Diodes

According to (1) and (3), the voltage change rate dv/dt of auxiliary switches during turn-off transient. The current change rate di/dt of the rectifier diodes during primary switch turn-on transient can be obtained as follows:

$$\frac{dv}{dt}=\frac{I_o}{C_r} \tag{18}$$

$$\frac{di}{dt}=\frac{V_{in}}{L_r} \tag{19}$$

Based on (18) and (19), we know that the voltage change rate dv/dt of auxiliary switches during turn-off transient and the current change rate di/dt of the rectifier diodes during primary switch turn-on transient are constants. It illustrates that the voltage across the auxiliary switches during turn-off transient and the current through the rectifier diodes during primary switch turn-on transient are in linear variation, and these change rates can be designed arbitrarily in the parameter design.

IV. SOFT-SWITCHING IMPLEMENTATION CONDITION

A. ZCS Implementation Condition of Primary Switch

Based on the operation principle of the converter, it can be seen that $t_{24}=t_{23}+t_{34}$ and $t_{25}=t_{23}+t_{34}+t_{45}$ from Fig. 2 and Fig. 3. To achieve ZVZCS turn off for the primary switches, the off delay time t_δ should satisfy $t_{24}\le t_\delta\le t_{25}$, according to(4), (10) and (14), t_δ can be expressed as

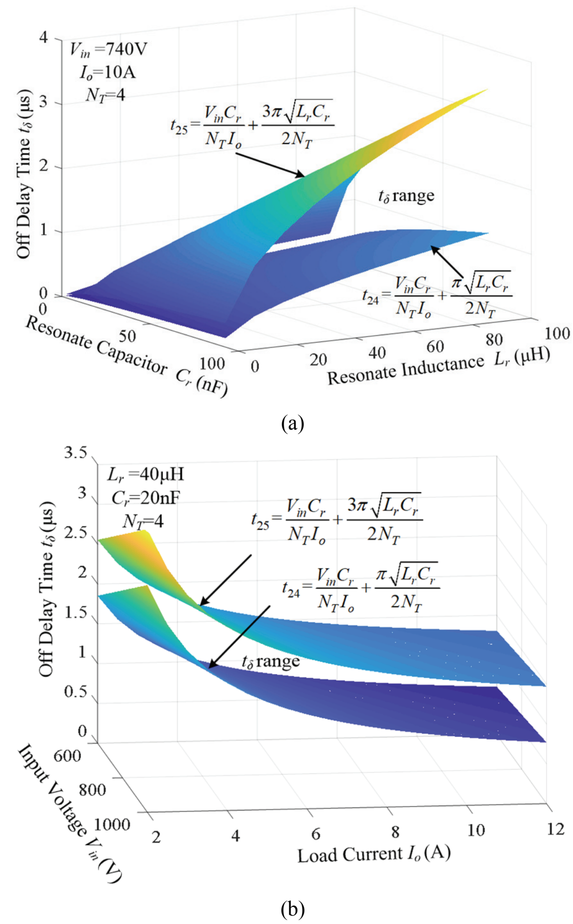


Fig. 7. Range of off delay time t_δ. (a) Range of t_δ with different C_r and L_r. (b) Range of t_δ with different V_{in} and I_o.

$$\frac{V_{in}C_r}{N_T I_o}+\frac{\pi\sqrt{L_r C_r}}{2N_T}\le t_\delta\le\frac{V_{in}C_r}{N_T I_o}+\frac{3\pi\sqrt{L_r C_r}}{2N_T} \tag{20}$$

Based on (20), the off delay time t_δ is related to the input voltage V_{in}, the load current I_o, the auxiliary resonant capacitor C_r, and the resonant inductor L_r. Fig. 7 shows the influence of the parameter variation on the value range of the off delay time t_δ. Fig. 7(a) shows the influence of the variation range of C_r and L_r to the off delay time t_δ when V_{in} and I_o are constant. Fig. 7(b) shows the influence of the input voltage V_{in} and the load current I_o to the range of the off delay time t_δ when C_r and L_r are constant. As evident from Fig. 7, when the input voltage V_{in} and the load current I_o are constant, the value interval length of the off delay t_δ varies with the different value of C_r and L_r. The larger value of C_r and L_r, and the longer value interval length of t_δ. When C_r and L_r are constant, the value interval length of t_δ does not change with the input voltage V_{in} and the load current I_o.

Fig. 8 shows the range ($t_{24}(I_{omax})\le t_\delta\le t_{25}(I_{omax})$) of the off delay time t_δ to realize the primary switches ZCS turn off under the maximum load current I_{omax}. The A area in the Fig. 8 is the soft switching area. Fig. 8 shows the larger the off delay time t_δ, the wider the soft switching range of load current.

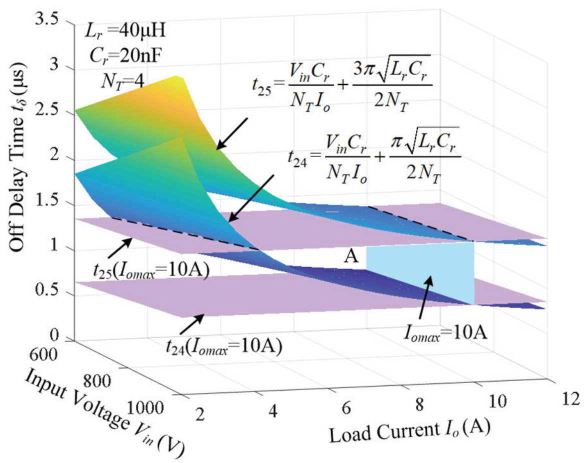


Fig. 8. Soft switching range.

B. ZVS Implementation Condition of Auxiliary Switch

To achieve ZVZCS turn on for the auxiliary switches, the voltage v_{Cr} must drop to zero during the dead time t_d.

Thus, t_d should satisfy $t_d \geq t_{56}$ according to(16), t_d can be expressed as

$$t_d \geq \frac{V_{in}C_r}{I_o N_T} - \frac{\sqrt{L_r C_r}}{N_T} \tag{21}$$

C. Maximum Effective Duty Cycle

Owing to the existence of the resonant inductance L_r and the auxiliary resonant capacitor C_r, the effective duty cycle D_{eff} in the secondary is smaller than the duty cycle D_{in} in the primary. The difference is the duty cycle loss D_{loss}. During the period of $[t_0,t_1]$ ($[t_7,t_8]$), negative voltage (positive voltage) occurs in the primary, but the primary is insufficient to provide for the load current. Therefore, the rectifier diodes D_{R1}–D_{R4} are both conducting, and the secondary voltage v_d=0. During the period of $[t_3,t_5]$ ($[t_{10},t_{12}]$), negative voltage (positive voltage) in the primary, but series resonance occurs between the resonant inductance L_r and resonant capacitor C_r. The primary does not provide for the load. Therefore, the rectifier diodes D_{R1}–D_{R4} are conducting, and the secondary voltage v_d=0. Thus, the voltage of $[t_0,t_1]$, $[t_3,t_5]$, $[t_7,t_8]$, and $[t_{10},t_{12}]$ are lost in the secondary, so the ratio of this duration time to T_h is D_{loss}:

$$D_{loss} = \frac{t_{01}+t_{34}+t_{45}}{T_h} \tag{22}$$

Based on (2), (10) and (14),

$$D_{loss} = \frac{3\pi\sqrt{L_r C_r}}{2N_T T_h} + \frac{I_o L_r}{N_T V_{in} T_h} \tag{23}$$

Considering the dead time and the duty cycle loss, the maximum effective duty cycle $D_{eff\text{-}max}$ of the converter is:

$$D_{eff-max} = 1 - D_{td} - D_{loss} \tag{24}$$

Among it, D_{td} is expressed as

$$D_{td} = \frac{t_d}{T_h} \tag{25}$$

Based on (23) and (25),

$$D_{eff-\max} = 1 - \left(\frac{3\pi\sqrt{L_r C_r}}{2N_T T_h} + \frac{I_o L_r}{N_T V_{in} T_h} + \frac{t_d}{T_h} \right) \tag{26}$$

V. Power Loss Analysis

A. Power Components Loss

The losses of the proposed converter include the switching loss and conduction loss of switching elements and the other losses generated by transformer and inductance and capacitor. The primary switches that use IGBT are ZVZCS turn off; the auxiliary switches that use MOSFET are ZVZCS turn on. Therefore, the losses of the switching elements only include the conduction loss, and it consists of three parts.

1) Conduction Loss of the Primary Switches:

The conduction loss $P_{Q1\text{-conl}}$ of switches Q_1/Q_2 includes the conduction loss $P_{S1\text{-conl}}$ of switches S_1/S_2 and the conduction loss $P_{D1\text{-conl}}$ of its antiparallel diodes. The conduction losses of switches Q_1/Q_2, $P_{Q1\text{-conl}}$ is expressed as

$$\begin{aligned} P_{Q_1-\text{conl}} &= P_{S_1-\text{conl}} + P_{D_1-\text{conl}} \\ &= f_s V_{S_1} \int_{t_0}^{t_4} i_{S_1} dt + f_s V_{D_1} \int_{t_4}^{t_5} i_{D_1} dt \\ &= f_s V_{S_1} \left(\frac{I_o D T_h}{N_T} + \frac{V_{in} C_r}{N_T^2} + \frac{I_o \sqrt{L_r C_r}}{N_T^2} \right) + f_s V_{D_1} \frac{I_o \sqrt{L_r C_r}}{N_T^2} \end{aligned} \tag{27}$$

where, $V_{S1}(V_{S2})$ and $V_{D1}(V_{D2})$ are the collector-emitter saturation voltage of switches Q_1/Q_2 and forward voltage of antiparallel diodes D_1/D_2, respectively.

The loss condition of switches Q_3/Q_4 is the same as that of switches Q_1/Q_2.

2) Conduction Loss of the Auxiliary Switches:

The conduction loss $P_{Q5\text{-conl}}$ of switch Q_5 includes the conduction loss $P_{S5\text{-conl}}$ of switches S_5 and the conduction loss $P_{D5\text{-conl}}$ of its antiparallel diode. The conduction losses of switch Q_5, $P_{Q5\text{-conl}}$ is expressed as

$$\begin{aligned} P_{Q_5-\text{conl}} &= P_{S_5-\text{conl}} + P_{D_5-\text{conl}} \\ &= f_s I_o^2 R_{DS(on)} D T_h + f_s V_{D_5} \int_{t_0}^{t_2} i_{D_5} dt \\ &= f_s I_o^2 R_{DS(on)} D T_h + f_s V_{D_5} I_o D T_h \end{aligned} \tag{28}$$

where V_{D5} is the forward voltage of antiparallel diode D_5 for the auxiliary switch S_5; $R_{DS(on)}$ is the conduction resistance of the auxiliary switch.

The condition loss of switch Q_6 is the same as that of switch Q_5.

3) Conduction Loss of Diodes:

The conduction loss of rectifier diodes D_{R1} (D_{R4}), $P_{DR1\text{-conl}}$ is expressed as

$$P_{D_{R1}-conl} = f_s V_{D_{R1}} \int_{t_0}^{t_6} i_{D_{R1}} dt = f_s V_{D_{R1}} \left[I_o D T_h + \frac{3V_{in}C_r}{2N_T} + \frac{(3\pi - 6) I_o \sqrt{L_r C_r}}{4N_T} \right] \quad (29)$$

where V_{DR1} is the forward voltage of rectifier diode D_{R1}.

The total loss of the converter P_{total} is expressed as follows:

$$P_{total} = 4P_{Q1-conl} + 2P_{Q5-conl} + 4P_{DR1-conl} \quad (30)$$

B. Circulating Current Loss Analysis

Based on the operation principle of the converter, mode 5 is the circulation period (see Fig. 3). According to (27), the circulating current loss is as follows:

$$P_{cir} = f_s V_{D_1} \int_{t_2}^{t_3} i_{D_1} dt = \frac{f_s I_o V_{D_1} \sqrt{L_r C_r}}{N_T^2} = \left(\frac{f_s I_o V_{D_1}}{2\pi N_T} \right) T_r \quad (31)$$

where $T_r = \frac{2\pi \sqrt{L_r C_r}}{N_T}$ is the resonance cycle.

Based on (11) and (31), we obtain the following.

(1) The square wave current with the amplitude value of the load current flowing through the primary side during circulation period in the conventional phase-shifted full-bridge converter. Compared with it, the circulating current is sinusoidal with the amplitude value of the load current in the proposed converter (see mode 5 in Fig. 3). The effective value of the circulating current is small. Thus, the circulating current loss is relatively smaller.

(2) The magnitude of the circulating current loss is related to the resonant period T_r. It means that the smaller the resonant period is, the smaller the circulating current loss.

VI. PARAMETER DESIGN

A. Design Methodology

Assuming that the input minimum DC voltage is V_{inmin}, the output maximum voltage is V_{omax} and the output maximum load current is I_{omax}. The parameter design of the converter should satisfy the following conditions:

1) Turns Ratio of the Transformer:

To achieve the required output maximum voltage at the lowest input voltage, the turn ratio of the transformer should satisfy the following equation:

$$N_T = \frac{V_{in\min} D_{eff\text{-}\max}}{V_{o\max} + 2V_D + V_{Lf}} \quad (32)$$

where V_D is the voltage drop in the secondary rectifier diode, V_{Lf} is the voltage drop in the output filter inductor.

2) Design of the Auxiliary Resonant Capacitor C_r:

To reduce the turn off the loss of the auxiliary switches, the voltage change rate dv/dt of auxiliary switches during turn-off transient should be smaller than or equal to the setting voltage change rate $(dv/dt)_{set}$. Based on (18), the rate can be expressed as follows:

$$\frac{I_{o\max}}{C_r} \le \left(\frac{dv}{dt} \right)_{set} \quad (33)$$

3) Design of the Resonant Inductor L_r:

To reduce the turn off the loss of the primary switches, the current change rate di/dt of primary switches during the turn-off transient period should smaller than or equal to the setting current change rate $(di/dt)_{set}$. Based on (19), the rate can be expressed as follows:

$$\frac{V_{in}}{L_r} \le \left(\frac{di}{dt} \right)_{set} \quad (34)$$

B. Design Example

The design example of circuit parameters in the prototype is demonstrated by using the numerical example of rating values as follows: input minimum DC voltage V_{inmin}=740 V, output maximum voltage V_{omax}=100 V, output maximum load current I_{omax}=10 A, switching frequency f_S=100 kHz, and rated load resistance R=10 Ω.

Assuming that the voltage change rate of the auxiliary switches $(dv/dt)_{set}$=500 V/μs, the current change rate of the primary switches $(di/dt)_{set}$=20 A/μs, the maximum effective duty cycle $D_{eff\text{-}max}$=0.58. The voltage drop of rectifier diode V_D=1.5 V, the voltage drop of the filter inductor V_{Lf}=0.1 V.

According to (32), the turns ratio of the transformer is N_T=4.16, N_T=4 is chosen. Owing to the voltage change rate of the auxiliary switches $(dv/dt)_{set}$=500V/μs, based on (33), C_r≥0.02 μF, and C_r is set as 0.02 μF. Owing to the current change rate of the primary switches $(di/dt)_{set}$=20 A/μs, according to (34), L_r≥37 μH, L_r is set as 40 μH.

According to(20), 0.7 $\mu s \le t_\delta \le 1.42\ \mu s$, $t_\delta = 1.4\ \mu s$ is chosen. Based on (21), $t_d \ge 0.7\ \mu s$, $t_d = 0.7\ \mu s$ is chosen.

To verify the rationality of the parameter design, based on (23) and (25), D_{loss} =0.24 and D_{td} =0.14. $D_{loss}+D_{td}+D_{eff\text{-}max}$=0.96<1. Consequently, the values of parameter design satisfy the demand.

VII. EXPERIMENTAL RESULTS

To verify the validity of the aforementioned analysis, we built a 1 kW prototype. The auxiliary switch uses MOSFET due to its small on-state resistance and low conduction losses. The specifications of the prototype converter are given in Table II.

Fig. 9 shows the experimental waveforms of transformer primary voltage v_{AB}, current i_p, and rectified voltage v_d. Clearly, the primary voltage is smooth and does not have voltage spikes. Owing to the effects of soft-switching technology, the energy stored in the leakage inductance of the transformer is fully absorbed.

TABLE II
COMPONENTS AND PARAMETERS OF THE PROPOSED CONVERTER

Components	Parameters
V_{in} (Input voltage)	740 V
V_o (Output voltage)	100 V
f (Switching frequency)	100 kHz
t_d(Dead time)	0.7 µs
t_δ(Off delay time)	1.4 µs
S_1–S_4 (Primary Switches)	IHW15N120E1 (1200 V, 15 A)
S_5–S_6 (Auxiliary switches)	IPW60R041P6 (650 V, 77.5 A)
D_{R1}–D_{R4} (Rectifier diodes)	SIDC06D60C8 (600 V, 20 A)
N_T (Transformer turn ratio)	4:1
L_r(Resonant inductance)	40 µH
C_r (Auxiliary resonant capacitance)	20 nF
L_o (Filter inductor)	300 µH
C_o (Filter capacitance)	560 µF

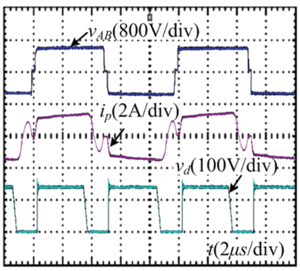
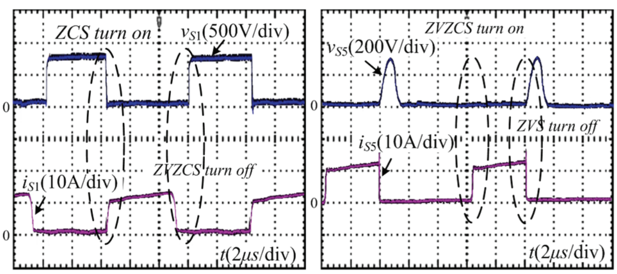


Fig. 9. Waveforms of v_{AB}, i_p, and v_d (I_o=10 A).



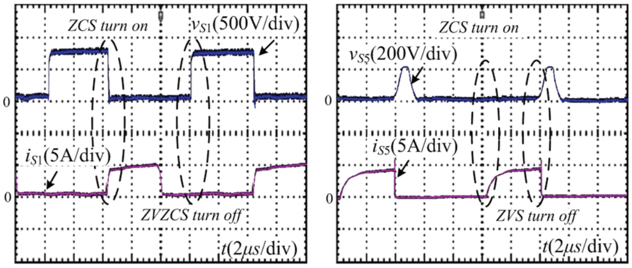
(a) (b)

Fig. 10. Switch voltage and current waveforms (I_o=10 A). (a) Switch S_1. (b) Switch S_5.

Fig. 10 and Fig. 11 show the voltage and current waveforms of the primary switch S_1 and the auxiliary switch S_5 at full load (I_o=10A) and light load (I_o=3A), respectively. From the experimental waveforms, it can be observed that the waveforms of power switches do not have voltage and current spikes. In a wide load range, S_1 turns on with ZCS and turns off with ZVZCS, and S_5 turns on with ZVZCS and turns off with ZVS.

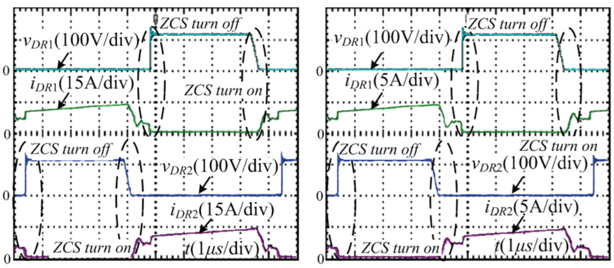
Fig. 12 shows the voltage and current waveforms of the rectifier diode D_{R2} and D_{R4} at full load (I_o=10A) and light load (I_o=3A). It can be seen directly, rectifier diodes can achieve natural switching. And it avoids the reverse recovery problem when the rectifier diode is turned off.

The experimental power loss analysis of the proposed converter and the traditional phase shift full-bridge converter under the rated power are shown in Fig. 13, where the power switch loss includes the switching loss and the conducting loss; the other loss mainly includes the transformer loss and the loss



(a) (b)

Fig. 11. Switch voltage and current waveforms (I_o=3 A). (a) Switch S_1. (b) Switch S_5.



(a) (b)

Fig. 12. Voltage and current waveforms of D_{R1} and D_{R2}. (a) Full load (I_o=10 A). (b) Light load (I_o=3 A).

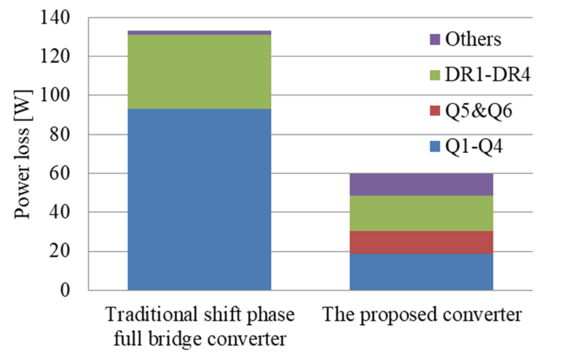


Fig. 13. Power loss analysis.

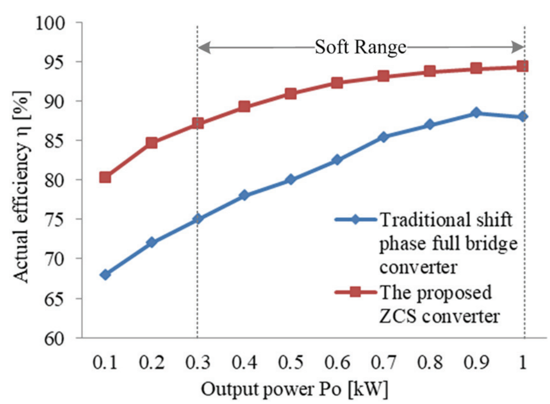


Fig. 14. Efficiency curves.

caused by inductors, capacitors, and line resistances. Based on Fig. 13, compared with the traditional phase shift full-bridge converter, the loss caused by the auxiliary switches Q_5 and Q_6 of the proposed converter is 11.44W, but the total loss saved by the primary switches Q_1–Q_4 is 74.45W. The total loss of the proposed converter is 59.87W, and the total loss of the traditional phase shift full-bridge converter is 133.19W. Therefore, the total loss savings is 73.32W in the proposed converter compared with the traditional phase shift full-bridge converter.

Fig. 14 illustrates the actual power efficiency characteristics of the proposed converter and the traditional phase shift full-bridge converter. Compared with the traditional phase shift full-bridge converter, the overall efficiency of the proposed converter has been appreciably improved, and it is more obvious at the light load. The total actual efficiency of the proposed converter is 94.35% at rated output power 1kW, improving approximately by 6.1%, while improving approximately by 13% at an output power of 300W. However, under power 300W, the proposed converter does not realize complete soft switching. At output power 100W, the efficiency is 81% which is improved approximately by 10%.

VIII. Conclusions

A novel ZCS full-bridge soft switching DC–DC converter topology and modulation strategy has been proposed in this paper. The operation principle, the soft switching conditions, and parameter design of the proposed converter have been illustrated in detail. Based on the theoretical analysis and the experimental research on the 1kW prototype, several conclusions have been summarized as follows.

1) The primary switches S_1–S_4 realize ZVZCS turn off and ZCS turn on, and the auxiliary switches S_5 and S_6 realize ZVS turn off and ZVZCS turn on, thereby reducing the switching loss.
2) The rectifier diodes achieve natural switching, and they overcome the reverse recovery problem.
3) The circulating current loss in the proposed converter is smaller than that of the phase shifted full-bridge converter. Furthermore, the smaller the resonant cycle is, the smaller the circulating current loss.
4) The current stress of the primary switches and the voltage stress of the rectifier diodes are the same as the phase-shifted full-bridge converter.
5) The efficiency of the proposed converter is higher than that of the traditional phase shifted full-bridge converter, and this is more obvious in light load. At output power 300 W, the efficiency can be obtained as 88%, which is improved approximately by 13%. At rated power 1kW, the actual high efficiency can be obtained as 94.35%, which is improved approximately by 6.1%.

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