

# Coupled Inductor Design Method for 2-Phase Interleaved Boost Converters

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## Abstract

To achieve high efficiency and reliability, multiphase interleaved converters with coupled inductors have been widely applied. In this paper, a coupled inductor design method for 2-phase interleaved boost converters is presented. A new area product equation is derived to select the proper core size. The wire size, number of turns and air gap length are also determined by using the proposed coupled inductor design method. Finally, the validity of the proposed coupled inductor design method is confirmed by simulation and experimental results obtained from a design example.

**Key words:** 2-phase interleaved boost converter, Coupled inductor

## I. INTRODUCTION

The interleaved boost converter is widely applied in electric vehicle applications, power factor correction converters and photovoltaic arrays [1]-[3]. However, applying the interleaved technique requires additional inductors according to the number of phases. Since multiple discrete inductors make up a significant percentage of the volume and increase the complexity of converters, the coupled inductor has been proposed instead of multiple discrete inductors [4]-[7]. By integrating discrete inductors into one coupled inductor, the volume, price and number of inductors are further reduced.

As mentioned in [4], with inversely coupled inductors, the efficiency of a converter can be improved by 2 % under full loads and by 10 % under light loads when compared with non-coupled inductors. The coupled inductor can improve both the steady-state and dynamic performances of VRMs. In [8], a generalized steady-state analysis of multiphase interleaved boost converters with coupled inductors was addressed. The coupled inductors can improve both the performances of the input and the inductor ripple current.

Unfortunately, although coupled inductors can improve the performances of interleaved converters, the design methods of the coupled inductors are not mentioned in [4] and [8]. In

addition, the core size is mentioned without giving a selection method, which leads to other designers not knowing how to start the design.

A coupled inductor design method was mentioned in [9]. The core selection was facilitated by calculating the core area product (AP) required by the application, and relating this calculation to the APs of the available cores. However, this coupled inductor design method is not suitable for the coupled inductor used in interleaved boost converters. Fig. 1 shows two existing coupled inductor structures of 2-phase interleaved boost converters. These structures were first presented by P. L. Wong in [4]. The winding structures of the coupled inductors are symmetrical. Therefore, the number of turns of phase 1 and phase 2 are the same. Considering the fabrication of EE or EI cores, the air gaps in the three legs are set to be the same. This is the simplest structure which means the cores do not need to be milled, and the two core parts can rely on separation to prevent them from saturating. The structure of the coupled inductor with two windings presented in [9] for a multiple-output buck derived regulator is shown in Fig. 2. The two windings are wound in the center leg, which is different from the coupled inductor structure of the 2-phase interleaved boost converter shown in Fig. 1. The inductor voltages of the coupled inductor shown in Fig. 2 are in phase, which means the maximum flux of the core is the sum of the maximum fluxes during windings 1 and 2. However, for interleaved converters, the inductor voltages are phase shifted. In addition, for the coupled inductor shown in Fig. 2, one core window area contains two windings. Thus, the currents flowing through

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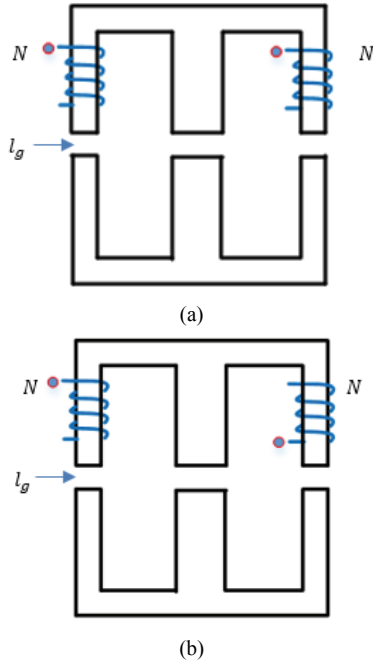


Fig. 1. Existing coupled inductor structures of a 2-phase interleaved boost converter. (a) Inversely coupled. (b) Directly coupled.

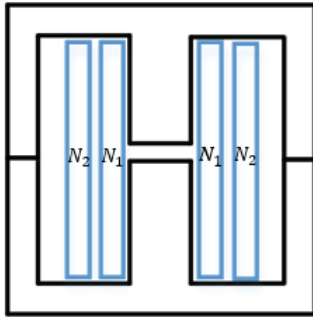


Fig. 2. Structure of the coupled inductor presented in [9].

both windings are taken into account when designing the inductor. However, for the coupled inductor used in 2-phase interleaved boost converters, there is only one winding in one core window area, which means that only one phase current needs to be considered in the design. The reasons described above lead to different AP equations for the coupled inductor of the 2-phase interleaved boost converter shown in Fig. 1 and the coupled inductor of the multiple-output buck derived regulator shown in Fig. 2.

Therefore, in this paper, with the coupled inductor structures shown in Fig. 1, a detailed coupled inductor design method is presented for 2-phase interleaved boost converters operated in the continuous conduction mode (CCM). A new AP equation is also derived for selecting the core size. The wire size, number of turns and air gap length are also determined by using the proposed coupled inductor design method. Finally, the validity of proposed coupled inductor design method is confirmed by simulation and experimental results.

## II. AREA PRODUCT OF THE COUPLED INDUCTORS FOR 2-PHASE INTERLEAVED BOOST CONVERTERS

The area product is the magnetic cross-sectional area times the window area. The AP method is a good strategy for selecting the core size when designing magnetic components. Since the energy handling capability of a core is related to its area product, the core selection is facilitated by calculating the core area product required by the application and relating this calculation to the APs of the available cores. The smallest available core can be selected from catalog data, where the area product exceeds the calculated value and the inductance is adjusted by the air gap length [10]. For the coupled inductors used in 2-phase interleaved boost converters, the AP equation can be derived as follows. The international system of units (SI) is used in the follow equations. However, the dimensions of the AP equation are later changed from meters to centimeters.

When the maximum allowed dc bias current is exceeded, the inductor saturates and the inductor peak current becomes extremely large, which results in a drop in efficiency and anomalous behavior. For 2-phase interleaved boost converters, the area product of the coupled inductors is calculated at the maximum inductor dc current. The case where the inductor dc current is maximum is regarded as the worst case. It occurs at the minimum input voltage, maximum output power and maximum duty cycle of the MOSFET. The maximum inductor dc current can be written as:

$$I_{Ldcmax} = \frac{P_{omax}}{2\eta V_o (1 - D_{max})}, \quad (1)$$

where  $P_{omax}$  is the maximum output power,  $V_o$  is the output voltage,  $\eta$  is the estimation efficiency of the converter, and  $D_{max}$  is the maximum duty cycle of the MOSFET, which can be expressed as:

$$D_{max} = 1 - \frac{V_{gmin}}{V_o}, \quad (2)$$

where  $V_{gmin}$  is the minimum input voltage.

For one core window area, the ampere-turns of one phase is equal to the current density times the conductor area of one phase, which in the worst case can be expressed as:

$$NI_{Lrmswt} = J_{max} W_a K_u, \quad (3)$$

where  $J_{max}$  is the maximum current density,  $W_a$  is one of the core window areas,  $K_u$  is the core window utilization factor, and  $I_{Lrmswt}$  is the inductor rms current in the worst case, which can be derived as:

$$I_{Lrmswt} \approx \sqrt{\left[ \frac{P_{omax}}{2\eta V_o (1 - D_{max})} \right]^2 + \frac{1}{12} \left( \frac{V_{gmin} D_{max}}{L_{eq} f_s} \right)^2}, \quad (4)$$

where  $f_s$  is the switching frequency, and  $L_{eq}$  is the equivalent inductance, which was analyzed in [4] and can be summarized as:

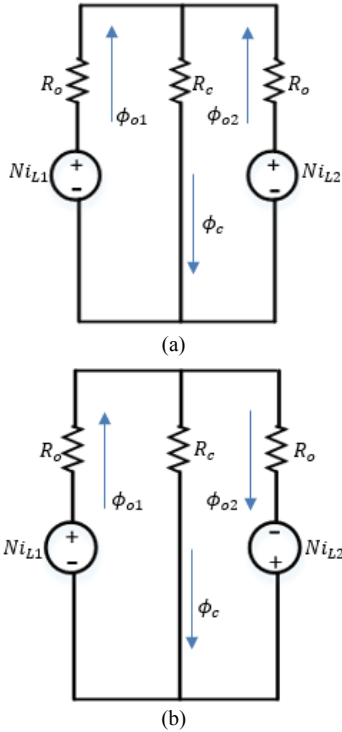


Fig. 3. Magnetic circuits. (a) Inversely coupled. (b) Directly coupled.

$$L_{eq} = \begin{cases} \frac{(L_s + \rho M)(L_s - \rho M)}{L_s + \rho M \frac{D_{max}}{1 - D_{max}}} & \text{for } 0 < D_{max} < 0.5 \\ \frac{(L_s + \rho M)(L_s - \rho M)}{L_s + \rho M \frac{1 - D_{max}}{D_{max}}} & \text{for } 0.5 < D_{max} < 1 \end{cases}, \quad (5)$$

where  $L_s$  and  $M$  are the self and mutual inductances, respectively.  $\rho$  is called coupling parameter,  $\rho = 1$  means direct coupling, and  $\rho = -1$  means inverse coupling.

In order to keep the core from saturation, the maximum flux density of the core under the worst case should be considered. For the coupled inductor structures shown in Fig. 1, the maximum flux density of the core is the maximum flux density of the outer leg (the derivation is shown in the appendix) and it can be expressed as:

$$B_{max} = \frac{\phi_{dc} + \frac{\Delta\phi}{2}}{A_{eo}}, \quad (6)$$

where  $A_{eo}$  is the cross-sectional area of the outer leg, and  $\phi_{dc}$  is the dc flux of the outer leg under the worst case, which can be obtained from the magnetic circuits shown in Fig. 3 as:

$$\phi_{dc} = \left(1 + \frac{\rho R_c}{R_o + R_c}\right) \frac{NI_{Ldcmax}}{R_o + R_o \parallel R_c}, \quad (7)$$

where  $N$  is the actual number of turns of one phase, and  $R_o$  is the reluctance of the outer leg, which can be expressed as:

$$R_o = \frac{l_g}{\mu_0 A_{eo}}, \quad (8)$$

where  $R_c$  is the reluctance of the center leg, which can be expressed as:

$$R_c = \frac{l_g}{\mu_0 A_e}, \quad (9)$$

where  $l_g$  is the air gaps in the center and outer legs,  $A_e$  is the cross-sectional area of the center leg,  $\mu_0$  is the permeability of air,  $\Delta\phi$  is the peak to peak flux of the outer leg under the worst case, which can be derived from Faraday's law as:

$$\Delta\phi = \frac{V_{gmin} D_{max}}{N f_s}. \quad (10)$$

Using the above equations, the maximum flux density under the worst case can be rewritten as:

$$B_{max} = \frac{1}{NA_{eo}} \left[ \left(1 + \frac{\rho R_c}{R_o + R_c}\right) \frac{N^2 I_{Ldcmax}}{R_o + R_o \parallel R_c} + \frac{V_{gmin} D_{max}}{2 f_s} \right]. \quad (11)$$

As mentioned in [4], the self and mutual inductances can be given as:

$$L_s = \frac{N^2}{R_o + R_o \parallel R_c}, \quad (12)$$

$$M = \frac{N^2 R_c}{(R_o + R_c)(R_o + R_o \parallel R_c)}. \quad (13)$$

Substituting (12) and (13) into (11) gives:

$$B_{max} = \frac{1}{NA_{eo}} \left[ (L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2 f_s} \right]. \quad (14)$$

Solving the above equation for  $N$  yields:

$$N = \frac{(L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2 f_s}}{B_{max} A_{eo}}. \quad (15)$$

Substituting (15) into (3) gives:

$$\frac{(L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2 f_s}}{B_{max} A_{eo}} I_{Lrmswt} = J_{max} W_a K_u. \quad (16)$$

Since  $A_e \approx 2A_{eo}$ , the above equation can be rewritten as:

$$2 I_{Lrmswt} \left[ \frac{(L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2 f_s}}{B_{max} A_e} \right] \approx J_{max} W_a K_u. \quad (17)$$

Finally, the above equation is solved for the area product dimension in centimeters as:

$$AP = W_a A_e = \frac{2 \times 10^4 I_{Lrmswt} \left[ \frac{(L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2 f_s}}{B_{max} A_e} \right]}{J_{max} B_{max} K_u} \text{ cm}^4. \quad (18)$$

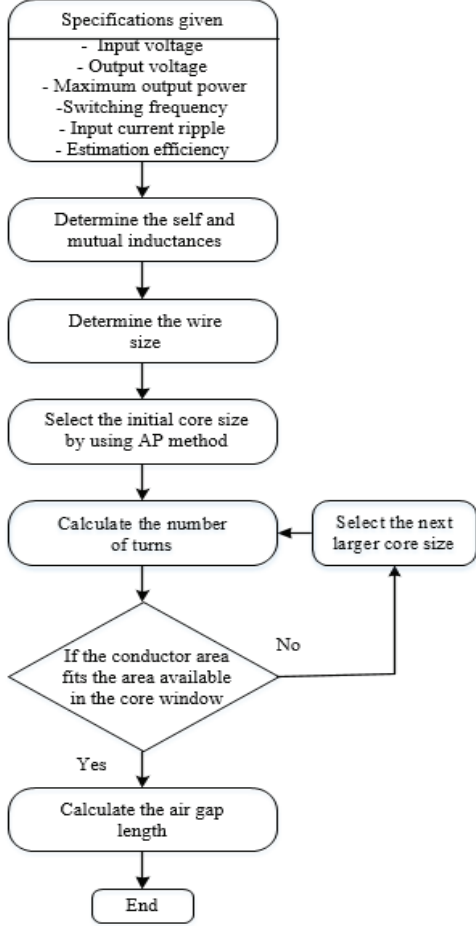


Fig. 4. Flowchart of the coupled inductor design method procedure for 2-phase interleaved boost converters.

### III. PROPOSED COUPLED INDUCTOR DESIGN METHOD FOR 2-PHASE INTERLEAVED BOOST CONVERTERS

A flowchart of the procedure for the proposed coupled inductor design method for 2-phase interleaved boost converters is presented in Fig. 4.

#### Step-1: Specifications given

The starting point of the procedure is the specifications of the converter system.

#### Step-2: Determine the self and mutual inductances

The input ripple current analyzed in [8] can be expressed as:

$$\Delta i_g = \begin{cases} \frac{V_g(1-2D)D}{(L_s + \rho M)(1-D)f_s} & \text{for } 0 < D < 0.5 \\ \frac{V_g(2D-1)}{(L_s + \rho M)f_s} & \text{for } 0.5 < D < 1 \end{cases}, \quad (19)$$

where  $V_g$  is the input voltage and  $D$  is the duty cycle of the MOSFET.

Since  $A_e \approx 2A_{eo}$ , substituting this into (8) and (9) gives:

$$R_o \approx 2R_c. \quad (20)$$

Substituting (20) into (12) and (13) gives:

$$L_s \approx 3M. \quad (21)$$

Then under the worst case, the self and mutual inductances can be derived from (19) and (21) as:

$$L_s = \begin{cases} \frac{3V_{gmin}(1-2D_{max})D_{max}}{(3+\rho)\Delta i_{gmax}(1-D_{max})f_s} & \text{for } 0 < D_{max} < 0.5 \\ \frac{3V_{gmin}(2D_{max}-1)}{(3+\rho)\Delta i_{gmax}f_s} & \text{for } 0.5 < D_{max} < 1 \end{cases}, \quad (22)$$

$$M = \begin{cases} \frac{V_{gmin}(1-2D_{max})D_{max}}{(3+\rho)\Delta i_{gmax}(1-D_{max})f_s} & \text{for } 0 < D_{max} < 0.5 \\ \frac{V_{gmin}(2D_{max}-1)}{(3+\rho)\Delta i_{gmax}f_s} & \text{for } 0.5 < D_{max} < 1 \end{cases}, \quad (23)$$

where  $\Delta i_{gmax}$  is the maximum input ripple current, which can be expressed as:

$$\Delta i_{gmax} = \%ripple \cdot I_{gmax}, \quad (24)$$

where  $\%ripple$  is the input current ripple at the minimum input voltage and a full load, given in the specifications. In addition,  $I_{gmax}$  is the maximum input dc current, which can be written as:

$$I_{gmax} = \frac{P_{omax}}{\eta V_o(1-D_{max})}. \quad (25)$$

When  $D_{max}$  is 0.5, the input current ripple is 0 for any self-inductances or mutual inductances. The inductance matrix cannot be determined.

#### Step-3: Determine the wire size

The wire area  $A_w$  can be determined as:

$$A_w \geq \frac{I_{Lrmswt}}{J_{max}}. \quad (26)$$

With the calculated  $A_w$ , a proper wire size can be selected from the wire table.

#### Step-4: Select the initial core size

The initial core size is selected by using the AP method. In addition, (18) shows the derived AP equation as:

$$AP = \frac{2 \times 10^4 I_{Lrmswt} \left[ (L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2f_s} \right]}{J_{max} B_{max} K_u} \text{ cm}^4. \quad (27)$$

#### Step-5: Calculate the number of turns

The minimum number of turns is expressed in (15) as:

$$N_{min} = \frac{(L_s + \rho M) I_{Ldcmax} + \frac{V_{gmin} D_{max}}{2f_s}}{B_{max} A_{eo}}. \quad (28)$$

The actual number of turns  $N$  is the next integer value greater than  $N_{min}$ .

**Step-6: Check the window**

Check the conductor area with  $N$  wires to make sure it fits the area available in the core window, which is shown as follows:

$$NA_w \leq K_u W_a. \quad (29)$$

If not, the next larger core size should be selected.

**Step-7: Calculate the air gap length**

The air gap length can be obtained by solving equations (8), (12) and (20) as:

$$l_g = \frac{3N^2 \mu_0 A_{eo}}{4L_s}. \quad (30)$$

## IV. DESIGN EXAMPLE

A design example is shown as follows to demonstrate the proposed coupled inductor design method.

**Step-1: Specifications given**

The specifications are given in Table I.

**Step-2: Determine the self and mutual inductances**

From (2), the maximum duty cycle of the MOSFET is:

$$D_{max} = 1 - \frac{18}{48} = 0.625.$$

Then the maximum input dc current can be calculated from (25) as:

$$I_{gmax} = \frac{48}{48 \times 97\% \times (1 - 0.625)} = 2.749 \text{ A}.$$

Next, the maximum input ripple current is calculated from (24):

$$\Delta i_{gmax} = 5\% \times 2.749 = 0.137 \text{ A}.$$

Finally, the self and mutual inductances can be obtained from (22) and (23) as:

$$L_s = \frac{3 \times 18 \times (2 \times 0.625 - 1)}{(3 - 1) \times 0.137 \times 123000} = 399 \text{ } \mu\text{H},$$

$$M = \frac{18 \times (2 \times 0.625 - 1)}{(3 - 1) \times 0.137 \times 123000} = 133 \text{ } \mu\text{H}.$$

**Step-3: Determine the wire size**

In the worst case, with the calculated self and mutual inductances,  $L_{eq}$  can be given from (5) as:

$$L_{eq} = \frac{(399 + 133) \times (399 - 133)}{399 - 133 \times \frac{1 - 0.625}{0.625}} = 444 \text{ } \mu\text{H},$$

which means the inductor rms current in the worst case is (from (4)):

TABLE I  
SPECIFICATIONS OF THE 2-PHASE INTERLEAVED BOOST CONVERTER

Parameters	Values
Coupled inductor type	Inversely
Input voltage	18 ~ 45 V
Output voltage	48 V
Maximum output power	48 W
Switching frequency	123 kHz
Input current ripple (peak to peak)	5 % @ minimum input voltage and full load
Estimation efficiency	97 % @ minimum input voltage and full load

$$I_{Lrmswt} \approx \sqrt{\left[ \frac{48}{2 \times 97\% \times 48 \times (1 - 0.625)} \right]^2 + \frac{1}{12} \times \left( \frac{18 \times 0.625}{444 \times 10^{-6} \times 123000} \right)^2} \approx 1.375 \text{ A}.$$

$I_{max}$  is selected as 600 A / cm<sup>2</sup>. Then the wire size can be determined from (26) as:

$$A_w \geq \frac{1.375}{600} = 0.0023 \text{ cm}^2.$$

From the wire table, a 24 AWG wire size is selected with  $A_w = 0.0025 \text{ cm}^2$ .

**Step-4: Select the initial core size**

The maximum inductor dc current can be calculated from (1) as:

$$I_{Ldmax} = \frac{48}{2 \times 97\% \times 48 \times (1 - 0.625)} = 1.375 \text{ A}.$$

The core material is a ferrite PC40. Thus,  $B_{max}$  is set as 0.3 T. In addition,  $K_u$  is selected as 0.3. Then the area product can be given from (27) as:

$$AP = \frac{2 \times 10^4 \times 1.375 \times \left[ (3.99 \times 10^{-4} - 1.33 \times 10^{-4}) \times 1.375 + \frac{18 \times 0.625}{2 \times 123000} \right]}{600 \times 0.3 \times 0.3} = 0.210 \text{ cm}^4.$$

An EI25 core is selected with  $AP = 0.339 \text{ cm}^4$ ,  $A_{eo} = 0.203 \text{ cm}^2$  and  $W_a = 0.772 \text{ cm}^2$ .

**Step-5: Calculate the number of turns**

The minimum number of turns is given from (28) as:

$$N_{min} = \frac{\left[ (3.99 \times 10^{-4} - 1.33 \times 10^{-4}) \times 1.375 + \frac{18 \times 0.625}{2 \times 123000} \right]}{0.3 \times 2.03 \times 10^{-5}} = 67.8.$$

Therefore, the actual number of turns is 68.

**Step-6: Check the window**

The calculated actual number of turns and the selected wire size lead to:

$$NA_w = 68 \times 0.0025 = 0.17 \text{ cm}^2.$$

In addition:

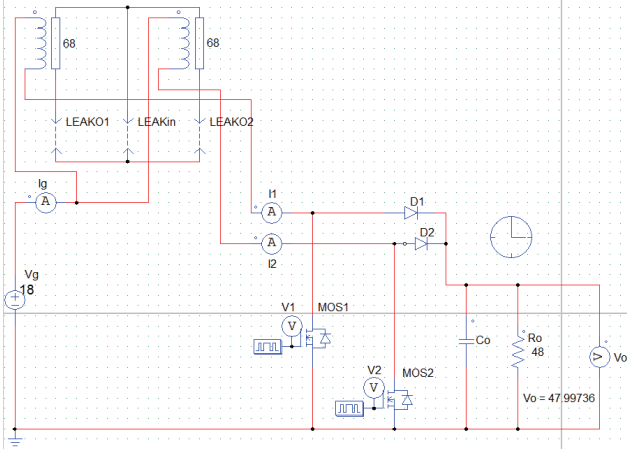


Fig. 5. Simulation model of a 2-phase interleaved boost converter with a coupled inductor structure in PSIM.

$$K_u W_a = 0.3 \times 0.772 = 0.23 \text{ cm}^2.$$

Check the window with (29),  $0.17 \text{ cm}^2 < 0.23 \text{ cm}^2$ , to make sure the EI25 core is a proper size.

#### Step-7: Calculate the air gap length

The air gap length can be calculated from (30) as:

$$l_g = \frac{3 \times 68^2 \times 4\pi \times 10^{-7} \times 2.03 \times 10^{-5}}{4 \times 399 \times 10^{-6}} = 0.22 \text{ mm}.$$

## V. SIMULATION AND EXPERIMENTAL RESULTS

Fig. 5 shows the simulation model for a 2-phase interleaved boost converter with a coupled inductor structure in PSIM. The input voltage is 18 V and the output power is 48 W. The simulated inductor current with a gate signal is plotted in Fig. 6(a), and the simulated input current is illustrated in Fig. 6(b). From Fig. 6(b), the simulated input ripple current is about 0.13 A, which has a small difference from the designed value 0.137 A. This is due to the fact that the efficiency of the converter in the simulation is 100 %. The simulated flux densities of the left and right outer legs are shown in Fig. 7, the maximum flux density is about 0.3 T, which satisfies the design very well.

A prototype of a coupled inductor with 68 turns per phase is shown in Fig. 8. By adjusting the air gap length to 0.3 mm, the self and mutual inductances measured with a precision LCR meter are 393  $\mu\text{H}$  and 106  $\mu\text{H}$ , respectively. When compared with the calculated inductances in step-2, the self-inductance has an error of 6  $\mu\text{H}$  and the mutual inductance has an error of 27  $\mu\text{H}$ . This is due to the fact that the air gap length of the coupled inductor during measurements and calculations is different. In addition, the leakage fluxes of the windings leaking into the air are neglected during calculations.

Experimental waveforms of the input and inductor currents are shown in Fig. 9 with a 48 W output power and an 18 V input voltage. The inductor current trend with a gate voltage shown in Fig. 9(a) is similar to that shown in Fig. 6(a). The input and

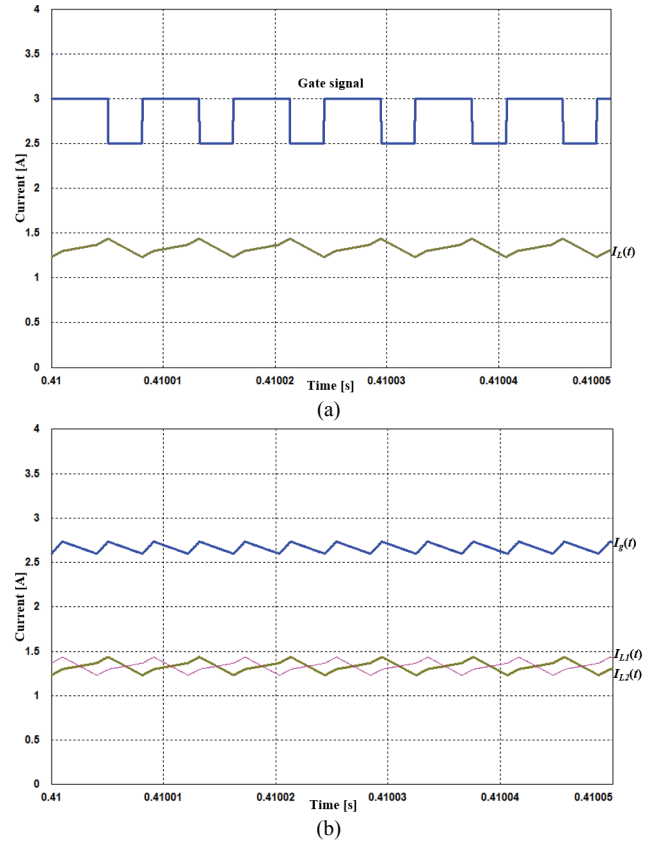


Fig. 6. Simulation waveforms. (a) Inductor current with a gate signal ( $I_L(t)$ : inductor current). (b) Input and inductor currents ( $I_g(t)$ : input current;  $I_{L1}(t)$ : inductor current of phase 1;  $I_{L2}(t)$ : inductor current of phase 2).

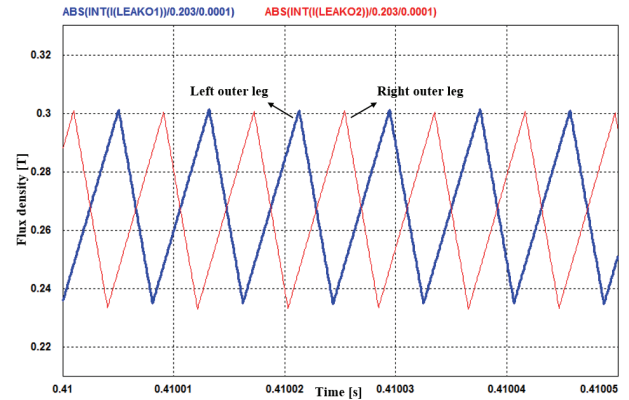


Fig. 7. Simulated flux densities of the left and right outer legs.

inductor waveforms illustrated in Fig. 9(b) coincide with those sketched in Fig. 6(b). From Fig. 9(b) it can be seen that the measured input ripple current is about 0.14 A, which matches the designed input ripple current in step-2. The measured efficiency of the converter and the inductor temperature with an 18 V input voltage are plotted in Figs. 10 and 11, respectively. Under a full load, the measured efficiency is about 96.3 % and the measured inductor temperature is about 50 °C at room temperature without fan cooling. These measurements also satisfy the design.

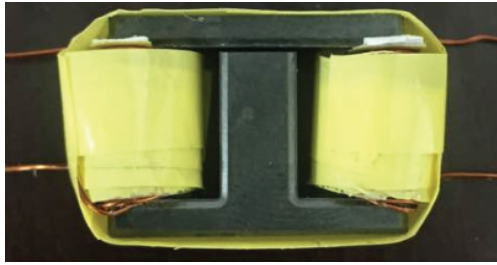
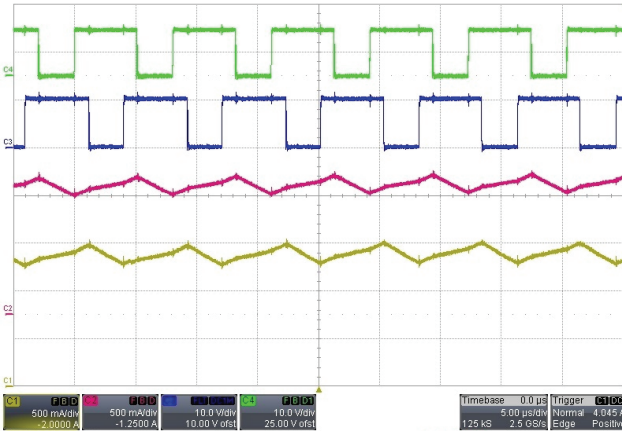
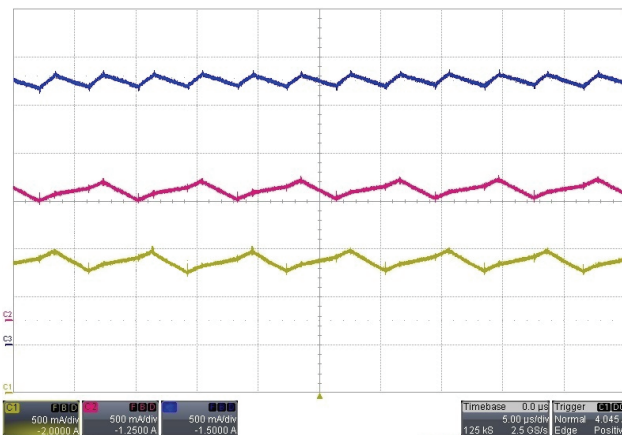


Fig. 8. Prototype of a coupled inductor.



(a)



(b)

Fig. 9. Experimental waveforms. (a) Inductor currents with gate voltages. From bottom to top: trace C1 (inductor current of phase 1), 500 mA/div; trace C2 (inductor current of phase 2), 500 mA/div; trace C3 (gate voltage of MOSFET 1), 10 V/div; trace C4 (gate voltage of MOSFET 2), 10 V/div. Time base: 5  $\mu$ s/div. (b) Input and inductor currents. From bottom to top: trace C1 (inductor current of phase 1), 500 mA/div; trace C2 (inductor current of phase 2), 500 mA/div; trace C3 (input current), 500 mA/div. Time base: 5  $\mu$ s/div.

A prototype of a coupled inductor with desired self and mutual inductances are obtained by using the proposed coupled inductor design method. The desired input current ripple is also obtained from experimental results obtained with the designed prototype. Therefore, the validity of the proposed coupled inductor design method has been confirmed.

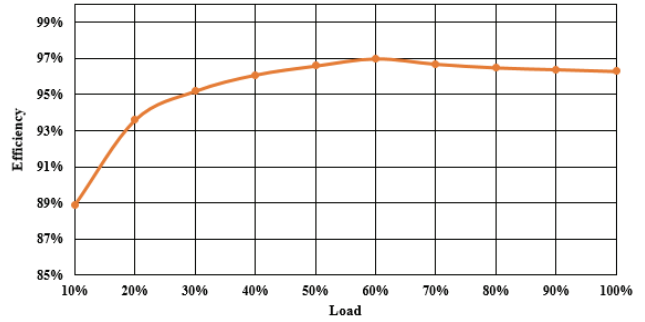


Fig. 10. Measured efficiency of a converter with an 18 V input voltage.

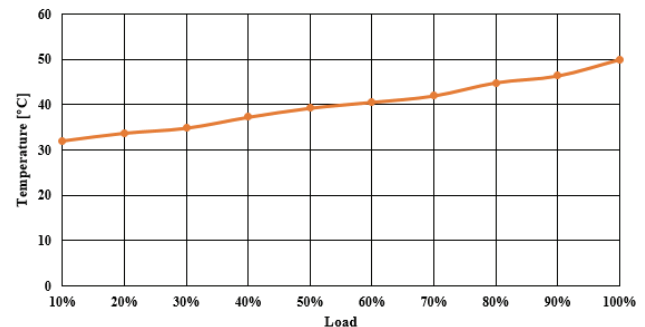
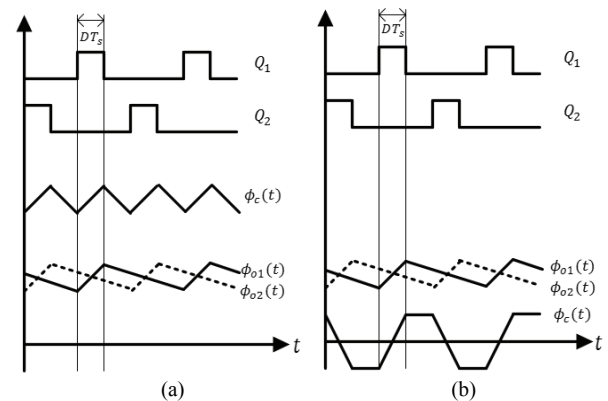


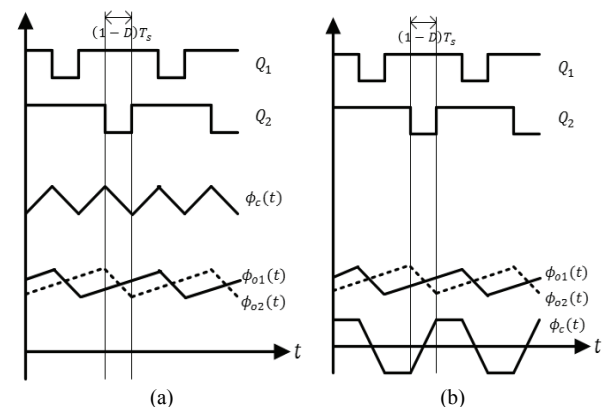
Fig. 11. Measured inductor temperature with an 18 V input voltage.



(a)

(b)

Fig. 12. Flux waveforms of center and outer legs when  $0 < D < 0.5$  (a) Inversely coupled. (b) Directly coupled.



(a)

(b)

Fig. 13. Flux waveforms of center and outer legs when  $0.5 < D < 1$ . (a) Inversely coupled. (b) Directly coupled.

## VI. CONCLUSIONS

In this paper, a coupled inductor design method for 2-phase interleaved boost converters has been proposed. To select a proper core size, an area product equation is newly derived. At the same time, by using the proposed coupled inductor design method, the wire size, number of turns and air gap length can be determined too. Finally, a design example indicates that the proposed coupled inductor design method is valid.

## APPENDIX

### Maximum flux density of the core

With the flux directions shown in Fig. 3, flux waveforms of the center and outer legs when  $0 < D < 0.5$  with inverse and direct coupling are shown in Fig. 12. For the inverse coupling, Fig. 3(a) shows that the flux of the center leg is the sum of the fluxes of the two outer legs. Therefore, during the  $DT_s$  period, the peak to peak flux of the center leg can be shown as:

$$\Delta\phi_c = \left[ \frac{\Delta\phi_o}{DT_s} - \frac{\Delta\phi_o}{(1-D)T_s} \right] DT_s = \frac{1-2D}{1-D} \Delta\phi_o, \quad (31)$$

where  $\Delta\phi_o$  is the peak to peak flux of the outer leg. For the direct coupling, Fig. 3(b) shows that the flux of the center leg is the difference between the fluxes of the two outer legs. Therefore, during the  $DT_s$  period, the peak to peak flux of the center leg can be given as:

$$\Delta\phi_c = \left[ \frac{\Delta\phi_o}{DT_s} + \frac{\Delta\phi_o}{(1-D)T_s} \right] DT_s = \frac{1}{1-D} \Delta\phi_o. \quad (32)$$

Fig. 13 shows flux waveforms of the center and outer legs when  $0.5 < D < 1$  with inverse and direct coupling. For the inverse coupling, during the  $(1-D)T_s$  period, the peak to peak flux of the center leg can be shown as:

$$\Delta\phi_c = - \left[ \frac{\Delta\phi_o}{DT_s} - \frac{\Delta\phi_o}{(1-D)T_s} \right] (1-D)T_s = \frac{2D-1}{D} \Delta\phi_o. \quad (33)$$

For the direct coupling, during the  $(1-D)T_s$  period, the peak to peak flux of the center leg can be given as:

$$\Delta\phi_c = \left[ \frac{\Delta\phi_o}{DT_s} + \frac{\Delta\phi_o}{(1-D)T_s} \right] (1-D)T_s = \frac{1}{D} \Delta\phi_o. \quad (34)$$

Hence, the maximum flux of the center leg can be expressed as:

$$\phi_{cmax} = \begin{cases} 2\phi_{odc} + \frac{\Delta\phi_c}{2} & \text{for inverse coupling} \\ \frac{\Delta\phi_c}{2} & \text{for direct coupling} \end{cases}, \quad (35)$$

where  $\phi_{odc}$  is the dc flux of the outer leg. The maximum flux of the outer leg for inverse coupling and direct coupling can be written as:

$$\phi_{omax} = \phi_{odc} + \frac{\Delta\phi_o}{2}. \quad (36)$$

From (31)-(36) it can be seen that, whether it is inversely coupled or directly coupled, the maximum flux of the center leg is always less than twice the maximum flux of the outer leg in all of the ranges of the duty cycle. This means that:

$$\phi_{cmax} < 2\phi_{omax}. \quad (37)$$

The maximum flux densities of the center leg  $B_{cmax}$  and the outer leg  $B_{omax}$  are presented as:

$$B_{cmax} = \frac{\phi_{cmax}}{A_e}, \quad (38)$$

$$B_{omax} = \frac{\phi_{omax}}{A_{eo}}. \quad (39)$$

Since  $A_e \approx 2A_{eo}$ , substituting this into (37)-(39) gives:

$$B_{omax} > B_{cmax}. \quad (40)$$

This means that the maximum flux density of the core  $B_{max}$  is the maximum flux density of the outer leg.

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