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프로그래머블 비디오 복호화기를 위한 구성요소의 성능 분석

김 재 현[a)], 박 구 만[a)‡]

Analysis of Components Performance for Programmable Video Decoder

Jaehyun Kim[a)] and Gooman Park[a)‡]

요 약

본 논문에서는 프로그래머블 멀티포맷 비디오 복호화기를 구성하기 위한 기본 모듈들의 요구 성능을 분석하고 제안하였다. 제안한 플랫폼의 목적은 고성능 FHD 비디오 복호화기 구성이다. 제안한 복호화기는 재구성 가능한 프로세서, 전용 비트스트림 코프로세서, 메모리 제어기, 움직임 보상용 캐쉬 및 플렉서블 하드웨어 가속기 등으로 구성되었다. 300MHz 클럭을 사용했을 때 HEVC로 부호화 된 초당 30 장의 FHD를 복호화 할 수 있는 모듈들의 성능에 대해서 분석하고 기본 성능을 제안하였다.

Abstract

This paper analyzes performances of modules in implementing a programmable multi-format video decoder. The goal of the proposed platform is the high-end Full High Definition (FHD) video decoder. The proposed multi-format video decoder consists of a reconfigurable processor, dedicated bit-stream co-processor, memory controller, cache for motion compensation, and flexible hardware accelerators. The experiments suggest performance baseline of modules for the proposed architecture operating at 300 MHz clock with capability of decoding HEVC bit-streams of FHD 30 frames per second.

Keyword : Cache, Coarse grain array, HEVC, Multi-format video decoder, Reconfigurable processor.

a) 서울과학기술대학교 나노IT디자인융합대학원(Seoul National University of Science and Technology, Graduate School of NID Fusion Technology)
‡ Corresponding Author : 박구만(Gooman Park)
E-mail: gmpark@seoultech.ac.kr
Tel: +82-2-970-6430
ORCID: https://orcid.org/0000-0002-7055-5568
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Ⅰ. INTRODUCTION

High Efficiency Video Coding (HEVC), which offers two times better efficiency than the existing compression standard H.264/Advanced Video Coding (AVC), has been widely used in various fields[1].

Since developing a method that separately implements an integrated SoC to each compression standard is a big loss in terms of cost, a multi-format decoder (MFD) has been developed in a manner that shares functional logics and memory resources[2]. While, a software solution offers quick and easy response to a variety of compression standards, it is relatively disadvantageous compared with the hardware solution in terms of power consumption and performance. In order to overcome this disadvantage, Kikuchi[3] proposed a method for use with a processor and a hardware accelerator. Entropy decoding complexity accounts for about 10% ~ 25% in the decoder complexity, and deviates according to the resolution and the amount of compressed bit-stream. If compression mode is only the inter-prediction, the operations related to motion compensation account for half of the overall complexity[4].

We suggested performance baseline of modules for the programmable multi-format video decoder capable of real-time decoding a variety of video compression standards.

Ⅱ. Related Work

The reconfigurable processor used in this paper is a high-performance Coarse Grain Reconfigurable Array (CGRA) processor consisting of a number of function units, to take full advantage of the parallelism of multimedia applications [5]. The reconfigurable processor supports two Very Long Instruction Word (VLIW) and Coarse Grain Array (CGA) modes. In this paper, we use a reconfigurable processor consisting of a 16-function unit, a shown in Fig. 1.

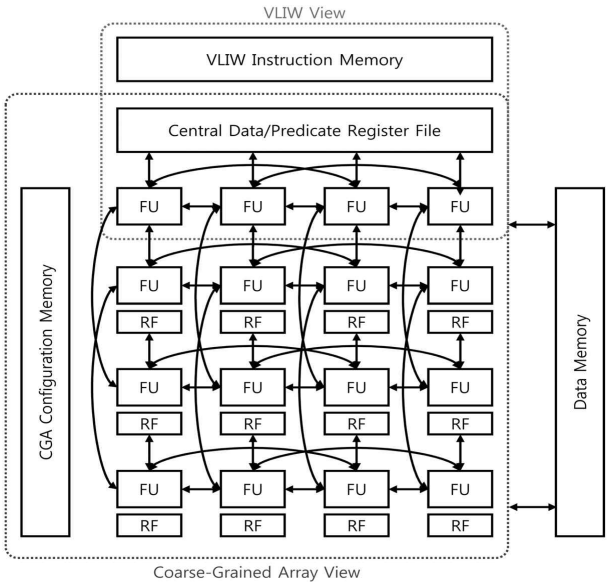

그림 1.재구성 가능한 프로세서의 구조
Fig. 1. Architecture of the Reconfigurable Processor

In this paper we use the entropy processor to accelerate the bit-stream process, the memory controller to reduce memory bandwidth, the hardware accelerator for motion compensation, and a parallel processing algorithm between the processor and the dedicated hardware accelerator.

Ⅲ. Programmable MFD

The proposed system is composed of a Bit-stream Processing Unit (BsPU) for bit-stream parsing and entropy decoding, a Memory Processing Unit (MemPU) to reduce the memory bandwidth of the external SDRAM in the video decoding process and accelerate the motion compensation calculation, and two reconfigurable processors for the acceleration process of the rest of the decoding module, except for entropy decoding.

We implement the bit-stream processor unit by a dedicated engine to accelerate Huffman and CABAC decoding to address all the compression standards, and process high bit rate streams. The bit-stream processing unit is com-

posed of an accelerator supporting bit acquisition, table mapping, and bit position updating to supply a real time bit-stream between the external memory and the entropy decoding engine.

1. Memory Processing Unit

The memory processing unit plays the role of memory controller for fast data transfer between the memory in the processor and an external SDRAM.

Maximizing the burst length of DRAM access with tile shape structure provides increased data transmission efficiency, and using multiple outstanding transactions reduces the memory access waiting time(latency).

Table 1 shows the desired clock frequency for the video decoding of the SD and FHD image using the proposed memory processing unit compared to the Direct Memory Access Controller (DMAC). In decoding SD (720x480) video, the proposed memory processing unit is required to operate at 140MHz, and improves performance by 18.6% compared to that achieved by the DMAC at 172MHz.

표 1. 메모리처리단의 성능
Table I. Performance of Memory Processing Unit

Resolution	DMAC	Memory Processing Unit
SD (720×480)	172 MHz	140 MHz
FHD (1920×1080)	1032 MHz	840 MHz

2. Cache for Motion Compensation

While supporting HEVC standard up to 4K resolution, we propose a cache system that can more effectively process a memory bandwidth problem than traditional caching technology. We design an optimum cache architecture to determine the relevant parameters in consideration of the specifications and cost of the video decoder. First, we investigate the average cache hit rate to determine the size of the cache through a combination of set and way in 8x8 tile size. We measure the cache hit rate by increasing the cache entry size from 48 to 2048. Table 2 shows that the cache hit rate is in the range of 69.9% ~ 71.5%, and that the most efficient entry size is 96. As a result of measuring the memory bandwidth for a variety of tile sizes, we can see that in terms of bandwidth, the 16 × 8 tile size shows the best efficiency.

표 2. 캐시 크기에 따른 캐쉬 히트 비율과 메모리 대역폭
Table 2. Cache hit ratio and Memory bandwidth according to cache size

Entry Size	Hit Ratio (%)	Tile Size	Bandwidth(MB/s)
48	69.96	16×16	790.60
96	71.32	16×8	686.39
1024	71.47	8×16	793.17
2048	71.48	8×8	731.36

Experimental results for a tile size of 16 × 8 with respect to the cache hit rate and data bandwidth in accordance with the set-way combination show that the 2set 48way structure offers a good cache hit rate and data bandwidth. The required DRAM bandwidth is about 4.5GB/s for 4 K 60 Hz video decoding, and Table 3 shows the experimental results of applying the determined cache parameters.

표 3. 압축률과 압축표준에 따른 캐시 히트율과 대역폭
Table 3. Cache hit ratio and Bandwidth according to compression ratio and compression standard

Bitrate	Codec	Hit Ratio (%)	Average B/W (MB/s)
High (64Mbps)	HEVC	69.84	875.89
	VP9	71.34	816.00
Low (32Mbps)	HEVC	70.10	824.50
	VP9	71.47	723.78

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Our experiments show that the proposed cache method offers a 70% cache hit rate, and has better performance than the 61.86% result of Shihao Wang [6]. We use a cache of 16x8 tile, 48way 2set, 12 Kb in size in this paper, and find more than 18% higher bandwidth reduction perform-

ance, while using the same cache size used by Shihao Wang.

3. Two-stage Parallel Processing

Table 4 shows the configuration of the main functions for parallel processing in the video decoding process.

표 4. 병렬처리를 위한 비디오 복호기의 기능들
Table 4. Video decoder functions for Parallel processing

Part		Functions
Bit-stream Processing Unit (BsPU)		Entropy Decoding De-Quantization, Intra Mode Decoding
Stage 1	VLIW	Load Neighbor Information MV Decoding
	CGA	Inverse Transform Intra Prediction (Y), Reconstruction
Stage 2	VLIW	Boundary Strength Store Neighbor Information
	CGA	Intra Prediction (U,V) De-Blocking filter, Sample Adaptive Offset

The remainder of the decoding process is composed of pixel decoding (Stage 1), post-processing of the restored pixel (Stage 2), and an acceleration process for motion compensation. After slice level entropy decoding, the first stage can parallel decode with the second stage.

Ⅳ. Experimental Results

In order to evaluate the performance of the proposed MFD, we tested our proposal using the most complicated compression standard HEVC.

The total memory used by the reconfigurable processor is 227 KB (instruction cache 96 KB, internal memory 80 KB, configuration memory 51 KB). The total hardware size of the proposed programmable decoder is 6.32 M gate count (logic 2.78 M G/C, memory 3.54 M G/C) at 45 nm process.

When using hardware accelerators for motion compensation, we improve the throughput by 30%, compared to the performance when using only software.

Ⅴ. Conclusion

This paper introduced analysis of desirable performances of some modules for the programmable multi-format video decoder based on a reconfigurable processor that can decode any type of compression standards, including HEVC and evaluated its performance.

Using the proposed programmable video decoder and suggested performances, we can reduce the period of product commercialization and upgrade functionality and performance even after product launch.

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