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Ringing Frequency Extraction Method Based on EMD and FFT for Health Monitoring of Power Transistors

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Abstract

Condition monitoring has been recognized as an effective and low-cost method to enhance the reliability and improve the maintainability of power electronic converters. In power electronic converters, high-frequency oscillation occurs during the switching transients of power transistors, which is known as ringing. The ringing frequency mainly depends on the values of the parasitic capacitance and stray inductance in the oscillation loop. Although circuit stray inductance is an important factor that leads to the ringing, it does not change with transistor aging. A shift in either the inside inductance or junction capacitance is an important failure precursor for power transistors. Therefore, ringing frequency can be used to monitor the health of power transistors. However, the switching actions of power transistors usually result in a dynamic behavior that can generate oscillation signals mixed with background noise, which makes it hard to directly extract the ringing frequency. A frequency extraction method based on empirical mode decomposition (EMD) and Fast Fourier transformation (FFT) is proposed in this paper. The proposed method is simple and has a high precision. Simulation results are given to verify the ringing analysis and experimental results are given to verify the effectiveness of the proposed method.

Key words: Condition monitoring, EMD, FFT, Frequency extraction, Power transistors, Ringing

I. INTRODUCTION

Power electronic converters have been widely used in many fields such as industry, military and aerospace due to their low noise and high efficiency [1]-[3]. However, with increases in the integration density and complexity level, reliability-related issues are becoming increasingly acute. To study the failure distribution of the different components in a power electronic system, an industry survey has been conducted and the results indicate that semiconductors are one of the most age-affected components [4]. In order to know the aging situation of power transistors to prevent catastrophic failures, several efforts in failure precursor parameter extraction have been made to monitor the health condition of power transistors. As reported in [5]-[8], the aging indicator parameters associated with power transistors include the threshold voltage, thermal resistance, on-resistance and parasitic capacitance/inductance of power transistors.

Increases in on-resistance are mainly caused by bond failure, which is a crack at the bond wire/chip interface due to the dissimilarity between the thermal expansion coefficients of Si and Al. To evaluate bond failures, the on-resistance is the most used failure indicator [9]-[11]. To identify variations of on-resistance, the most direct approach is to measure the on-state voltage and current for calculations. However, in live converters, the voltage across the transistor is under the alteration of the on-state level and the off-state voltage level. When measuring the on-state voltage, the measurement range of the voltage sensor must be set wide enough to sustain the off-state voltage. Otherwise, the voltage sensor can be saturated or even damaged, which results in further measurement failures due to the lack of recovery. To solve this problem, voltage clamp circuits are proposed to clamp the off-state voltage to a low value [9], [11]. However, these voltage clamp circuits often introduce problems such as time delays, voltage peaks and measurement offsets. To avoid the

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aforementioned problems, spread spectrum time domain reflectometry (SSTDR) is adopted to detect the on-resistance variations of MOSFETs [10]. However, this method needs to introduce additional hardware. It also needs to inject signals to the tested transistor. Most importantly, on-resistance-based methods all need to add extra circuits, which increase the system complexity and produce more power loss.

The increase in the thermal resistance is mainly caused by die solder layer failures, which are cracks at silicon die and copper substrate interfaces. To evaluate die solder layer failures, thermal resistance is often used. To identify the thermal resistance, the power loss on the transistor and junction temperature of the transistor need to be measured for calculation [12], [13]. To accurately calculate the power loss on the transistor, extra high-precision sensors need to be added, which increases system cost. The junction temperature, unlike the surface temperature, is difficult to measure directly by thermos-sensitive material. Although a lot of junction temperature estimation methods have been proposed [14], [15], their implementation approaches are highly complex.

Shifts of threshold voltage are mainly caused by degradation in the gate oxide of transistors. To monitor the threshold voltage in real-time, the most popular method is to simultaneously extract the drain current and the gate-to-source voltage [13], [14]. However, there is a problem similar to that in on-state voltage measurement when measuring the drain current. Moreover, capturing the threshold voltage accurately under high-speed switching is very difficult. Although increasing the driving resistance to slow the switching speed is an effective method, it is not suitable for on-line monitoring.

Variations of the parasitic capacitance/inductance are mainly caused by bond failures. Cracks at bond wire/chip interfaces or bond wire liftoff increases the parasitic inductance. The switching dynamic characteristics of MOSFETs/IGBTs, such as the turn-on/turn-off time, gate-voltage behavior and gate current, can be used to monitor this degradation [16]-[18]. However, these methods are not suitable for diodes. For improved commonality, frequency response (ringing) has been verified and adopted to monitor related degradation [19]-[21]. In power electronic converters, high-frequency oscillations occur during the switching transients of power transistors, which is known as ringing. In [19], a band-pass filter is used to extract the ringing current and FFT is used to acquire the ringing frequency spectrum characterization. The obtained ringing characteristic is used for transistor condition monitoring. However, in the case of unknown ringing characteristic, it is difficult to design such a band-pass filter. In [20], the matric pencil method was used to plot the pole locations associated with a ringing waveform. However, the aging information acquired from the pole locations may not be effective since other factors, such as the driving resistance and the load current, can also result in changes in the pole locations. In [21], by measuring the voltage across the stray inductance, a ringing frequency capture method based on FFT is proposed. However, the ringing frequency is affected by the input voltage, and the voltage across the stray inductance cannot provide information on the input voltage. To avoid these problems, by measuring the leg midpoint voltage, a ringing frequency extraction method based on EMD and FFT is proposed in this paper. The proposed method can obtain both the ringing frequency and the input voltage, which can provide effective information on the health of transistors. The proposed method is simple and has high precision.

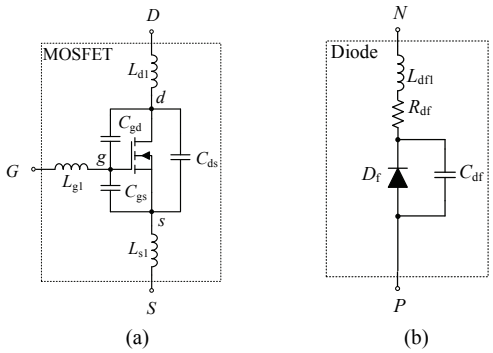

Fig. 1. Equivalent models of: (a) Power MOSFET; (b) Diode.

This paper is organized as follows. Section II analyzes the ringing characterization and the ringing frequency is shown to be a good failure indicator for power transistors. To accurately extract the ringing frequencies, a ringing frequency extraction method based on EMD and FFT is proposed in Section III. Simulations are carried out to verify the ringing analysis in Section IV. Experimental results are provided to demonstrate the validity of the proposed frequency extraction method in Section V. Finally, a summary is presented in Section VI.

II. Ringing Characterization Analysis

In this section, ringing during the switching process is deeply analyzed. As a basic circuit topology, a Buck converter is adopted as the object of analysis. Equivalent models of a power MOSFET and a diode that consider all of the crucial parasitic elements are shown in Fig. 1.

The considered parasitic elements of the power MOSFET are the drain-source capacitance C_{ds}, gate-source capacitance C_{gs}, gate-drain capacitance C_{gd} (C_{rss}), drain inductance L_{d1}, source inductance L_{s1}, and gate inductance L_{g1}. $C_{iss} = C_{gs} + C_{gd}$ and $C_{oss} = C_{ds} + C_{gd}$ are denoted as the input and output capacitances of the MOSFET, respectively. The considered parasitic elements of the power diode are its junction capacitance C_{df}, on-state resistance R_{df}, and parasitic inductance L_{df1}. With these taken into consideration, an equivalent circuit model is shown in Fig. 2, where L_{d2}, L_{s2}, L_{g2}, and L_{df2} are the stray inductances external to the MOSFET and diode in the circuit. For the sake of convenience, the

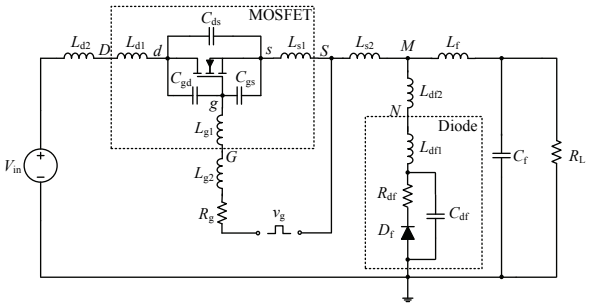

Fig. 2. Equivalent circuit model of a Buck converter considering the parasitic parameters.

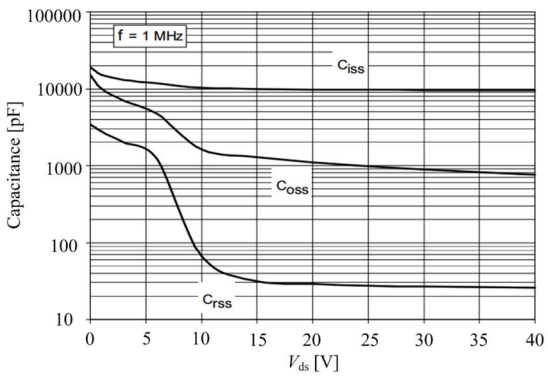

Fig. 3. Nonlinear capacitance obtained from a datasheet.

parasitic inductances in the power loop are denoted as L_e = L_{d1}+ L_{d2} + L_{s2}+ L_{df1}+ L_{df2}. R_g is the driving resistance and the gate signal is assumed to flip between 0 and V_g with a zero rise time and a zero fall time in the analysis. L_f is the output filter inductor and C_f is the output filter capacitor. R_L is the load resistance.

Referring to a datasheet of the MOSFET IXFK64N50P, the parasitic capacitances characteristics are presented in Fig. 3, where v_{ds} is the drain-source voltage. It can be found that the junction capacitances of the power MOSFET are affected by the drain- source voltage. Similarly, the junction capacitances of the power diodes are affected by its reverse voltage. Therefore, the voltage across a MOSFET or diode is an important factor that needs to be considered for health evaluation.

A. Turn-On Switching Ringing

Turn-on ringing occurs after a MOSFET is turned on and the ringing loop is denoted by the red line in Fig. 4(a). During this transient, the MOSFET can be equivalent to its on-resistance $R_{ds(on)}$ and the diode can be equivalent to its junction capacitor C_{df}. According to the oscillation loop, it has been reported that oscillation damping can be used to monitor the variation of $R_{ds(on)}$ in [20]. However, it can be seen that the driver resistance R_g affects the oscillation damping due to the stray inductance L_{s1}, which is shared by both the driver and power loops. For this consideration, the ringing equivalent circuit can be derived as Fig. 4(b). In

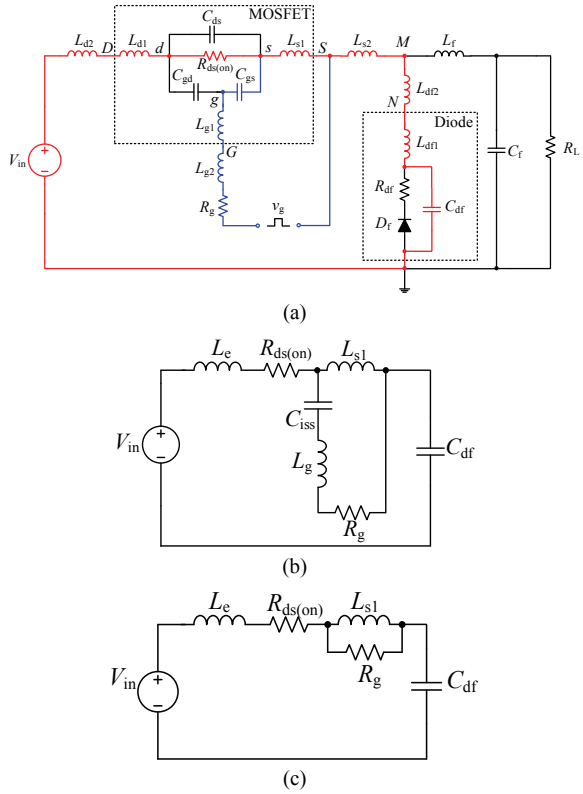

Fig. 4. Turn-on ringing equivalent circuits: (a) Circuit 1; (b) Circuit 2; (c) Circuit 3.

general, the gate drive circuit is placed close enough to the MOSFET to decrease the oscillation introduced by L_g, where L_g= L_{g1}+ L_{g2}. Due to the large value of C_{iss} and the small value of L_g, the impedance of C_{iss} and L_g at the oscillation frequency is much smaller than R_g, i.e., $1/C_{iss}s_{ringing}$+ $L_g s_{ringing}$ << R_g. Therefore, to simplify the analysis, an equivalent circuit model can be simplified as shown in Fig. 4(c).

According to Fig. 4(c), the frequency-domain expression of the voltage across C_{df} can be derived as:

$$\frac{v_{df}(s)}{V_{in}(s)} = \frac{\dfrac{1}{C_{df\_Vin}s}}{R_{ds(on)} + L_{s1}s//R_g + L_e s + \dfrac{1}{C_{df\_Vin}s}} = \frac{(L_{s1}s+R_g)}{\left\{L_{s1}L_e C_{df\_Vin}s^3 + \left[R_g R_{ds(on)} C_{df\_Vin} + L_{s1}\right]s + \right\}} \quad (1)$$

where C_{df_Vin} is the capacitance of C_{df} at the voltage V_{in}. Usually, it is satisfied that:

$$\frac{L_{s1}L_e C_{df\_Vin}}{R_g(L_e+L_{s1}) + R_{ds(on)}L_{s1}} \square \frac{R_g(L_e+L_{s1}) + R_{ds(on)}L_{s1}}{R_g} \quad (2)$$

$$R_{ds(on)}L_{s1} \square R_g(L_e+L_{s1}) \quad (3)$$

Accordingly, Equ. (1) can be simplified as:

$$\frac{v_{df}(s)}{V_{in}(s)} \approx \frac{R_g}{R_g(L_e+L_{s1})C_{df\_Vin}s^2 + \left[R_gR_{ds(on)}C_{df\_Vin}+L_{s1}\right]s+R_g} \tag{4}$$

For a second-order system as in (4), the oscillation damping and frequency can be calculated as:

$$\begin{cases} \zeta_{on} = \dfrac{R_{ds(on)}\sqrt{C_{df\_Vin}}}{2\sqrt{L_e+L_{s1}}} + \dfrac{L_{s1}}{2R_g\sqrt{(L_e+L_{s1})C_{df\_Vin}}} \\ f_{on\_n} = \dfrac{1}{2\pi\sqrt{(L_e+L_{s1})C_{df\_Vin}}} \\ f_{on\_d} = f_{on\_n}\sqrt{1-\xi_{on}^2} \end{cases} \tag{5}$$

where ζ_{on}, f_{on_n} and f_{on_d} are the oscillation damping coefficient, undamped oscillation frequency and damped oscillation frequency, respectively. In most cases, it is satisfied that:

$$R_{ds(on)}R_gC_{df\_Vin} \gg L_{s1} \tag{6}$$

which means that R_g dominates the damping value of the turn-on ringing. In this case, it is hard to evaluate the power MOSFET aging associated with R_{dson} from the damping detection.

B. Turn-Off Switching Ringing

Similar to the derivation of the turn-on ringing circuit model, an equivalent circuit model of the turn-off ringing can be derived as shown in Fig. 5.

According to the derived model shown in Fig. 5(c), the oscillation damping and frequency of the turn-off ringing can be calculated as:

$$\begin{cases} \zeta_{off} = \dfrac{R_{df}\sqrt{C_{oss\_Vin}}}{2\sqrt{L_e+L_{s1}}} + \dfrac{L_{s1}}{2R_g\sqrt{(L_e+L_{s1})C_{oss\_Vin}}} \\ f_{off\_n} = \dfrac{1}{2\pi\sqrt{(L_e+L_{s1})C_{oss\_Vin}}} \\ f_{off\_d} = f_{on\_n}\sqrt{1-\xi_{off}^2} \end{cases} \tag{7}$$

where C_{oss_Vin} is the capacitance of C_{oss} at the voltage V_{in}. In most power electronic converters, it also satisfies:

$$R_{df}R_gC_{oss\_Vin} \gg L_{s1} \tag{8}$$

which means that it is hard to evaluate the diode aging associated with R_{df} from the damping information.

Although an increase in on-resistance is an aging indicator for the bond failure of power transistors, the damping coefficient is not a good indicator to evaluate the transistor aging associated with on-resistance. Actually, a degradation at the contact area of the bonding wire metallization causes increased in both the on-resistance (R_{dson} and R_{df}) and parasitic inductance (L_{s1}/L_{d1} and L_{df1}). Combining Equ. (5) and Equ. (7), it can be found that the ringing frequency is decreased due to a bond wire failure. Therefore, a shift of the switching ringing frequency is used to evaluate bond wire degradation for the transistors in this paper.

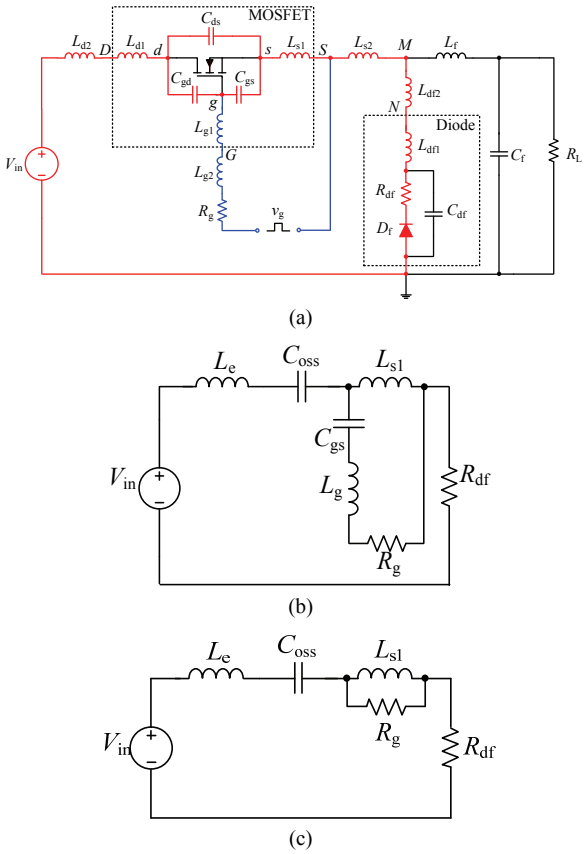

Fig. 5. Turn-off ringing equivalent circuits: (a) Circuit 1; (b) Circuit 2; (c) Circuit 3.

III. Proposed Ringing Frequency Extraction Method

To obtain the input voltage and the ringing frequency simultaneously, v_M is chosen for ringing frequency extraction. In order to extract the ringing frequency from the signal v_M, the proposed method is illustrated in Fig. 6. The ringing frequencies obtaining process is divided into four steps:

A. Step 1 (Pre-processing)

To acquire useful ringing signals, the signal v_M needs pre-processing. When off-to-on ringing occurs on the high-voltage level, a high-pass filter is adopted to remove the dc component. In addition to a dc component, v_M contains a switching-frequency component. Therefore, the cut-off frequency of the high-pass filter should be set higher than switching frequency. However, it should be lower than the ringing frequency. 5 times the switching frequency is chosen in this paper. The on-to-off ringing occurs on the low-voltage level and on-to-off ringing data can be directly acquired by step 2.

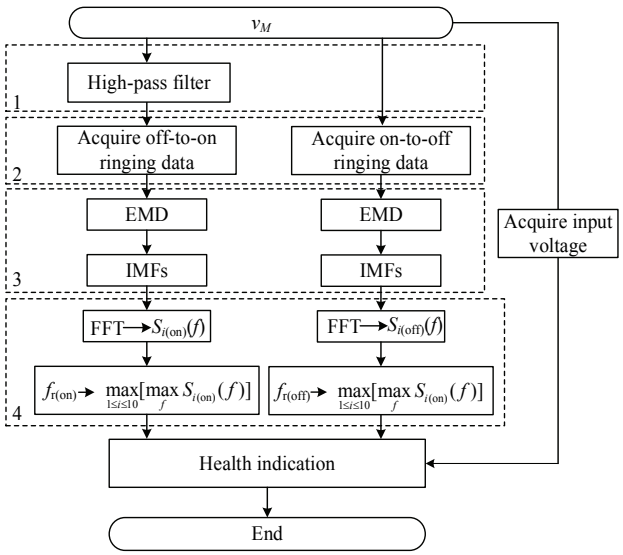

Fig. 6. Flow chart of the proposed health indication for power transistors.

B. Step 2 (Obtaining Ringing Data)

The off-to-on and on-to-off ringing data are obtained as follows:

1) According to the phenomenon where the maximum voltage peak is caused by the off-to-on ringing, the first zero crossing point after the maximum voltage peak is chosen as the starting point to extract the off-to-on ringing data.
2) According to the phenomenon where the minimum voltage valley is caused by the on-to-off ringing, the first zero crossing point after the minimum voltage valley is chosen as the starting point to extract the on-to-off ringing data.

The number of selected ringing signal data is determined by the switching frequency and the sampling frequency.

C. Step 3 (Obtaining IMFs by EMD)

Empirical mode decomposition (EMD) [22] is an emerging time-frequency signal processing technique that has been used in many fields, such as earthquake prediction and mechanical fault diagnostics [23], [24]. EMD can decompose an input signal into several intrinsic mode functions (IMFs) in different specific frequency bands. Fig. 7 shows the sifting process of IMFs, and the detailed steps are shown as follows. First, take the input signal $x(t)$ and find all of the local extrema. Then connect all of the local maxima by the cubic spline as shown in the upper envelope, and connect all of the minima by the cubic spline as shown in the lower envelope. The mean of the upper envelope and lower envelope is designated as $m_1(t)$, as shown in Fig. 7, and the first component $h_1(t)$ is designated as:

$$h_1(t) = x(t) - m_1(t) \tag{9}$$

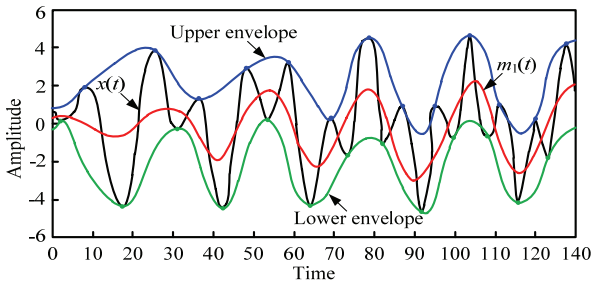

Fig. 7. Sifting process: original signal, $x(t)$; upper envelope (blue line); lower envelope (green line); mean of the upper and lower envelopes (red line), $m_1(t)$.

$h_1(t)$ is denoted as the first IMF if it satisfies [22]:

1) In the entire data set of $x(t)$, the number of zero crossings and extrema must differ at most by one.
2) At each instant t, the mean value of the envelope defined by the local maxima and the envelope defined by the local minima is near to zero.

If $h_1(t)$ is not an IMF, it is treated as the original signal and the sifting process is repeated:

$$h_{11}(t) = h_1(t) - m_{11}(t) \tag{10}$$

where $m_{11}(t)$ is the mean value defined by the upper and lower envelope of $h_1(t)$. The sifting process is repeated and until k times, $h_{1k}(t)$ becomes an IMF:

$$h_{1k}(t) = h_{1(k-1)}(t) - m_{1(k-1)}(t) \tag{11}$$

Then h_{1k} is designated as the first IMF component from $x(t)$. Repeating the steps above, $x(t)$ can be decomposed as:

$$x(t) = \sum_{i=1}^{n} c_i(t) + r_n(t) \tag{12}$$

where $c_i(t)$ (i-1,2,…,n) is a set of IMFs of signal $x(t)$. The first IMF is the decomposition of the signal component with the highest frequency. The components of lower frequencies are decomposed in order in the next IMFs. The IMFs related to the off-to-on ringing and the on-to-off ringing are denoted as $c_{i(on)}(t)$ and $c_{i(off)}(t)$, respectively. Ten off-to-on IMFs ($c_{i(on)}(t)$, i=1,2,3,…,10) and ten on-to-off IMFs ($c_{i(off)}(t)$, i=1,2,3,…,10) are chosen for FFT analysis.

D. Step 4 (Obtaining Ringing Frequencies by FFT)

With the obtained IMFs, a spectrum analysis is conducted by FFT. $S_{i(on)}(f)$ and $S_{i(off)}(f)$ are the frequency spectrums of $c_{i(on)}(t)$ and $c_{i(off)}(t)$, respectively. The frequency corresponding to the maximum peak value of $S_{i(on)}(f)$ is the identified off-to-on ringing frequency, and the frequency corresponding to the maximum peak value of $S_{i(off)}(f)$ is the identified on-to-off ringing frequency.

The health of the power transistors are determined by using the identified frequencies along with the identified input voltage.

TABLE I
CONVERTER PARAMETERS

Parameters	Variable	Value
input voltage	V_{in}/V	50
filter inductance	L_f/μH	100
filter capacitance	C_f/μF	470
driving resistance	R_g/Ω	10
load resistance	R_L/Ω	10
duty cycle	D	0.5
switching frequency	f_s/kHz	100

TABLE II
TRANSISTORS PARAMETERS

Variable	Value	Variable	Value
C_{oss_50V}/pF	650	L_{d1}/nH	0.2
C_{df_50V}/nF	1.54	L_{d2}/nH	1
$R_{ds(on)}$/mΩ	50	L_{s1}/nH	1
R_{df}/mΩ	10	L_{s2}/nH	1
L_{g1}/ nH	0.2	L_{df1}/nH	0.2
L_{g2}/ nH	1	L_{df2}/nH	1

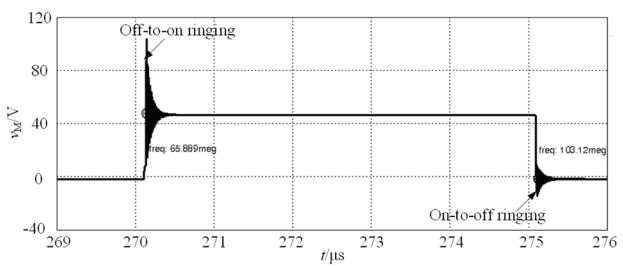

Fig. 8. Simulation waveform of switching ringings.

IV. SIMULATION STUDIES

In order to verify the analysis in Section II, a Buck converter model is built and simulated in SABER. The converter parameters are listed in Table I and the transistors parameters are listed in Table II.

Fig. 8 shows a simulation waveform of the switching ringings, where the measured turn-on ringing frequency is 65.889MHz, and the measured turn-off ringing frequency is 103.12MHz. According the used transistors parameters, the calculated undamped turn-on and turn-off ringing frequencies are 67.28MHz and 104.09MHz, respectively. These figures are consistent with the results in the waveform. Therefore, the ringing frequency is an effective parameter to monitor variation of the parasitic capacitance and inductance for the power transistors.

To verify the effect of R_g on the ringing damping caused by L_{s1}, L_{s1} is removed and L_{s2} is increased to 2nH for comparison. Origin and adjusted turn-on ringing waveforms are shown in Fig. 9(a). It can be seen that the ringing damping is affected by R_g due to the existence of L_{s1}. To further illustrate that variations of the on-resistance have little effect on ringing,

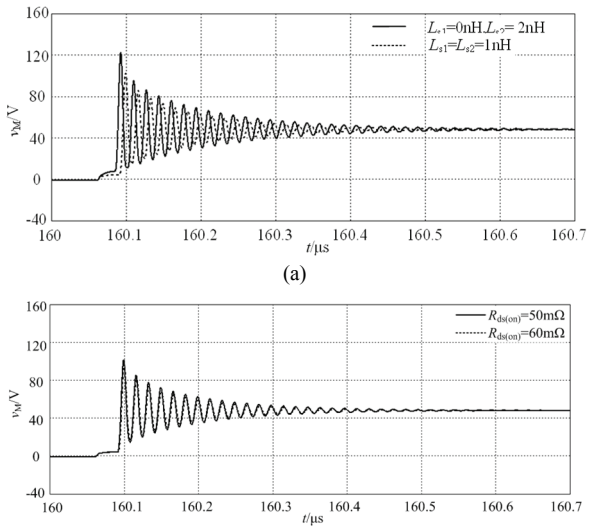

Fig. 9. Simulation waveform under different conditions: (a) With a different parasitic inductance; (b) With a different on-resistance.

$R_{ds(on)}$ is increased to 60 mΩ and the resulting simulation waveforms are shown in Fig. 9(b). In general, once $R_{ds(on)}$ is increased 20%, the power MOSFET is indicated to be lapsed. However, from Fig. 9(b), little difference is made when $R_{ds(on)}$ is increased 20%. Therefore, according to these comparisons, it can be seen that it is hard to evaluate the power MOSFET aging associated with R_{dson} from the ringing information.

V. EXPERIMENTAL RESULTS

In order to verify the effectiveness of the proposed frequency extraction method, an open-loop Buck converter has been constructed. The main circuit parameters are as follows: input voltage: 50V; duty cycle: 0.5; switching frequency: 20kHz; switch: IXYS IXFK64N50P; diode: IXYS DSEP60-06A; filter capacitor: 470μF/100V; output resistance: 10Ω; control IC: SG3535; and driving IC: IXDN609PI. For each measurement, one switching cycle is acquired by the oscilloscope (MDO3000) and the sampling frequency is 2.5GHz. The identification algorithm is implemented in MATLAB. The cut-off frequency of the high-pass filter is designed to 1MHz in MATLAB. Fig. 10(a) shows sampled ringing waveform, where a high dc voltage offset can be found. The filtered turn-on ringing and turn-off ringing signals are shown in Fig. 10(b) and Fig. 10(c) respectively. It can be seen from these figures that the maximum voltage peak is caused by the turn-on ringing.

Then the obtained turn-on and turn-off ringing signals are decomposed to a set of IMFs. Based on FFT, the peak amplitude of each IMF frequency spectrum can be calculated. The peak amplitude and corresponding frequency for each of the amplitude-frequency curves for turn-on ringing are listed in Table III. It can be seen that $S_{4(on)}(f)$ has the maximum A_{peak}

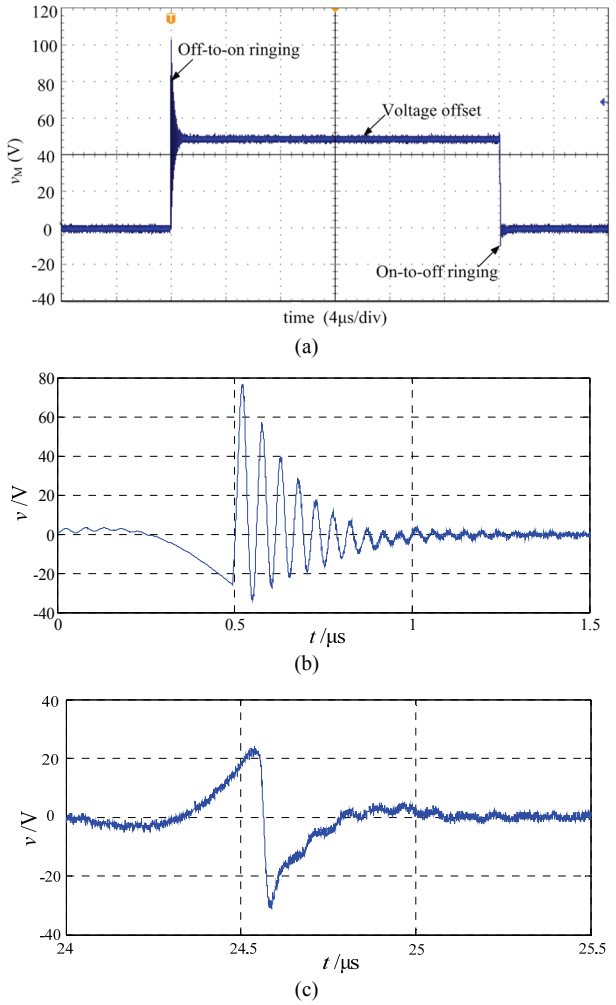

Fig. 10. Experimental waveforms: (a) ringing waveform in an oscilloscope; (b) Filtered turn-on ringing waveform; (c) Filtered turn-off ringing waveform.

TABLE III
AMPLITUDE-FREQUENCY CURVE PARAMETERS OF THE TURN-ON RINGING IMFS

$S_{i(on)}(f)$	1	2	3	4	5
A_{peak}	0.011	0.039	0.05	1.55	0.17
f/MHz	70.2	34.1	22.4	20.0	21.1
$S_{i(on)}(f)$	6	7	8	9	10
A_{peak}	0.09	0.19	0.4	0.21	0.21
f/MHz	19.7	3.5	2.3	1.8	1.4

TABLE IV
AMPLITUDE-FREQUENCY CURVE PARAMETERS OF THE TURN-OFF RINGING IMFS

$S_{i(off)}(f)$	1	2	3	4	5
A_{peak}	0.01	0.01	0.02	0.03	0.04
f/MHz	74.0	61.9	69.1	80.7	54.7
$S_{i(off)}(f)$	6	7	8	9	10
A_{peak}	0.05	0.155	0.09	0.04	0.07
f/MHz	14.2	11.6	3.8	2.3	1.7

TABLE V
MEASURED RINGING FREQUENCIES UNDER DIFFERENT INPUT VOLTAGES

V_{in}/V	20	40	50	60
$V_{in\_indentified}$/V	20.8	40.6	50.8	61.2
f_{on}/MHz	16.7	17.9	20.0	22.3
f_{off}/MHz	9.02	10.7	11.6	12.8

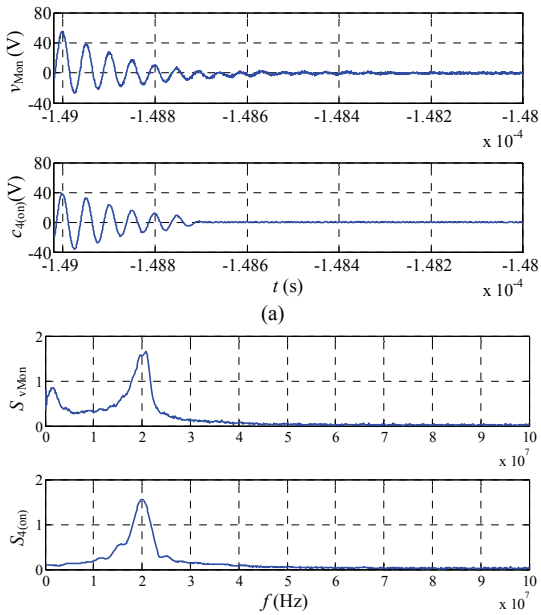

Fig. 11. Comparison of the turn-on ringing signal and $c_{4(on)}$: (a) Comparison of waveforms; (b) Comparison of frequency spectrums.

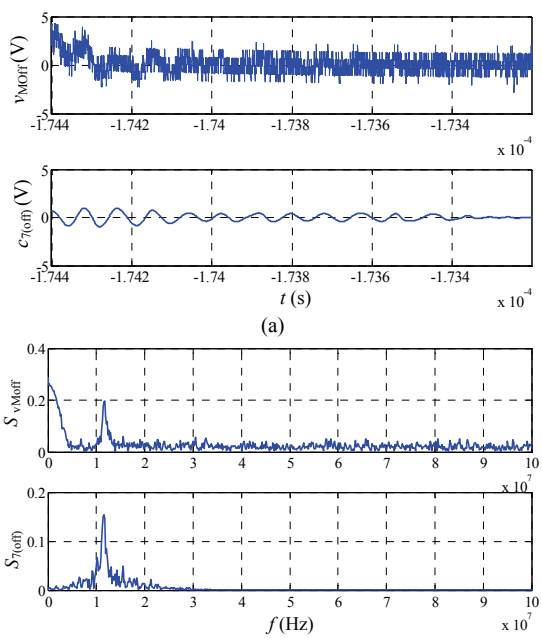

Fig. 12. Comparison of the turn-off ringing signal and $c_{7(off)}$: (a) Comparison of waveforms; (b) Comparison of frequency spectrums.

and that the corresponding frequency is 20.0MHz. Fig. 11 shows a comparison of the obtained turn-on ringing signals.

To verify that the proposed method can be used to monitor variations in ringing frequency, the input voltage is changed and the obtained results under different input voltages are shown in Table V. It can be seen that the ringing frequencies are increased with an increasing of the input voltages. This agrees with the capacitance characteristics shown in Fig. 2.

VI. CONCLUSIONS

A ringing frequency extraction method based on EMD and FFT for health monitoring of power transistors is proposed in this paper.

1) Ringing characterization is analyzed. The problems with using ringing damping for health monitoring are pointed out and ringing frequency is shown to be a good failure indicator for power transistors.
2) v_M is used for ringing frequency extraction and a non-invasive and easy to implement ringing frequency extraction method based on EMD and FFT is proposed.
3) When compared to existing methods, the proposed method can simultaneously extract the turn-on ringing frequency, turn-off ringing frequency and input voltage from only one signal detection point. In addition, this method is easier to realize and provides more information.
4) Simulation results are presented to verify the analysis of ringing characterization.
5) Experimental results are presented to demonstrate the validity of the proposed frequency extraction method. By comparing the obtained ringing signals with the identified IMF, the effectiveness of the proposed method is confirmed.

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